

# SCH5027E

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- SMBus Isolation Circuitry (2 sets external and 1 set internal for Hardware Monitoring Block)
- SMBus 2.0 compliant interface for Hardware Monitoring
- LED Control (2)
- Fan Control
  - 5 PWM (Pulse width Modulation) Outputs
  - Low frequency and high frequency PWM support
  - 6 Fan Tachometer Inputs
  - Programmable automatic fan control based on temperature
  - Interrupt Pin for out-of-limit Fantach Events
  - Fantach events generate PME's
- Temperature Monitor
  - Monitoring of Two Remote Thermal Diodes
  - Processor temperature monitoring by PECI
  - Internal Ambient Temperature Measurement
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Temperature Indication
  - Thermal events generate PME's
  - Configurable offset for internal or external temperature channels.
- Voltage Monitor
  - Monitor Power supplies (2 at 1.125V, one at 5V, one each for Vccp, Vbat, VTR, and VCC)
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Voltage Indication
  - Voltage events generate PME's
- Security Features
  - Security Key Register (32 byte) for Device Authentication
- 3 VID (Voltage Identification) Inputs
- Phoenix Keyboard BIOS ROM
- 128-Pin QFP, RoHS Compliant Package

## Description

The SCH5027E is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. SCH5027E also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

The SCH5027E's hardware monitoring capability includes temperature, voltage and fan speed monitoring. It has the ability to alert the system to out-of-limit conditions and automatically control the speeds of multiple fans. There are four analog inputs for monitoring external voltages, two at 1.125V, one at 5V and one at 2.25V for Vccp (core processor voltage). There is also internal monitoring of the SIO's VCC, VTR, and Vbat power supplies. The SCH5027E is capable of monitoring two external diodes, one internal ambient temperature sensor or retrieving temperatures from external processors that implement the PECI interface. The

PECI implementation in the SCH5027E includes support for the PECI REQUEST# and PECI AVAILABLE signals that are used to wake processors from the C3/C4sleep states. There are three pulse width modulation (PWM) outputs with high frequency support that may be controlled by the auto fan block, as well as four fan tachometer inputs. There are two additional software controlled PWM inputs with associated tachometer inputs that may be used to monitor fans. The nHWM\_INT pin is implemented to indicate out-of-limit temperature, voltage, and FANTACH conditions. The hardware monitoring block of the SCH5027E is accessible via the System Management Bus (SMBus). The same interrupt event reported on the nHWM\_INT pin also creates PME wakeup events and speaker alarm annunciation.

The SCH5027E also allows for a two or three piece linear fan function.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST, SMBus buffers, and buffered PCI reset outputs.

The SCH5027E incorporates complete legacy Super I/O functionality including an 8042 based keyboard and mouse controller, an IEEE 1284, EPP, and ECP compatible parallel port, one serial port that is 16C550A UART compatible, one IrDA 1.0 infrared ports, and a floppy disk controller with Microchip's true CMOS 765B core and enhanced digital data separator. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures and is software and register compatible with Microchip's proprietary 82077AA core. System related functionality, which offers flexibility to the system designer, General Purpose I/O control functions, control of two LED's, and fan control using fan tachometer inputs and pulse width modulator (PWM) outputs.

The SCH5027E is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes support for keyboard and mouse wake-up events.

The SCH5027E supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, DMA Channel and hardware IRQ of each logical device in the SCH5027E may be reprogrammed through the internal configuration registers. There are up to 480 (960 - Parallel Port) I/O address location options, a Serialized IRQ interface, and Three DMA channels.

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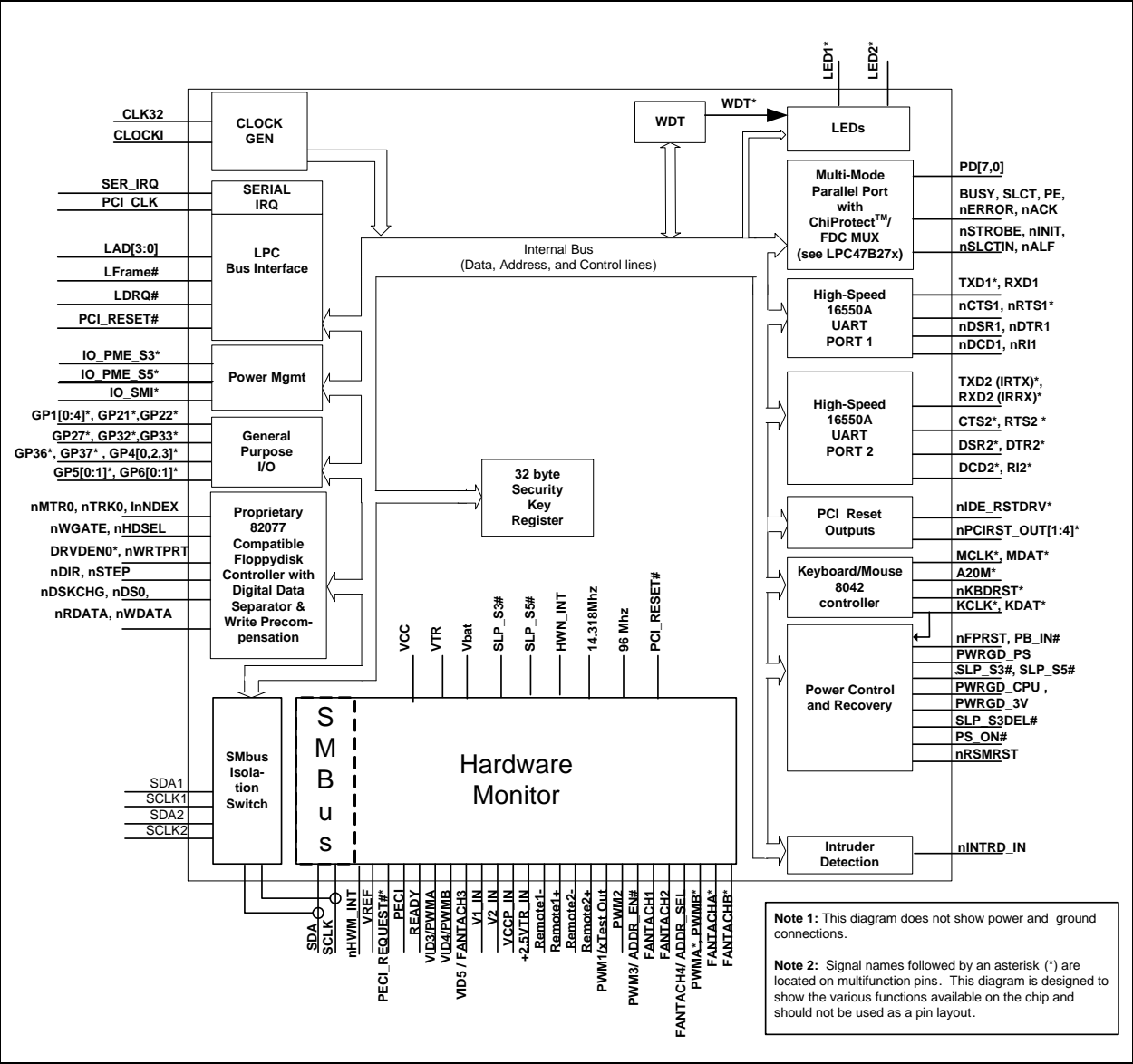
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# SCH5027E

## BLOCK DIAGRAM

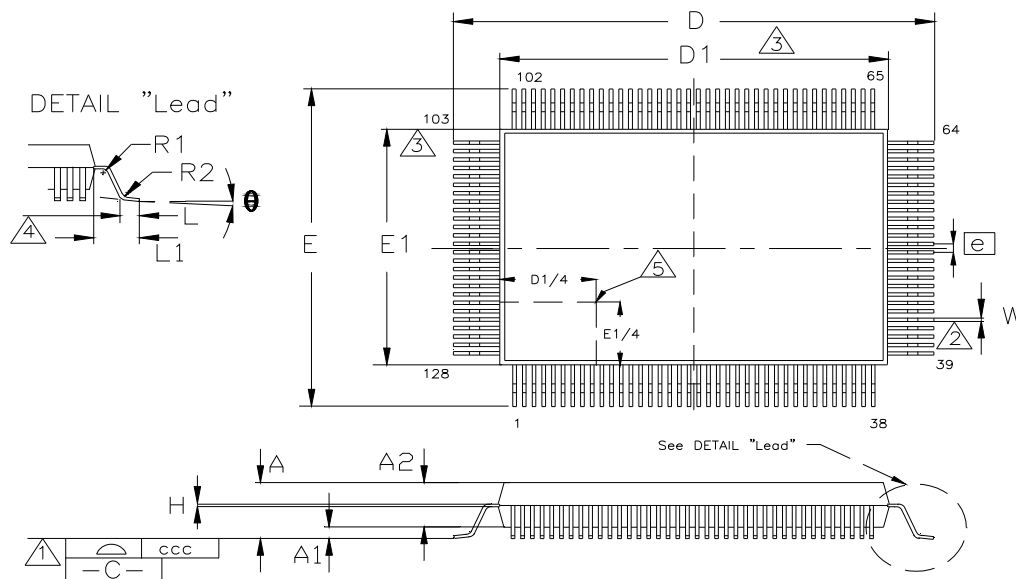
FIGURE 1: SCH5027E BLOCK DIAGRAM



## PACKAGE OUTLINE

**Note:** For the most current package drawings, see the Microchip Packaging Specification at: <http://www.microchip.com/packaging>.

## 128 Pin QFP Package Outline, 14X20X2.7 Body, 3.2 mm Footprint



	Min	Nominal	Max	Remarks
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.00	23.20	23.40	X Span
D1	19.90	20.00	20.10	X body Size
E	17.00	17.20	17.40	Y Span
E1	13.90	14.00	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.60	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.30	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

**Note 1:** Controlling Unit: millimeter.

**2:** Controlling Unit: millimeter.

**3:** Tolerance on the position of the leads is  $\pm 0.04$  mm maximum.

**4:** Package body dimensions D1 and E1 do not include the mold protrusion.

**5:** Maximum mold protrusion is 0.25 mm.

**6:** Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

**7:** Details of pin 1 identifier are optional but must be located within the zone indicated.

## APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001784A (07-03-14)	Replaces previous SMSC version Rev. 0.2 (02-11-09)	

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