

- Fan Control
 - 5 PWM (Pulse width Modulation) Outputs
 - Two and three piece linear fan function options.
 - Low frequency and high frequency PWM support
 - 6 Fan Tachometer Inputs
 - Programmable automatic fan control based on temperature
 - Interrupt Pin for out-of-limit Fantach Events
 - Fantach events generate PME's and/or Speaker warning
- Temperature Monitor
 - Monitoring of Two Remote Thermal Diodes
 - Internal Ambient Temperature Measurement
 - Limit Comparison of all Monitored Values
 - Interrupt Pin for out-of-limit Temperature Indication
 - Thermal events generate PME's and/or Speaker warning
 - Configurable offset for internal or external temperature channels.
- Voltage Monitor
 - Monitor Power supplies (5V, +5VTR, +12V, Vccp, Vbat, VTR, and VCC)
 - Limit Comparison of all Monitored Values
 - Interrupt Pin for out-of-limit Voltage Indication
 - Voltage events generate PME's and/or Speaker warning
- Security Features
 - Security Key Register (32 byte) for Device Authentication
- 6 VID (Voltage Identification) Inputs
- Phoenix Keyboard BIOS ROM
- 128-Pin, QFP RoHS Compliant Package

Description

The SCH5017 is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. SCH5017 also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

The SCH5017's hardware monitoring capability includes temperature, voltage and fan speed monitoring. It has the ability to alert the system to out-of-limit conditions and automatically control the speeds of multiple fans. There are four analog inputs for monitoring external voltages of +5V, +5VTR, +12V and Vccp (core processor voltage), as well as internal monitoring of the SIO's VCC, VTR, and Vbat power supplies. The SCH5017 includes support for monitoring two external temperatures via thermal diode inputs and an internal sensor for measuring ambient temperature. The nHWM_INT pin is implemented to indicate out-of-limit temperature, voltage, and FANTACH conditions. The hardware monitoring block of the SCH5017 is accessible via the System Management Bus (SMBus). The same interrupt event reported on the nHWM_INT pin also creates PME wakeup events and speaker alarm annunciation.

The SCH5017 also allows for a two or three piece linear fan function.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST, SMBus buffers, and buffered PCI reset outputs.

The SCH5017 incorporates complete legacy Super I/O functionality including an 8042 based keyboard and mouse controller, an IEEE 1284, EPP, and ECP compatible parallel port, one serial port that is 16C550A UART compatible, one IrDA 1.0 infrared ports, and a floppy disk controller with Microchip's true CMOS 765B core and enhanced digital data separator. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures and is software and register compatible with Microchip's proprietary 82077AA core. System related functionality, which offers flexibility to the system designer, General Purpose I/O control functions, control of two LED's, and fan control using fan tachometer inputs and pulse width modulator (PWM) outputs.

The SCH5017 is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes support for keyboard and mouse wake-up events.

The SCH5017 supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, DMA Channel and hardware IRQ of each logical device in the SCH5017 may be reprogrammed through the internal configuration registers. There are up to 480 (960 - Parallel Port) I/O address location options, a Serialized IRQ interface, and Three DMA channels.

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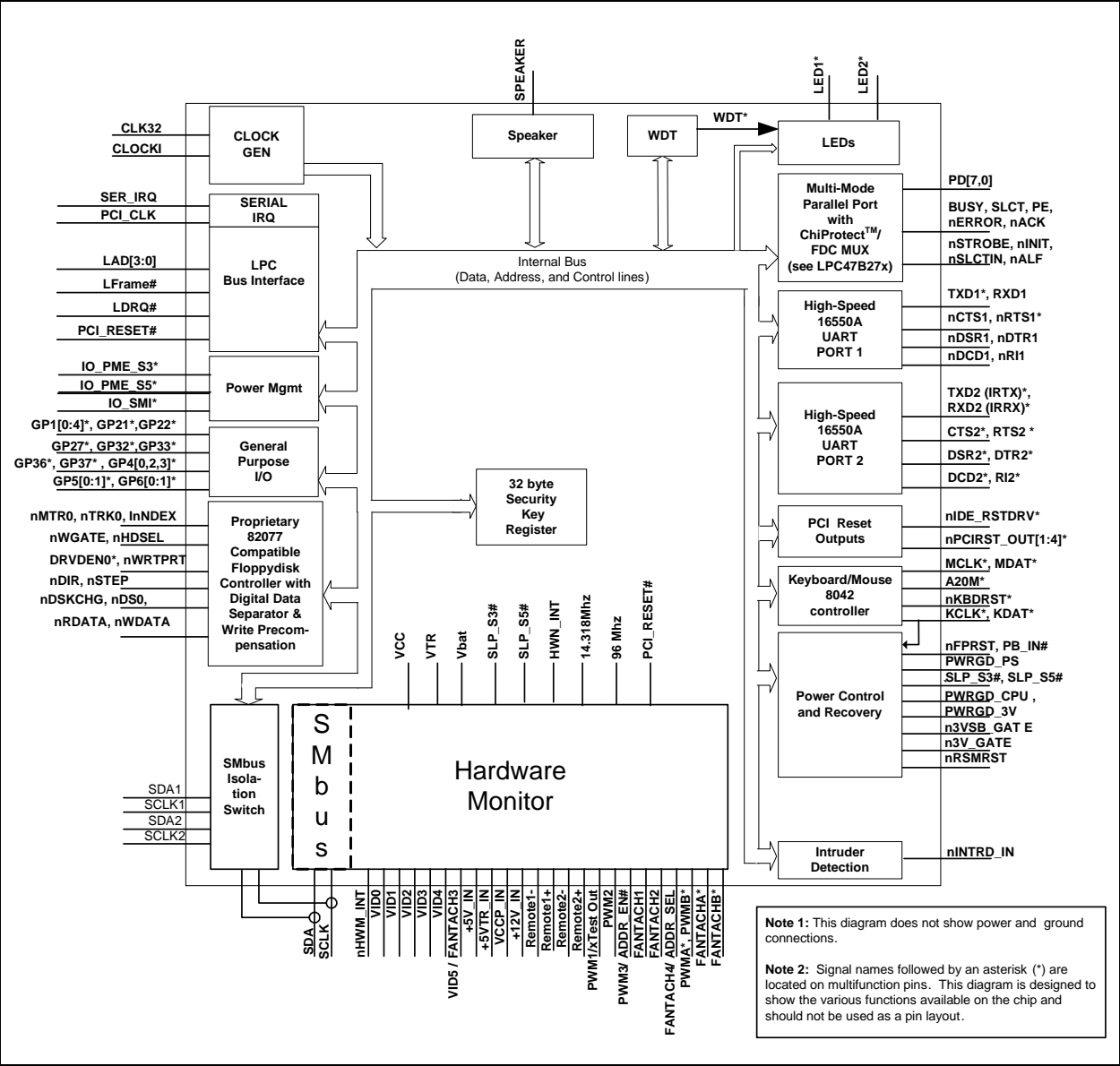
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SCH5017

BLOCK DIAGRAM

FIGURE 1: SCH5017 BLOCK DIAGRAM



APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001781A (06-20-14)	Replaces previous SMSC version Rev. 0.5 (05-24-07)	

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