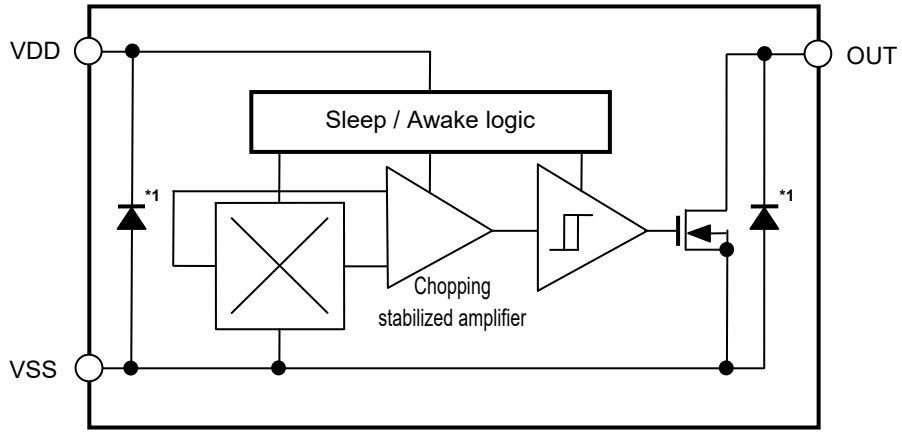
■ Block Diagrams

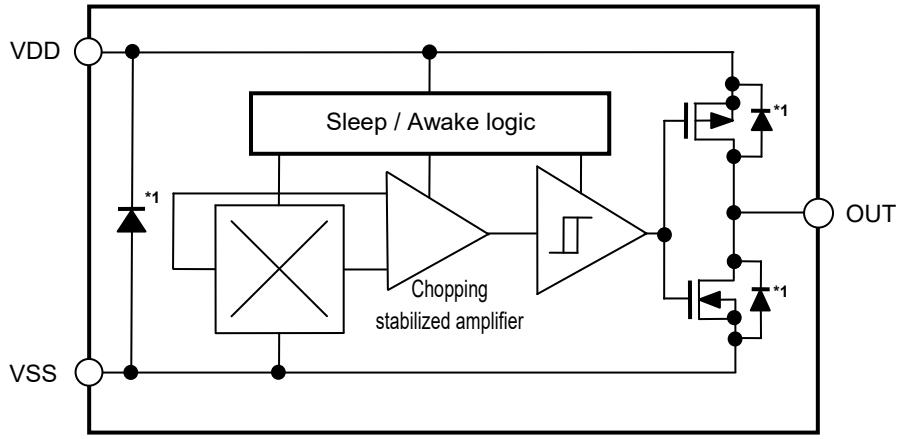
1. Nch open-drain output product



***1.** Parasitic diode

Figure 1

2. CMOS output product



***1.** Parasitic diode

Figure 2

■ Product Name Structure

1. Product name

S-5712 x x x x x - xxxx U

Environmental code
- U: Lead-free (Sn 100%), halogen-free

Package abbreviation and packing specifications*1
- M3T1: SOT-23-3, Tape
- I4T1: SNT-4A, Tape

Magnetic sensitivity
- 0: B_{OP} = 1.8 mT typ.
- 1: B_{OP} = 3.0 mT typ.
- 2: B_{OP} = 4.5 mT typ.
- 3: B_{OP} = 7.0 mT typ.

Output logic
- L: Active "L"
- H: Active "H"

Pole detection
- D: Detection of omnipolar
- S: Detection of S pole
- N: Detection of N pole

Output form
- N: Nch open-drain output
- C: CMOS output

Operating cycle
- A: t_{CYCLE} = 50.50 ms typ.
  (Product with omnipolar detection)
  t_{CYCLE} = 50.85 ms typ.
  (Product with S pole or N pole detection)
- B: t_{CYCLE} = 204.10 ms typ.
  (Product with omnipolar detection)
  t_{CYCLE} = 204.05 ms typ.
  (Product with S pole or N pole detection)
- C: t_{CYCLE} = 5.70 ms typ.
  (Product with omnipolar detection)
  t_{CYCLE} = 6.05 ms typ.
  (Product with S pole or N pole detection)

***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-3	MP003-C-P-SD	MP003-C-C-SD	MP003-Z-R-SD	–
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

3. Product name list

3. 1 SOT-23-3

3. 1. 1 Nch open-drain output product

Table 2

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B_{OP})
S-5712ANDL0-M3T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	1.8 mT typ.
S-5712ANDL1-M3T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	3.0 mT typ.
S-5712ANDL2-M3T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	4.5 mT typ.
S-5712ANSL1-M3T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "L"	3.0 mT typ.
S-5712ANSL2-M3T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "L"	4.5 mT typ.
S-5712ANSH1-M3T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "H"	3.0 mT typ.
S-5712BNDL2-M3T1U	204.10 ms typ.	Nch open-drain output	Omnipolar	Active "L"	4.5 mT typ.
S-5712BNDH2-M3T1U	204.10 ms typ.	Nch open-drain output	Omnipolar	Active "H"	4.5 mT typ.

Remark Please contact our sales representatives for products other than the above.

3. 1. 2 CMOS output product

Table 3

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B_{OP})
S-5712ACDL0-M3T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	1.8 mT typ.
S-5712ACDL1-M3T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712ACDL2-M3T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	4.5 mT typ.
S-5712ACDH1-M3T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5712ACDH2-M3T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "H"	4.5 mT typ.
S-5712ACSL1-M3T1U	50.85 ms typ.	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5712ACSL2-M3T1U	50.85 ms typ.	CMOS output	S pole	Active "L"	4.5 mT typ.
S-5712ACNL1-M3T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	3.0 mT typ.
S-5712ACNL2-M3T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	4.5 mT typ.
S-5712BCDH2-M3T1U	204.10 ms typ.	CMOS output	Omnipolar	Active "H"	4.5 mT typ.
S-5712CCDL1-M3T1U	5.70 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712CCSL1-M3T1U	6.05 ms typ.	CMOS output	S pole	Active "L"	3.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

3. 2 SNT-4A

3. 2. 1 Nch open-drain output product

Table 4

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B_{OP})
S-5712ANDL0-I4T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	1.8 mT typ.
S-5712ANDL1-I4T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	3.0 mT typ.
S-5712ANDL2-I4T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	4.5 mT typ.
S-5712ANSL1-I4T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "L"	3.0 mT typ.
S-5712ANSL2-I4T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "L"	4.5 mT typ.
S-5712BNDL2-I4T1U	204.10 ms typ.	Nch open-drain output	Omnipolar	Active "L"	4.5 mT typ.
S-5712BNDH2-I4T1U	204.10 ms typ.	Nch open-drain output	Omnipolar	Active "H"	4.5 mT typ.
S-5712BNDH3-I4T1U	204.10 ms typ.	Nch open-drain output	Omnipolar	Active "H"	7.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

3. 2. 2 CMOS output product

Table 5

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B_{OP})
S-5712ACDL0-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	1.8 mT typ.
S-5712ACDL1-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712ACDL2-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	4.5 mT typ.
S-5712ACDL3-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	7.0 mT typ.
S-5712ACDH1-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5712ACDH2-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "H"	4.5 mT typ.
S-5712ACSL1-I4T1U	50.85 ms typ.	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5712ACSL2-I4T1U	50.85 ms typ.	CMOS output	S pole	Active "L"	4.5 mT typ.
S-5712ACSL3-I4T1U	50.85 ms typ.	CMOS output	S pole	Active "L"	7.0 mT typ.
S-5712ACSH1-I4T1U	50.85 ms typ.	CMOS output	S pole	Active "H"	3.0 mT typ.
S-5712ACSH2-I4T1U	50.85 ms typ.	CMOS output	S pole	Active "H"	4.5 mT typ.
S-5712ACNL1-I4T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	3.0 mT typ.
S-5712ACNL2-I4T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	4.5 mT typ.
S-5712ACNL3-I4T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	7.0 mT typ.
S-5712ACNH1-I4T1U	50.85 ms typ.	CMOS output	N pole	Active "H"	3.0 mT typ.
S-5712BCDL1-I4T1U	204.10 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712BCDL2-I4T1U	204.10 ms typ.	CMOS output	Omnipolar	Active "L"	4.5 mT typ.
S-5712BCDH1-I4T1U	204.10 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5712BCDH2-I4T1U	204.10 ms typ.	CMOS output	Omnipolar	Active "H"	4.5 mT typ.
S-5712BCSL2-I4T1U	204.05 ms typ.	CMOS output	S pole	Active "L"	4.5 mT typ.
S-5712CCDL1-I4T1U	5.70 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712CCDL2-I4T1U	5.70 ms typ.	CMOS output	Omnipolar	Active "L"	4.5 mT typ.
S-5712CCDH1-I4T1U	5.70 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5712CCSL1-I4T1U	6.05 ms typ.	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5712CCNL1-I4T1U	6.05 ms typ.	CMOS output	N pole	Active "L"	3.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

■ Pin Configurations

1. SOT-23-3

Top view

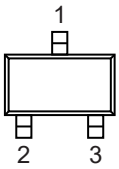


Figure 3

Table 6

Pin No.	Symbol	Pin Description
1	VSS	GND pin
2	VDD	Power supply pin
3	OUT	Output pin

2. SNT-4A

Top view

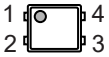


Figure 4

Table 7

Pin No.	Symbol	Pin Description
1	VDD	Power supply pin
2	VSS	GND pin
3	NC*1	No connection
4	OUT	Output pin

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 8

(Ta = +25°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD}	V_{SS} – 0.3 to V_{SS} + 7.0	V
Output current		I_{OUT}	±1.0	mA
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} – 0.3 to V_{SS} + 7.0	V
	CMOS output product		V_{SS} – 0.3 to V_{DD} + 0.3	V
Operation ambient temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 9

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SOT-23-3	Board A	–	200	–	°C/W
			Board B	–	165	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		SNT-4A	Board A	–	300	–	°C/W
			Board B	–	242	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Product with omnipolar detection

1. 1 S-5712AxDxx

Table 10

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	2.0	4.0	µA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	µA	4
Awake mode time	t_{AW}	–		–	0.10	–	ms	–
Sleep mode time	t_{SL}	–		–	50.40	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	50.50	100.00	ms	–

1. 2 S-5712BxDxx

Table 11

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	1.0	2.0	µA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	µA	4
Awake mode time	t_{AW}	–		–	0.10	–	ms	–
Sleep mode time	t_{SL}	–		–	204.00	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	204.10	400.00	ms	–

1. 3 S-5712CxDxx

Table 12

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	12.0	22.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.10	–	ms	–
Sleep mode time	t_{SL}	–		–	5.60	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	5.70	12.00	ms	–

2. Product with S pole or N pole detection

2. 1 S-5712AxSxx, S-5712AxNxx

Table 13

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	1.4	3.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	50.80	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	50.85	100.00	ms	–

2. 2 S-5712BxSxx, S-5712BxNxx

Table 14

($Ta = +25°C$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	1.0	2.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, $I_{OUT} = 0.5$ mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, $I_{OUT} = 0.5$ mA	–	–	0.4	V	2
			Output transistor Pch, $I_{OUT} = -0.5$ mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, $V_{OUT} = 3.5$ V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	204.00	–	ms	–
Operating cycle	t_{CYCLE}	$t_{AW} + t_{SL}$		–	204.05	400.00	ms	–

2. 3 S-5712CxSxx, S-5712CxNxx

Table 15

($Ta = +25°C$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	6.0	11.0	μA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, $I_{OUT} = 0.5$ mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, $I_{OUT} = 0.5$ mA	–	–	0.4	V	2
			Output transistor Pch, $I_{OUT} = -0.5$ mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, $V_{OUT} = 3.5$ V		–	–	1	μA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	6.00	–	ms	–
Operating cycle	t_{CYCLE}	$t_{AW} + t_{SL}$		–	6.05	12.00	ms	–

■ Magnetic Characteristics

1. Product with omnipolar detection

1. 1 Product with B_{OP} = 1.8 mT typ.

Table 16

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	0.6	1.8	3.0	mT	5
	N pole	B_{OPN}	–	–3.0	–1.8	–0.6	mT	5
Release point*2	S pole	B_{RPS}	–	0.1	1.1	2.4	mT	5
	N pole	B_{RPN}	–	–2.4	–1.1	–0.1	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.7	–	mT	5
	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	0.7	–	mT	5

1. 2 Product with B_{OP} = 3.0 mT typ.

Table 17

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	1.4	3.0	4.0	mT	5
	N pole	B_{OPN}	–	–4.0	–3.0	–1.4	mT	5
Release point*2	S pole	B_{RPS}	–	1.1	2.2	3.7	mT	5
	N pole	B_{RPN}	–	–3.7	–2.2	–1.1	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.8	–	mT	5
	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	0.8	–	mT	5

1. 3 Product with B_{OP} = 4.5 mT typ.

Table 18

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	2.5	4.5	6.0	mT	5
	N pole	B_{OPN}	–	–6.0	–4.5	–2.5	mT	5
Release point*2	S pole	B_{RPS}	–	2.0	3.5	5.5	mT	5
	N pole	B_{RPN}	–	–5.5	–3.5	–2.0	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.0	–	mT	5
	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	1.0	–	mT	5

1. 4 Product with B_{OP} = 7.0 mT typ.

Table 19

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	5.0	7.0	8.5	mT	5
	N pole	B_{OPN}	–	–8.5	–7.0	–5.0	mT	5
Release point*2	S pole	B_{RPS}	–	3.7	5.2	7.2	mT	5
	N pole	B_{RPN}	–	–7.2	–5.2	–3.7	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.8	–	mT	5
	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	1.8	–	mT	5

2. Product with S pole detection

2. 1 Product with B_{OP} = 1.8 mT typ.

Table 20

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	0.6	1.8	3.0	mT	5
Release point*2	S pole	B_{RPS}	–	0.1	1.1	2.4	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.7	–	mT	5

2. 2 Product with B_{OP} = 3.0 mT typ.

Table 21

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	1.4	3.0	4.0	mT	5
Release point*2	S pole	B_{RPS}	–	1.1	2.2	3.7	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.8	–	mT	5

2. 3 Product with B_{OP} = 4.5 mT typ.

Table 22

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	2.5	4.5	6.0	mT	5
Release point*2	S pole	B_{RPS}	–	2.0	3.5	5.5	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.0	–	mT	5

2. 4 Product with B_{OP} = 7.0 mT typ.

Table 23

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	5.0	7.0	8.5	mT	5
Release point*2	S pole	B_{RPS}	–	3.7	5.2	7.2	mT	5
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.8	–	mT	5

3. Product with N pole detection

3. 1 Product with B_{OP} = 1.8 mT typ.

Table 24

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	N pole	B_{OPN}	–	–3.0	–1.8	–0.6	mT	5
Release point*2	N pole	B_{RPN}	–	–2.4	–1.1	–0.1	mT	5
Hysteresis width*3	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	0.7	–	mT	5

3. 2 Product with B_{OP} = 3.0 mT typ.

Table 25

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	N pole	B_{OPN}	–	–4.0	–3.0	–1.4	mT	5
Release point*2	N pole	B_{RPN}	–	–3.7	–2.2	–1.1	mT	5
Hysteresis width*3	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	0.8	–	mT	5

3. 3 Product with B_{OP} = 4.5 mT typ.

Table 26

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	N pole	B_{OPN}	–	–6.0	–4.5	–2.5	mT	5
Release point*2	N pole	B_{RPN}	–	–5.5	–3.5	–2.0	mT	5
Hysteresis width*3	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	1.0	–	mT	5

3. 4 Product with B_{OP} = 7.0 mT typ.

Table 27

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	N pole	B_{OPN}	–	–8.5	–7.0	–5.0	mT	5
Release point*2	N pole	B_{RPN}	–	–7.2	–5.2	–3.7	mT	5
Hysteresis width*3	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	1.8	–	mT	5

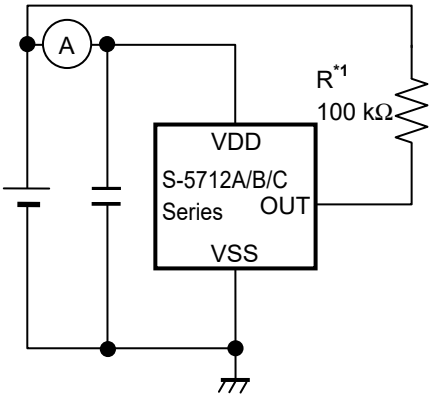
***1.** B_{OPN}, B_{OPS}: Operation points
B_{OPN} and B_{OPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is increased (by moving the magnet closer).
Even when the magnetic flux density exceeds B_{OPN} or B_{OPS}, V_{OUT} retains the status.

***2.** B_{RPN}, B_{RPS}: Release points
B_{RPN} and B_{RPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is decreased (the magnet is moved further away).
Even when the magnetic flux density falls below B_{RPN} or B_{RPS}, V_{OUT} retains the status.

***3.** B_{HYSN}, B_{HYSS}: Hysteresis widths
B_{HYSN} and B_{HYSS} are the difference between B_{OPN} and B_{RPN}, and B_{OPS} and B_{RPS}, respectively.

Remark The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

■ Test Circuits



***1.** Resistor (R) is unnecessary for the CMOS output product.

Figure 5 Test Circuit 1

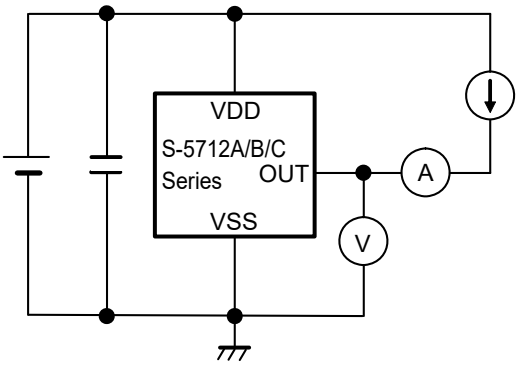


Figure 6 Test Circuit 2

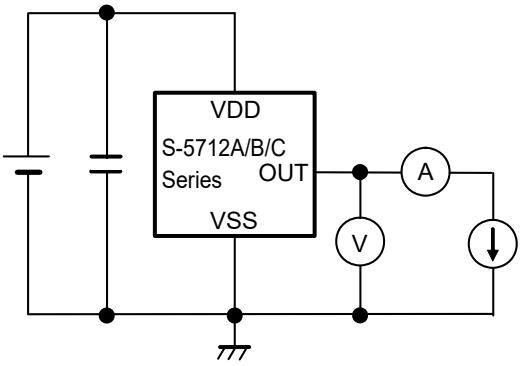


Figure 7 Test Circuit 3

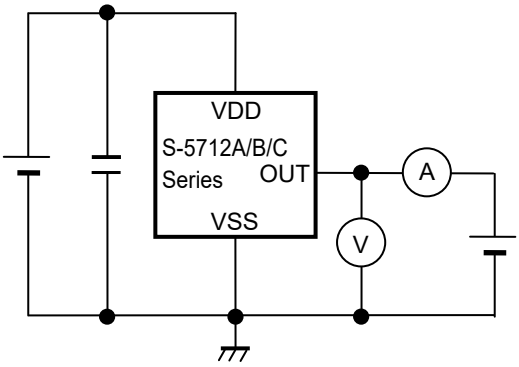
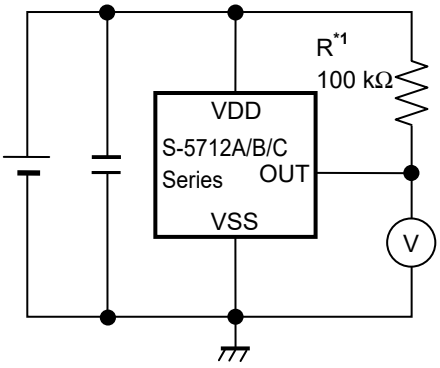


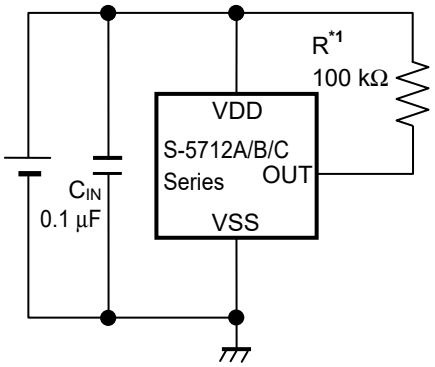
Figure 8 Test Circuit 4



***1.** Resistor (R) is unnecessary for the CMOS output product.

Figure 9 Test Circuit 5

■ Standard Circuit



***1.** Resistor (R) is unnecessary for the CMOS output product.

Figure 10

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Operation

1. Direction of applied magnetic flux

This IC detects the flux density which is vertical to the marking surface.
Figure 11 and **Figure 12** show the direction in which magnetic flux is being applied.

1. 1 SOT-23-3

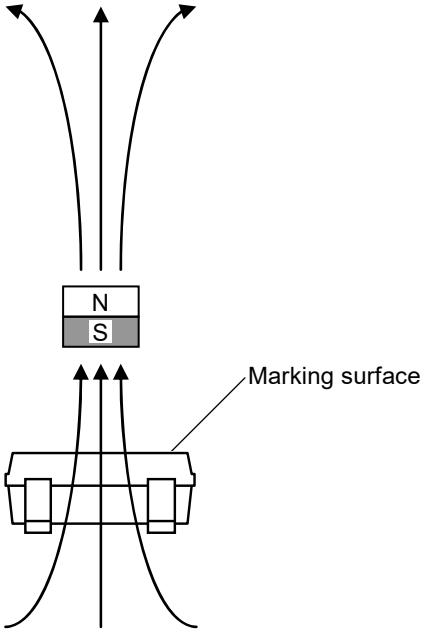


Figure 11

1. 2 SNT-4A

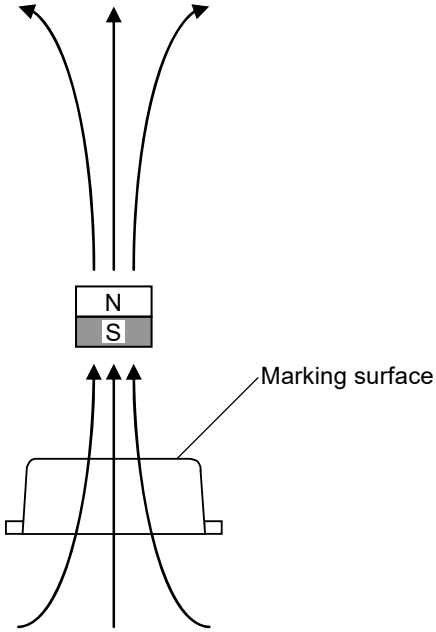


Figure 12

2. Position of Hall sensor

Figure 13 and **Figure 14** show the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

2. 1 SOT-23-3

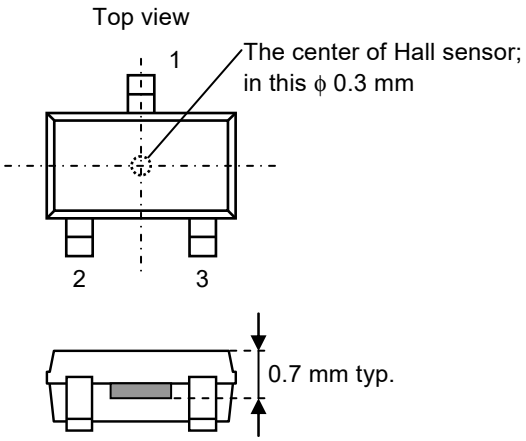


Figure 13

2. 2 SNT-4A

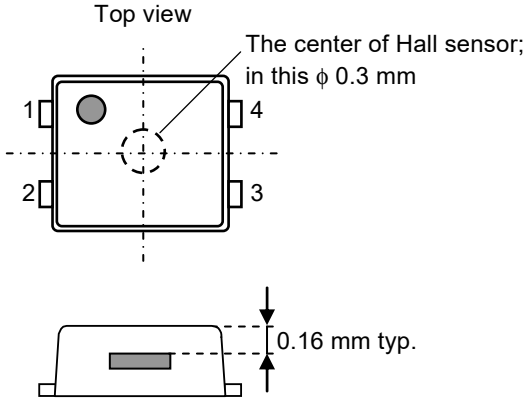


Figure 14

3. Basic operation

This IC changes the output voltage level (V_{OUT}) according to the level of the magnetic flux density (N pole or S pole) applied by a magnet.
The following explains the operation when the output logic is active "L".

3. 1 Product with omnipolar detection

When the magnetic flux density vertical to the marking surface exceeds the operation point (B_{OPN} or B_{OPS}) after the S pole or N pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "H" to "L". When the S pole or N pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than the release point (B_{RPN} or B_{RPS}), V_{OUT} changes from "L" to "H".
Figure 15 shows the relationship between the magnetic flux density and V_{OUT}.

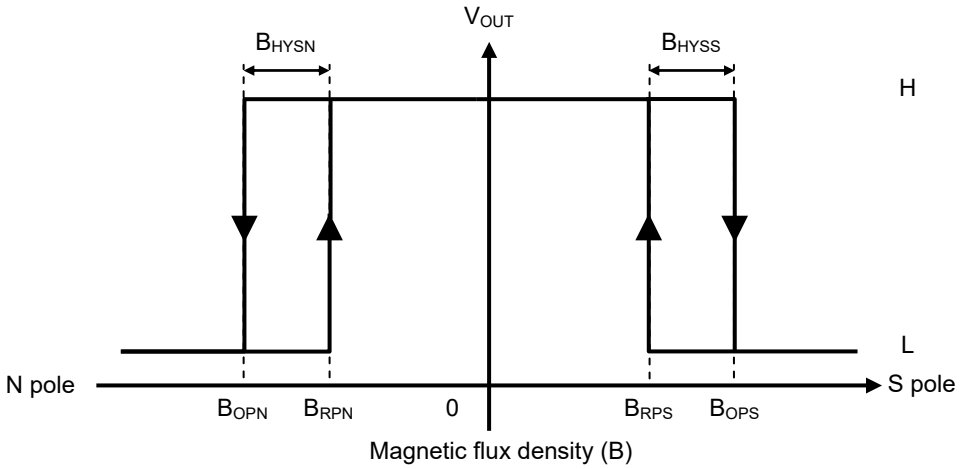


Figure 15

3. 2 Product with S pole detection

When the magnetic flux density vertical to the marking surface exceeds B_{OPS} after the S pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "H" to "L". When the S pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than B_{RPS}, V_{OUT} changes from "L" to "H".
Figure 16 shows the relationship between the magnetic flux density and V_{OUT}.

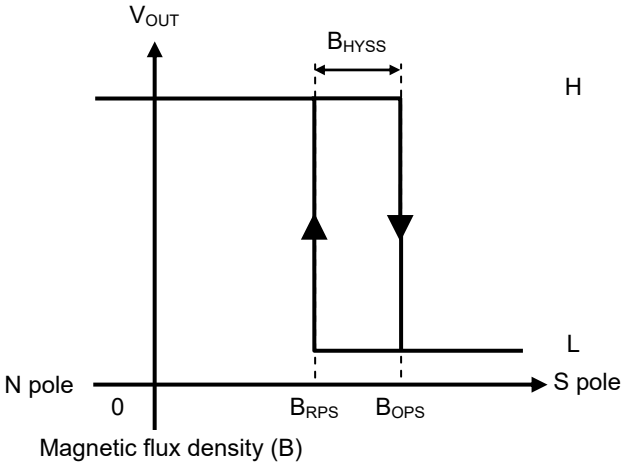


Figure 16

3. 3 Product with N pole detection

When the magnetic flux density vertical to the marking surface exceeds B_{OPN} after the N pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "H" to "L". When the N pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than B_{RPN}, V_{OUT} changes from "L" to "H".

Figure 17 shows the relationship between the magnetic flux density and V_{OUT}.

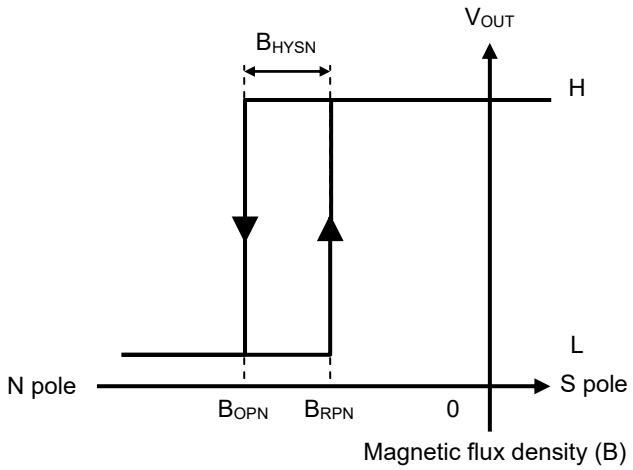


Figure 17

4. Time dependency in the current consumption

This IC performs the intermittent operation, and operates at low current consumption due to repeating the sleep mode (t_{SL}) and the awake mode (t_{AW}).
Figure 18 shows the time dependency in the current consumption.

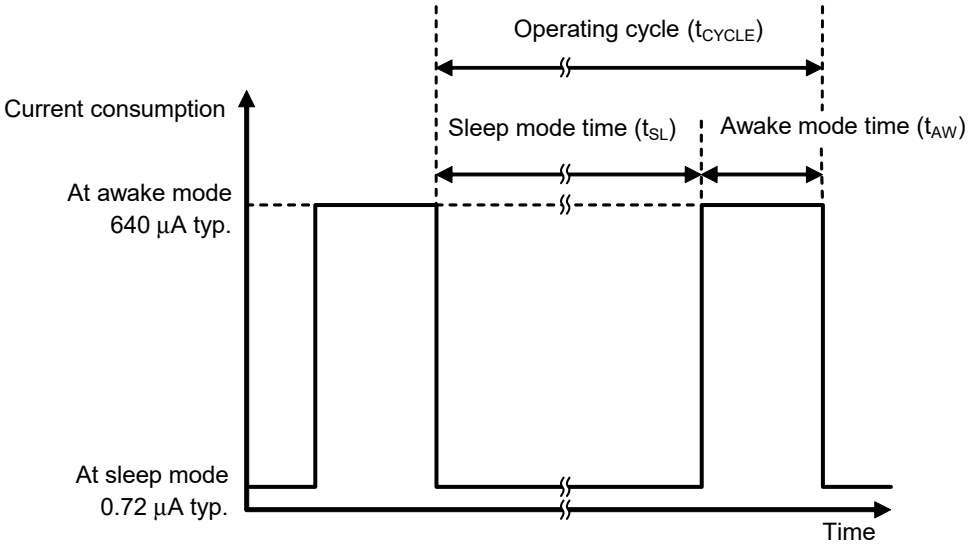


Figure 18

5. Timing chart

Figure 19 shows the operation timing of this IC.

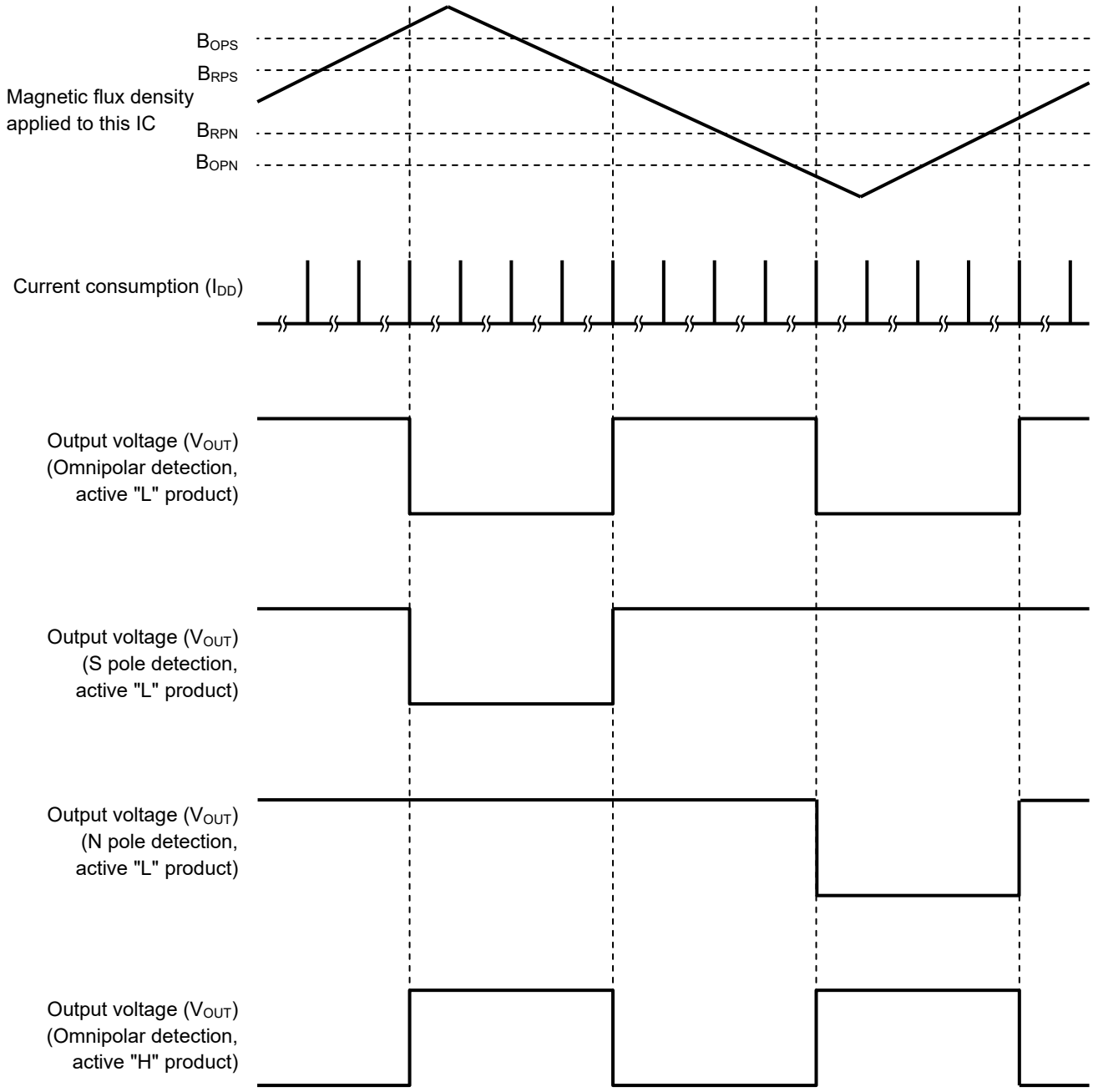


Figure 19

■ Precautions

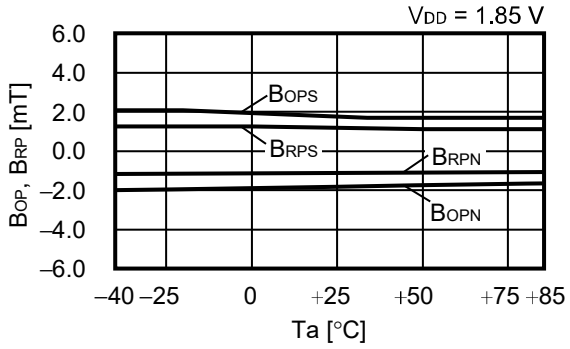
- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

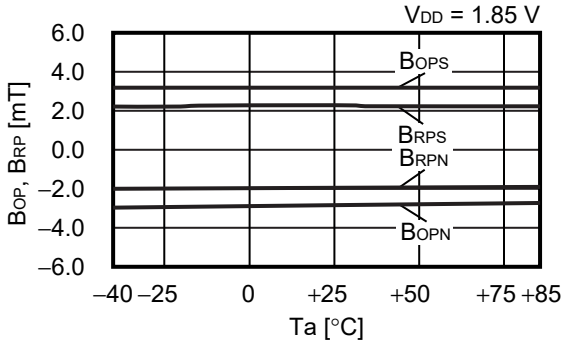
1. S-5712AxDxx

1. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

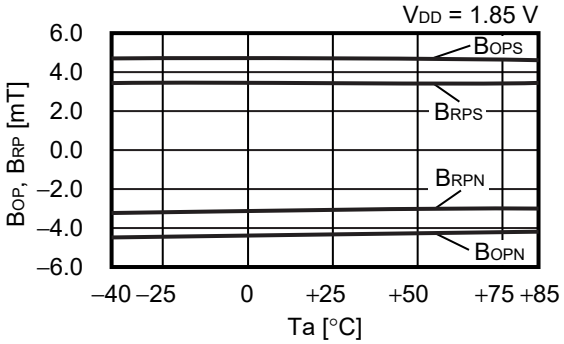
1. 1. 1 S-5712AxDx0



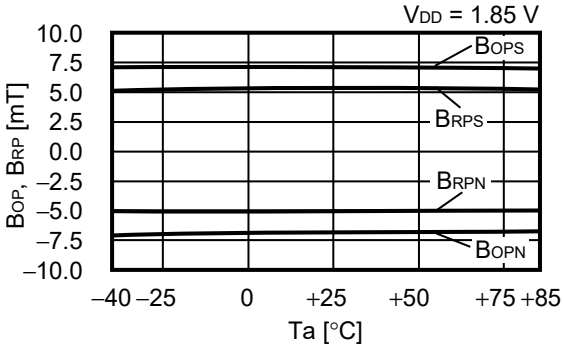
1. 1. 2 S-5712AxDx1



1. 1. 3 S-5712AxDx2

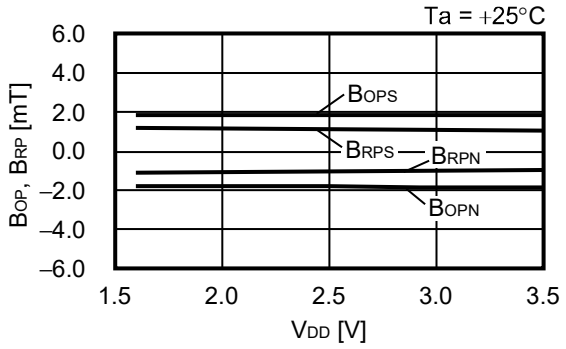


1. 1. 4 S-5712AxDx3

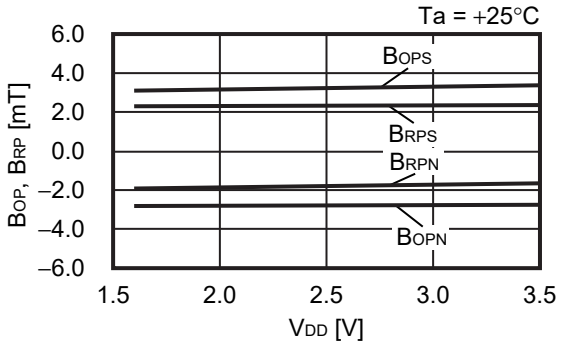


1. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

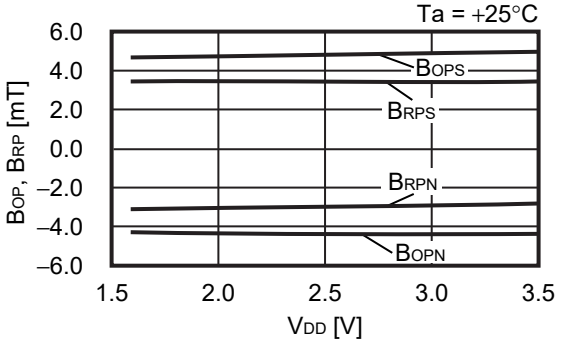
1. 2. 1 S-5712AxDx0



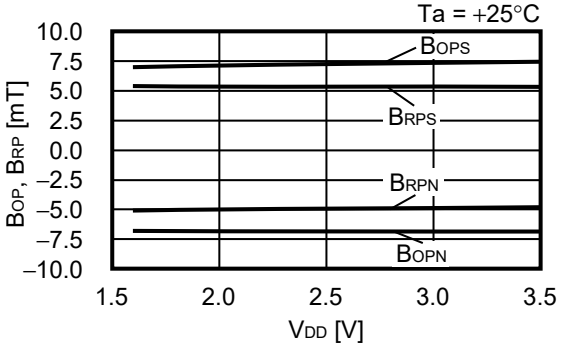
1. 2. 2 S-5712AxDx1



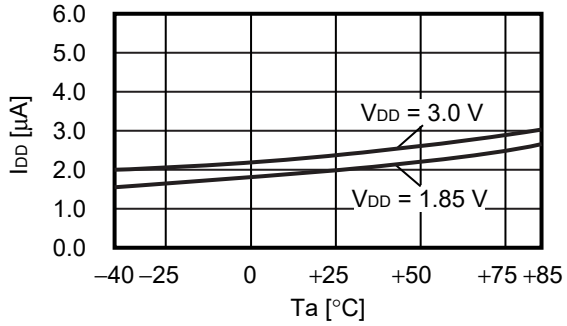
1. 2. 3 S-5712AxDx2



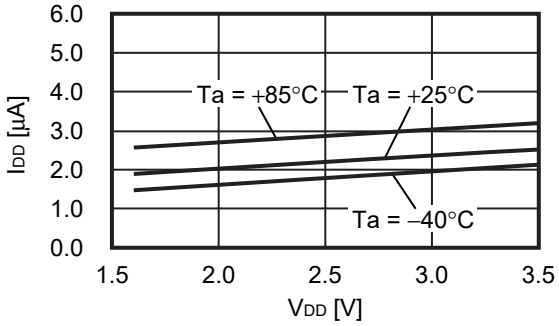
1. 2. 4 S-5712AxDx3



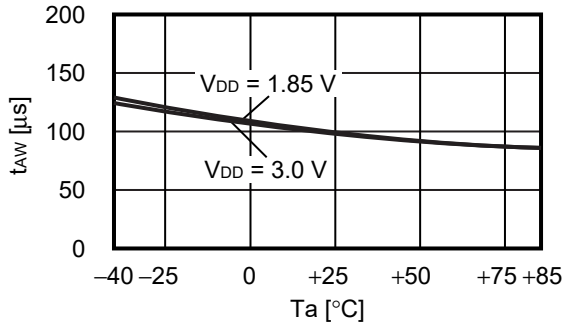
1. 3 Current consumption (I_{DD}) vs. Temperature (Ta)



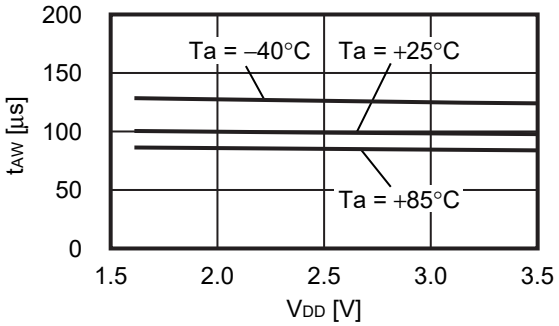
1. 4 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



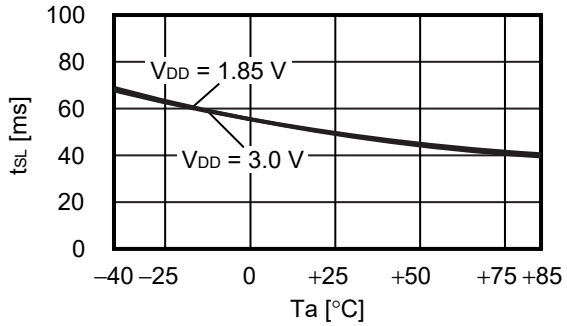
1. 5 Awake mode time (t_{AW}) vs. Temperature (Ta)



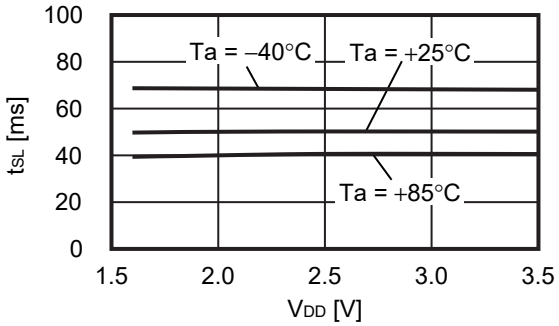
1. 6 Awake mode time (t_{AW}) vs. Power supply voltage (V_{DD})



1. 7 Sleep mode time (t_{SL}) vs. Temperature (Ta)



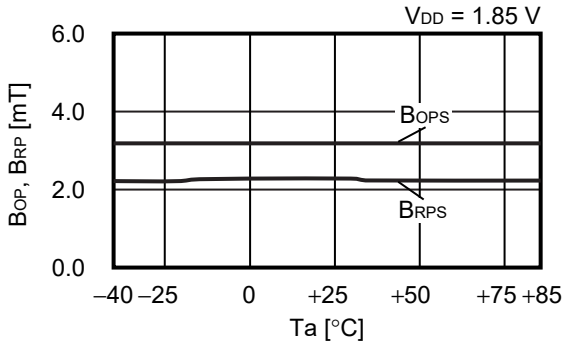
1. 8 Sleep mode time (t_{SL}) vs. Power supply voltage (V_{DD})



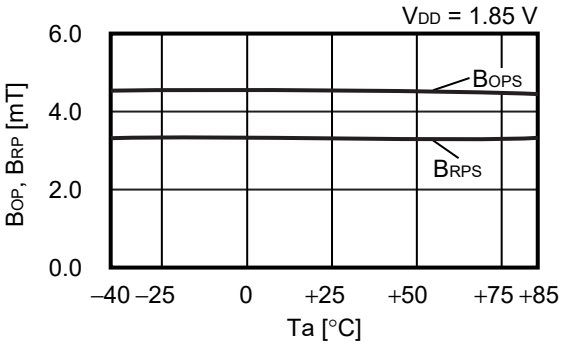
2. S-5712AxSxx, S-5712AxNxx

2. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

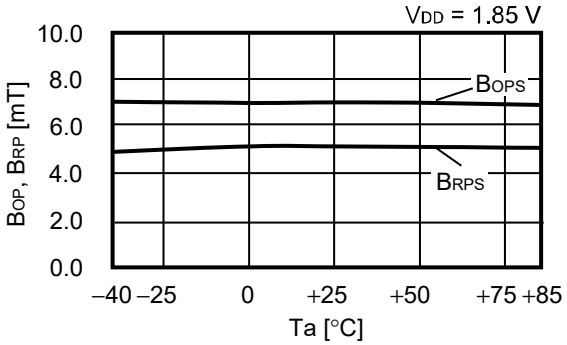
2. 1. 1 S-5712AxSx1



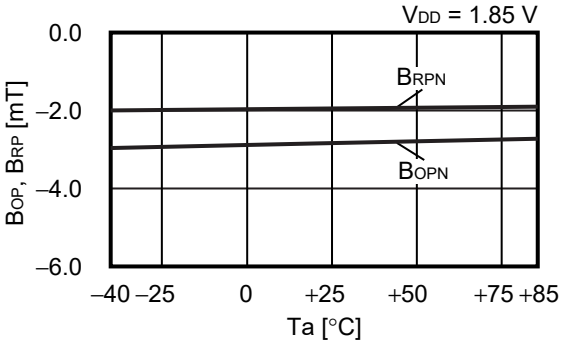
2. 1. 2 S-5712AxSx2



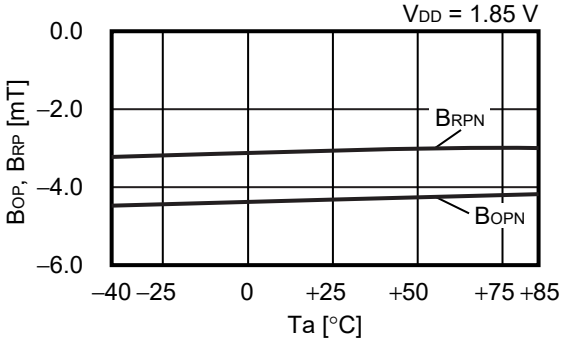
2. 1. 3 S-5712AxSx3



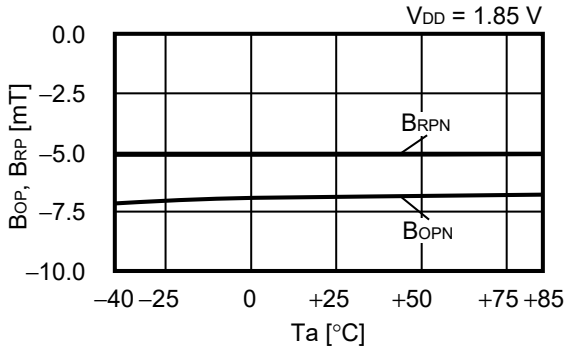
2. 1. 4 S-5712AxNx1



2. 1. 5 S-5712AxNx2

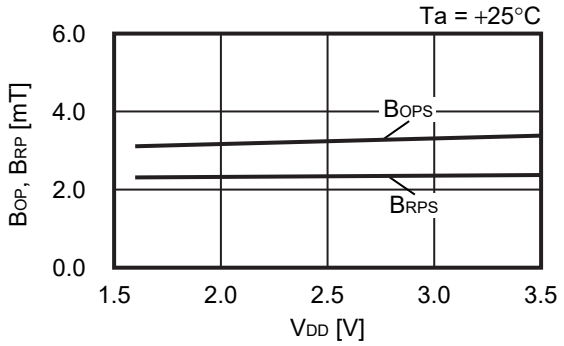


2. 1. 6 S-5712AxNx3

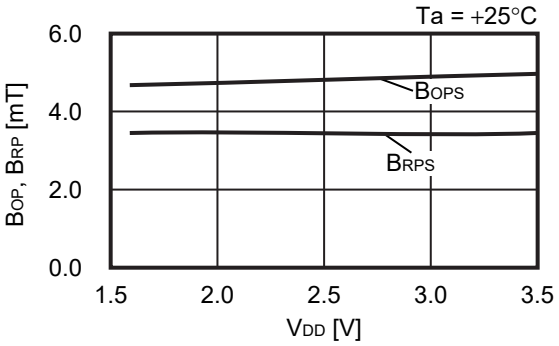


2. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

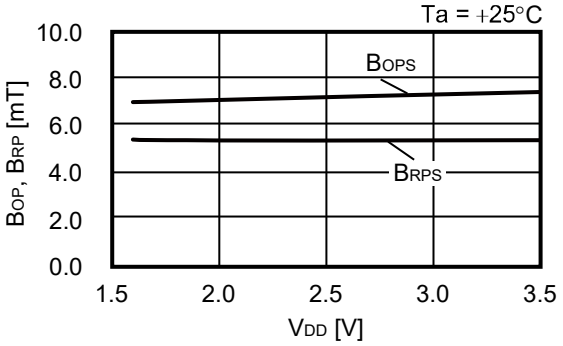
2. 2. 1 S-5712AxSx1



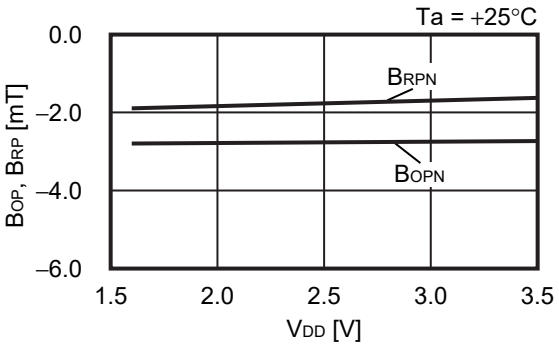
2. 2. 2 S-5712AxSx2



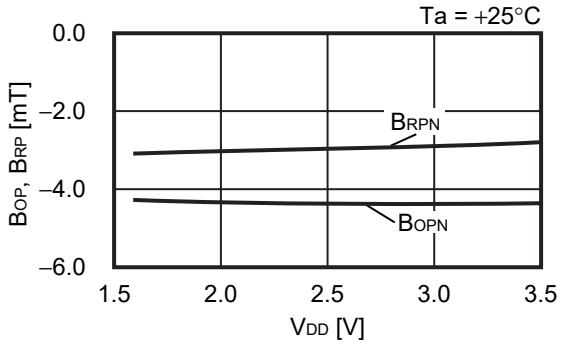
2. 2. 3 S-5712AxSx3



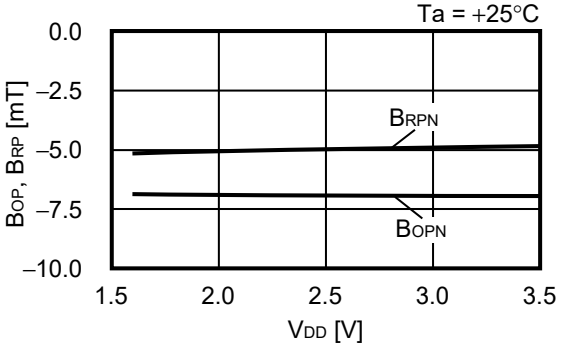
2. 2. 4 S-5712AxNx1



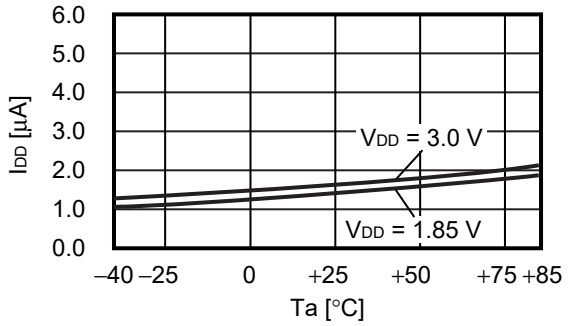
2. 2. 5 S-5712AxNx2



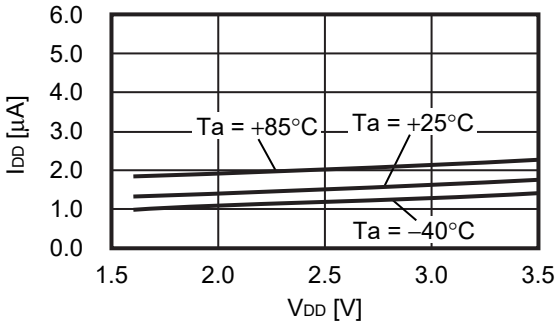
2. 2. 6 S-5712AxNx3



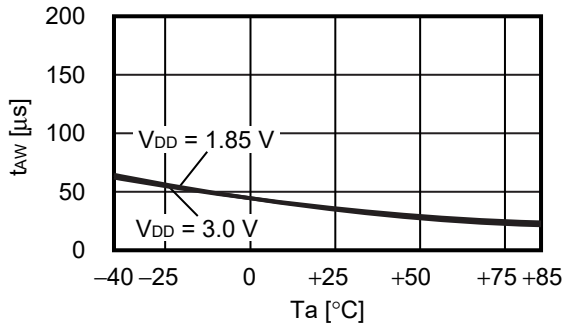
2. 3 Current consumption (I_{DD}) vs. Temperature (Ta)



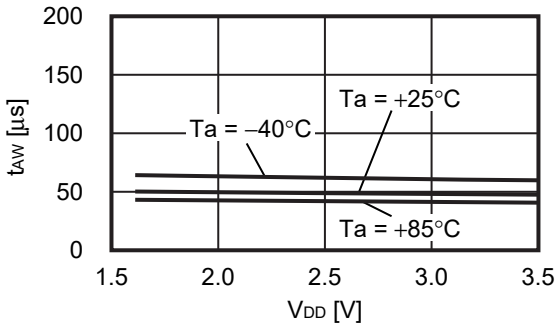
2. 4 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



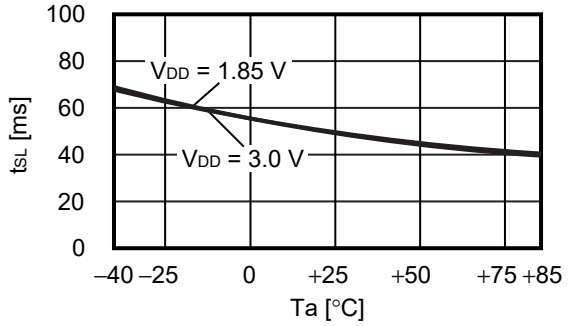
2. 5 Awake mode time (t_{AW}) vs. Temperature (Ta)



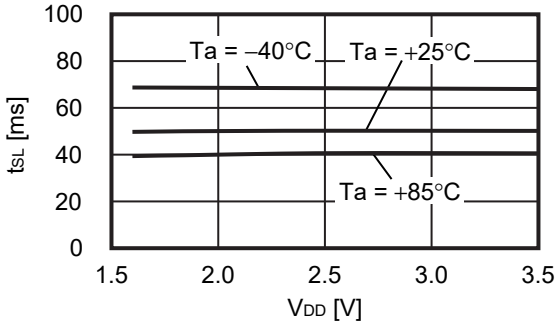
2. 6 Awake mode time (t_{AW}) vs. Power supply voltage (V_{DD})



2. 7 Sleep mode time (t_{SL}) vs. Temperature (Ta)



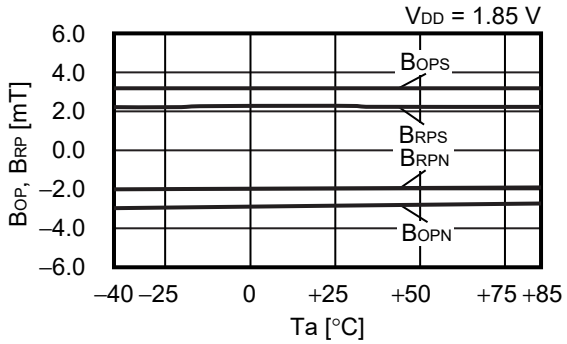
2. 8 Sleep mode time (t_{SL}) vs. Power supply voltage (V_{DD})



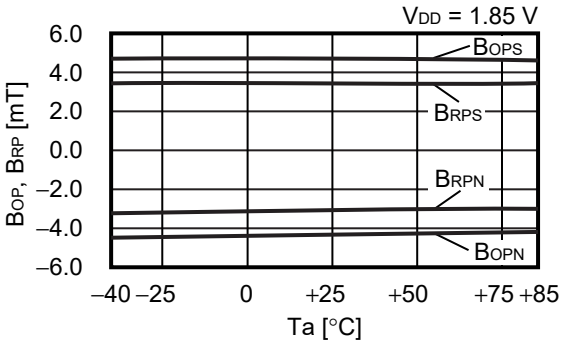
3. S-5712BxDxx

3. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

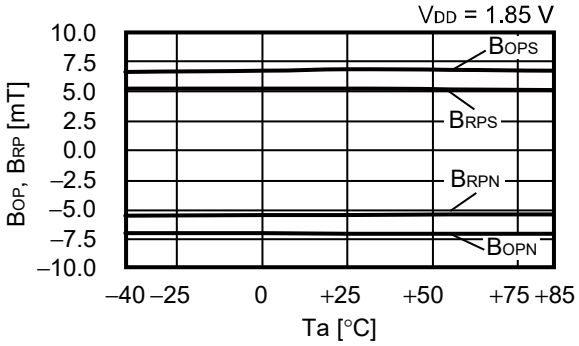
3. 1. 1 S-5712BxDx1



3. 1. 2 S-5712BxDx2

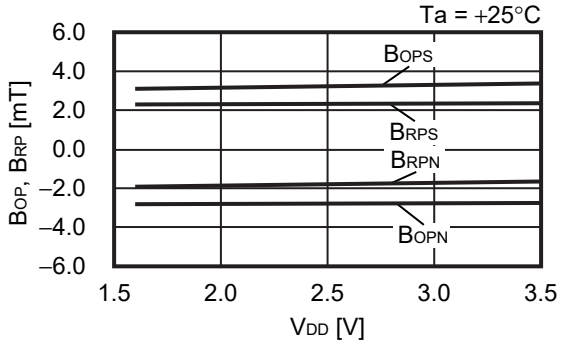


3. 1. 3 S-5712BxDx3

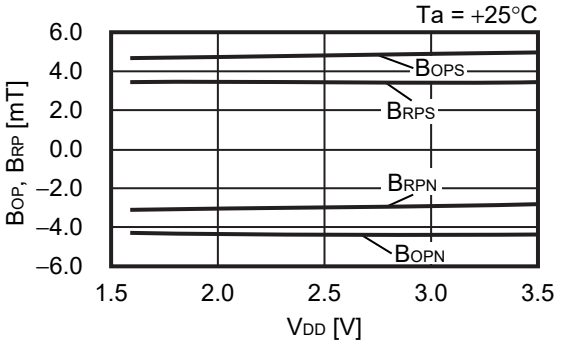


3. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

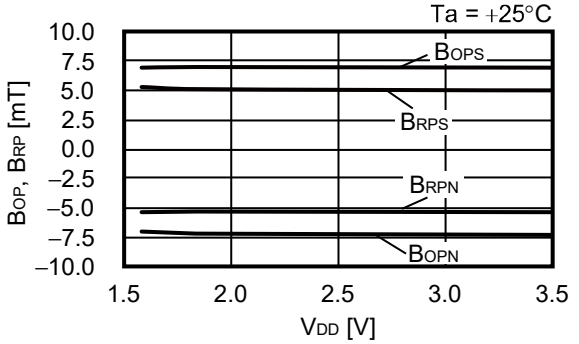
3. 2. 1 S-5712BxDx1



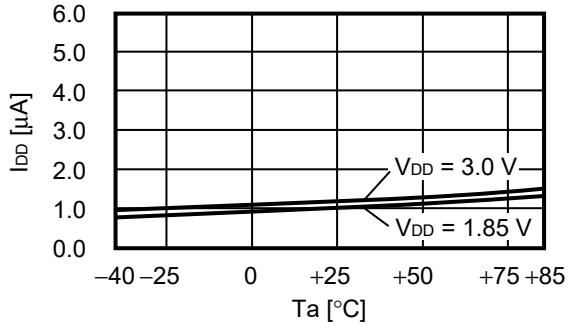
3. 2. 2 S-5712BxDx2



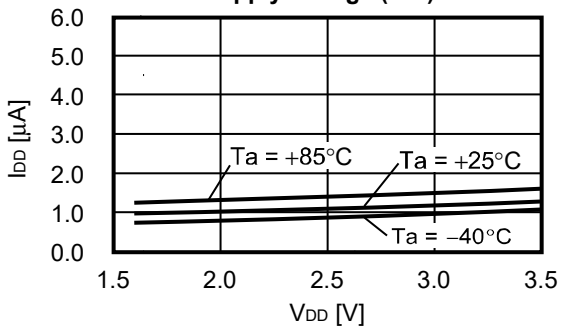
3. 2. 3 S-5712BxDx3



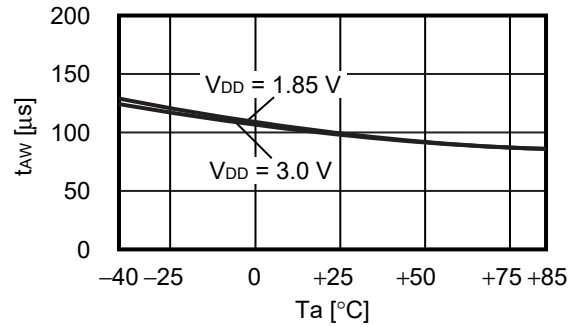
3. 3 Current consumption (I_{DD}) vs. Temperature (Ta)



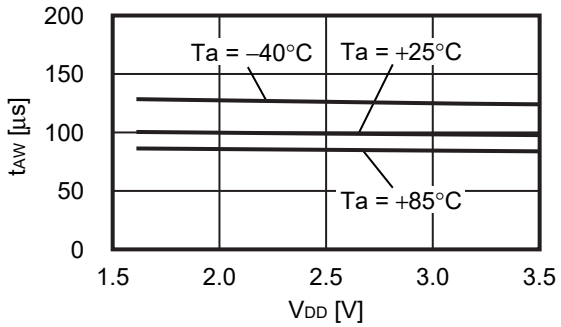
3. 4 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



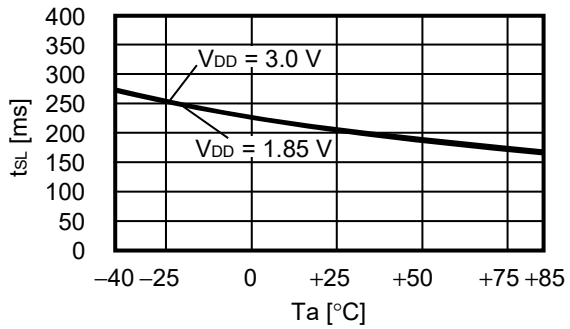
3. 5 Awake mode time (t_{AW}) vs. Temperature (Ta)



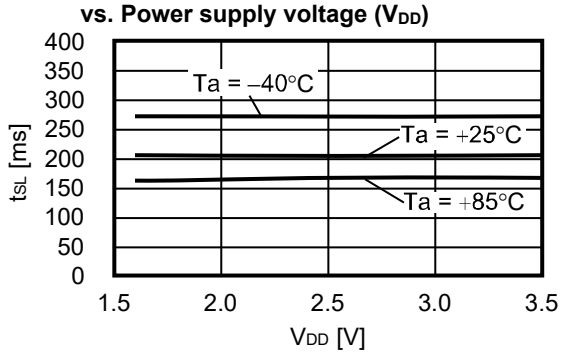
3. 6 Awake mode time (t_{AW}) vs. Power supply voltage (V_{DD})



3. 7 Sleep mode time (t_{SL}) vs. Temperature (Ta)



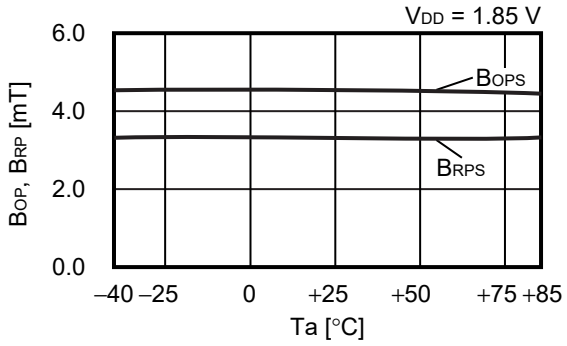
3. 8 Sleep mode time (t_{SL}) vs. Power supply voltage (V_{DD})



4. S-5712BxSxx, S-5712BxNxx

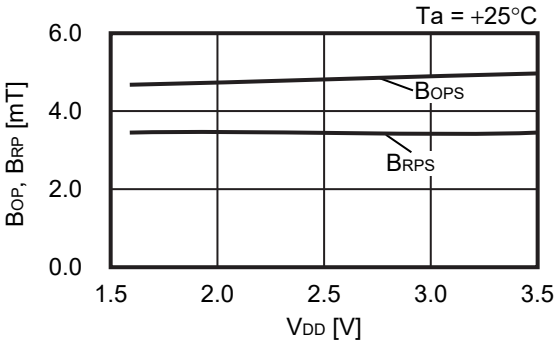
4. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

4. 1. 1 S-5712BxSx2

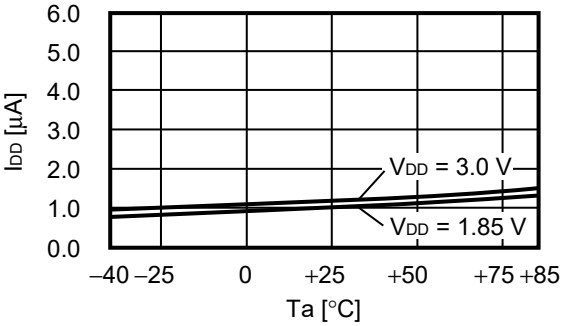


4. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

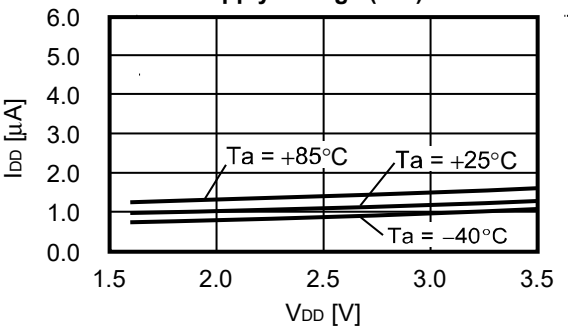
4. 2. 1 S-5712BxSx2



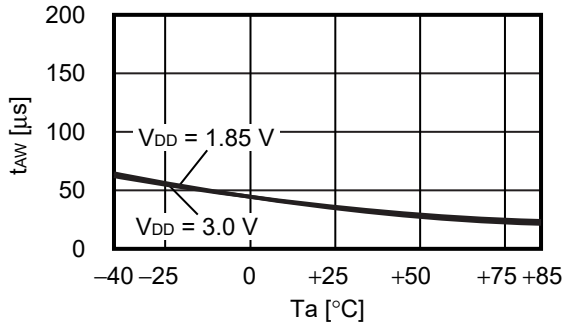
4. 3 Current consumption (I_{DD}) vs. Temperature (Ta)



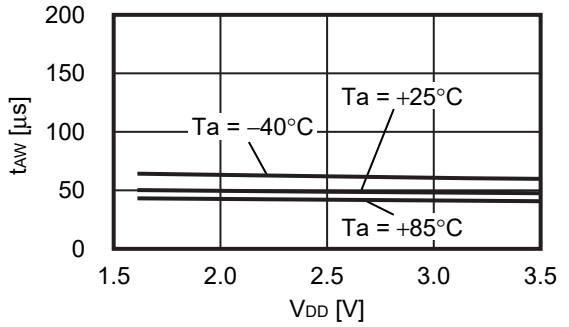
4. 4 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



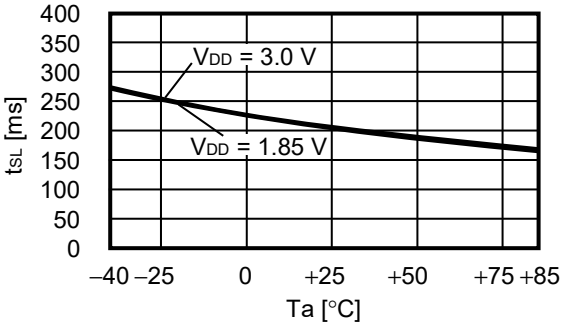
4. 5 Awake mode time (t_{AW}) vs. Temperature (Ta)



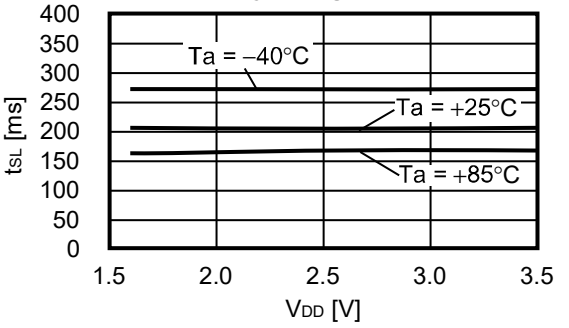
4. 6 Awake mode time (t_{AW}) vs. Power supply voltage (V_{DD})



4. 7 Sleep mode time (t_{SL}) vs. Temperature (Ta)



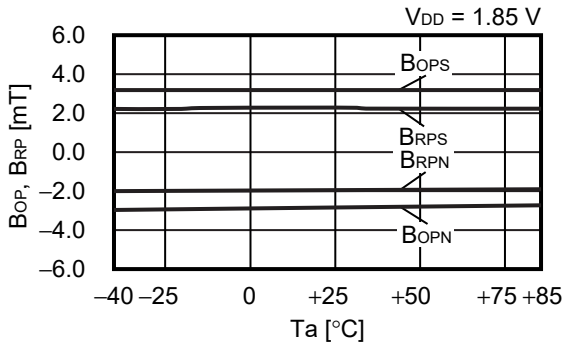
4. 8 Sleep mode time (t_{SL}) vs. Power supply voltage (V_{DD})



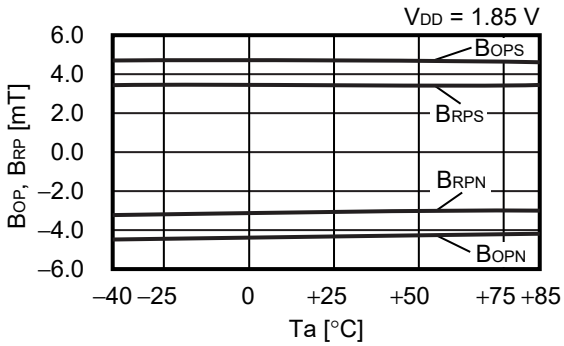
5. S-5712CxDxx

5. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

5. 1. 1 S-5712CxDx1

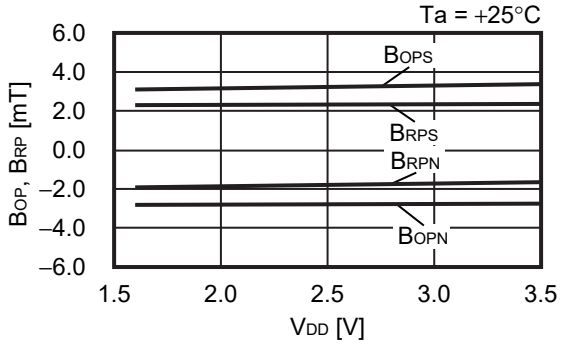


5. 1. 2 S-5712CxDx2

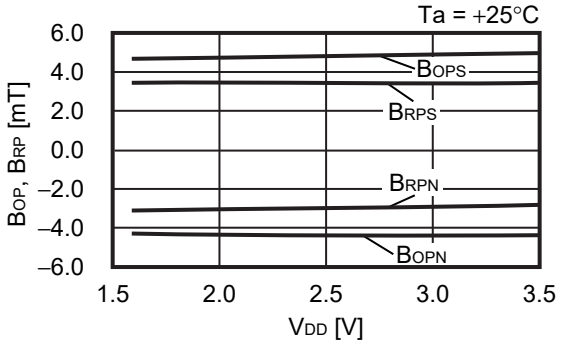


5. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

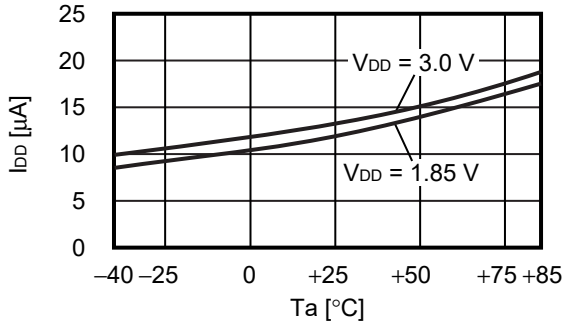
5. 2. 1 S-5712CxDx1



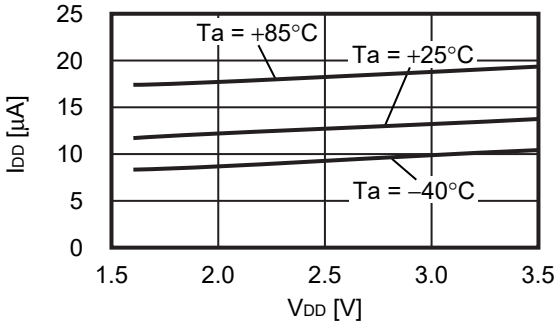
5. 2. 2 S-5712CxDx2



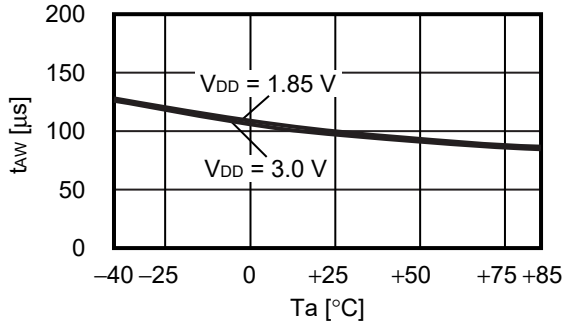
5. 3 Current consumption (I_{DD}) vs. Temperature (Ta)



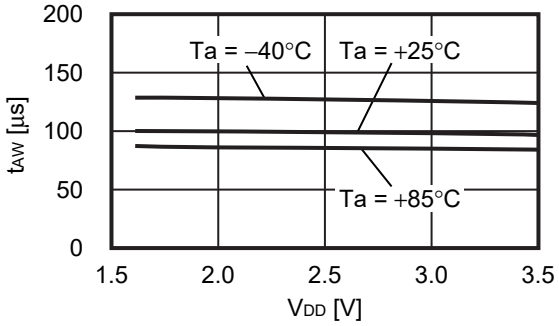
5. 4 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



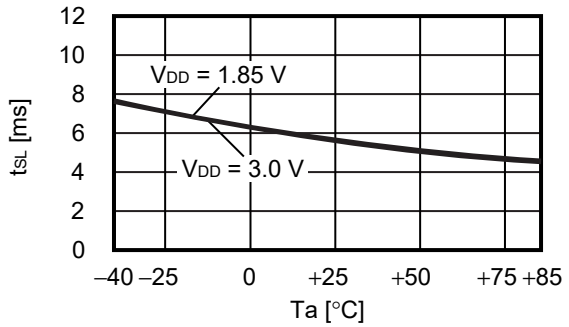
5. 5 Awake mode time (t_{AW}) vs. Temperature (Ta)



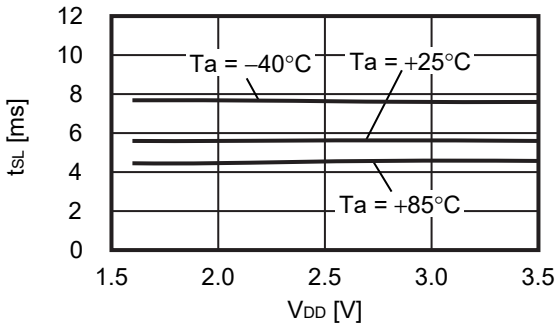
5. 6 Awake mode time (t_{AW}) vs. Power supply voltage (V_{DD})



5. 7 Sleep mode time (t_{SL}) vs. Temperature (Ta)



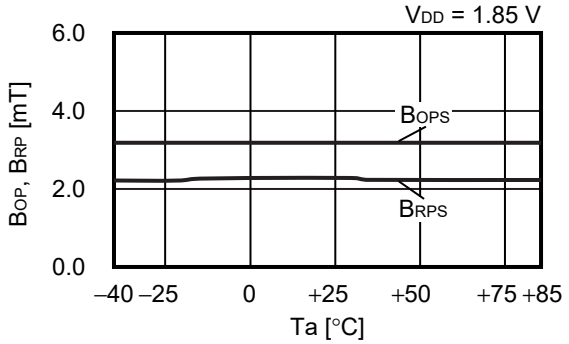
5. 8 Sleep mode time (t_{SL}) vs. Power supply voltage (V_{DD})



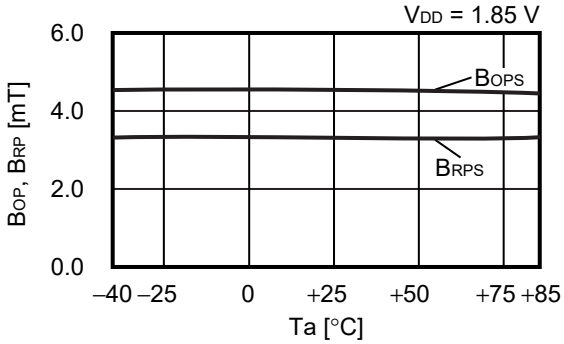
6. S-5712CxSxx, S-5712CxNxx

6. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

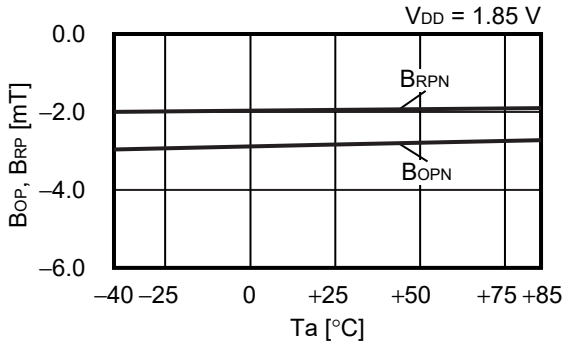
6. 1. 1 S-5712CxSx1



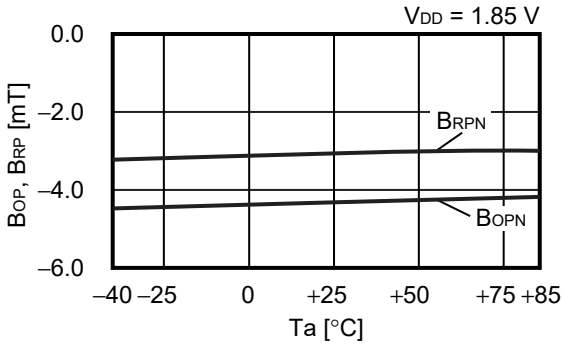
6. 1. 2 S-5712CxSx2



6. 1. 3 S-5712CxNx1

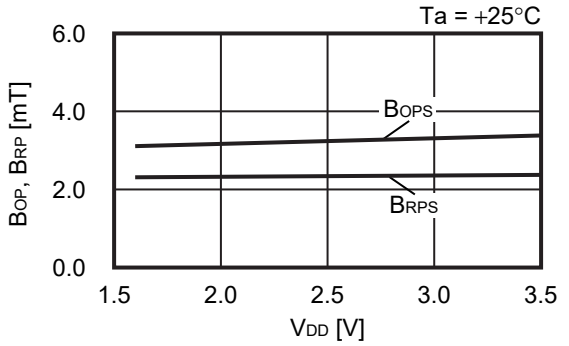


6. 1. 4 S-5712CxNx2

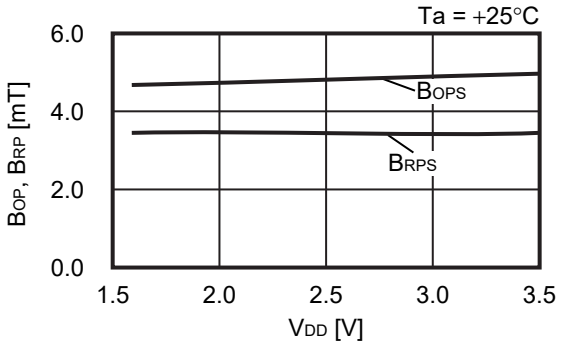


6. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

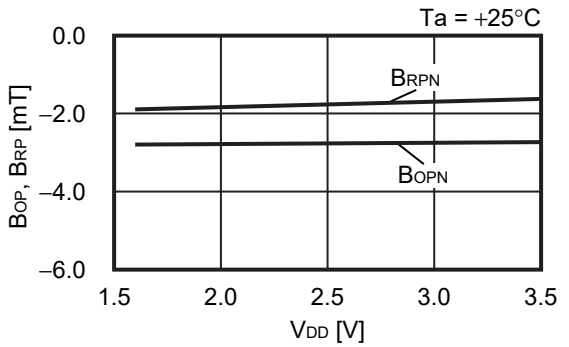
6. 2. 1 S-5712CxSx1



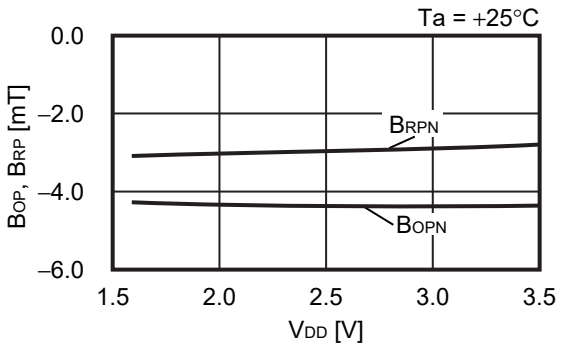
6. 2. 2 S-5712CxSx2



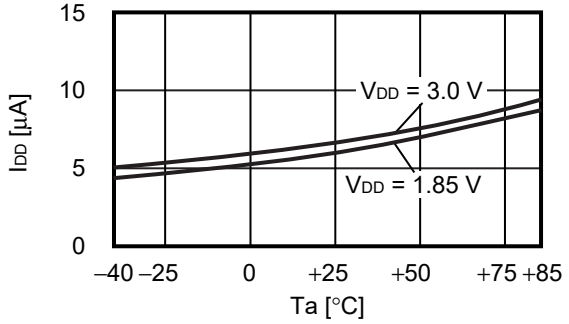
6. 2. 3 S-5712CxNx1



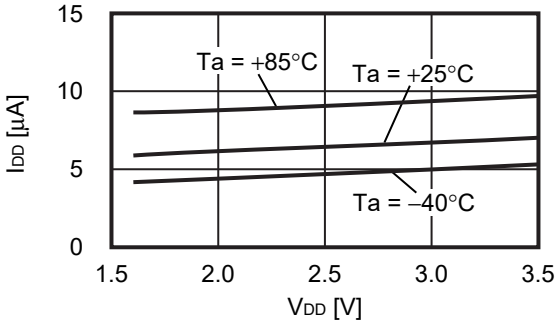
6. 2. 4 S-5712CxNx2



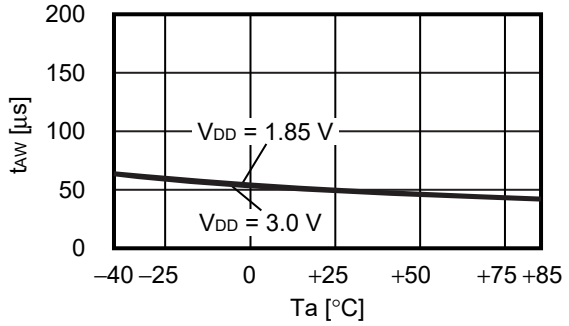
6. 3 Current consumption (I_{DD}) vs. Temperature (Ta)



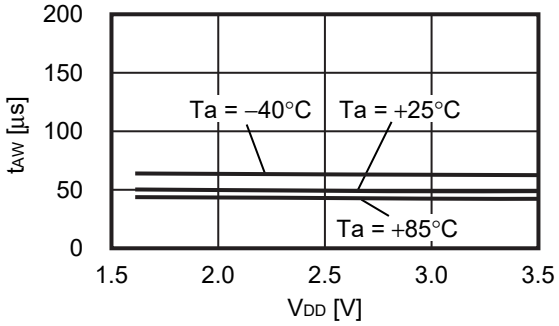
6. 4 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



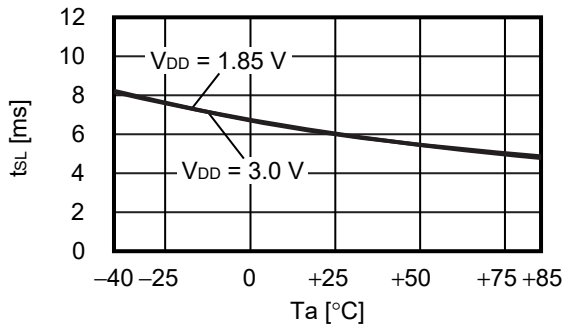
6. 5 Awake mode time (t_{AW}) vs. Temperature (Ta)



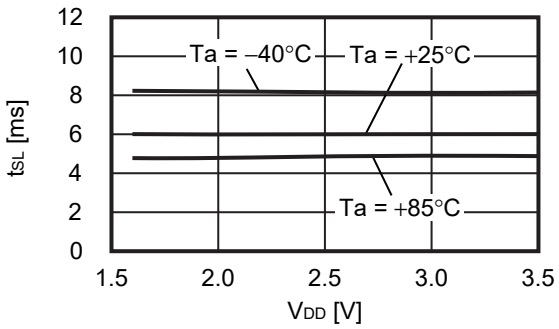
6. 6 Awake mode time (t_{AW}) vs. Power supply voltage (V_{DD})



6. 7 Sleep mode time (t_{SL}) vs. Temperature (Ta)

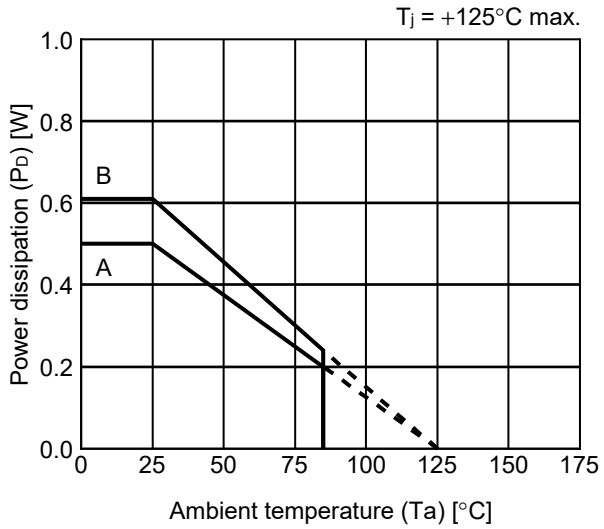


6. 8 Sleep mode time (t_{SL}) vs. Power supply voltage (V_{DD})



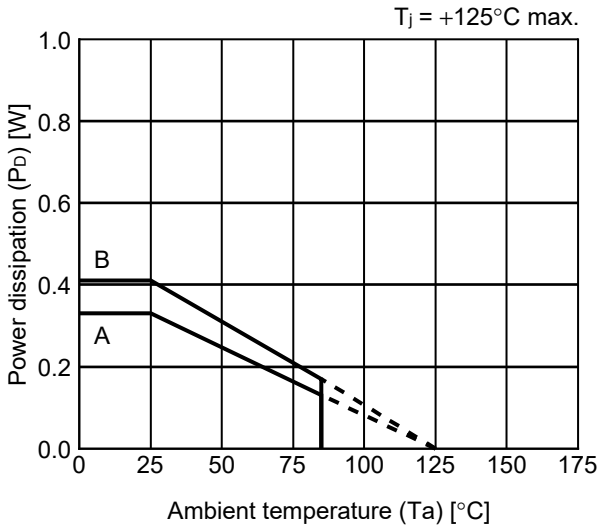
■ Power Dissipation

SOT-23-3



Board	Power Dissipation (P_D)
A	0.50 W
B	0.61 W
C	–
D	–
E	–

SNT-4A

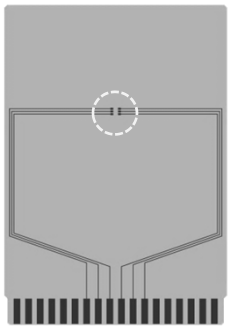


Board	Power Dissipation (P_D)
A	0.33 W
B	0.41 W
C	–
D	–
E	–

SOT-23-3/3S/5/6 Test Board

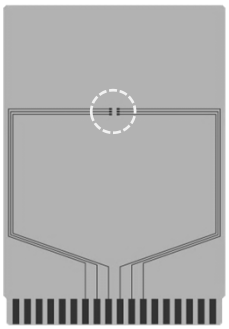
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



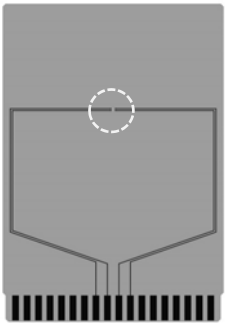
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SOT23x-A-Board-SD-2.0

SNT-4A Test Board

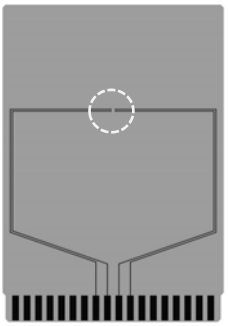
IC Mount Area

(1) Board A



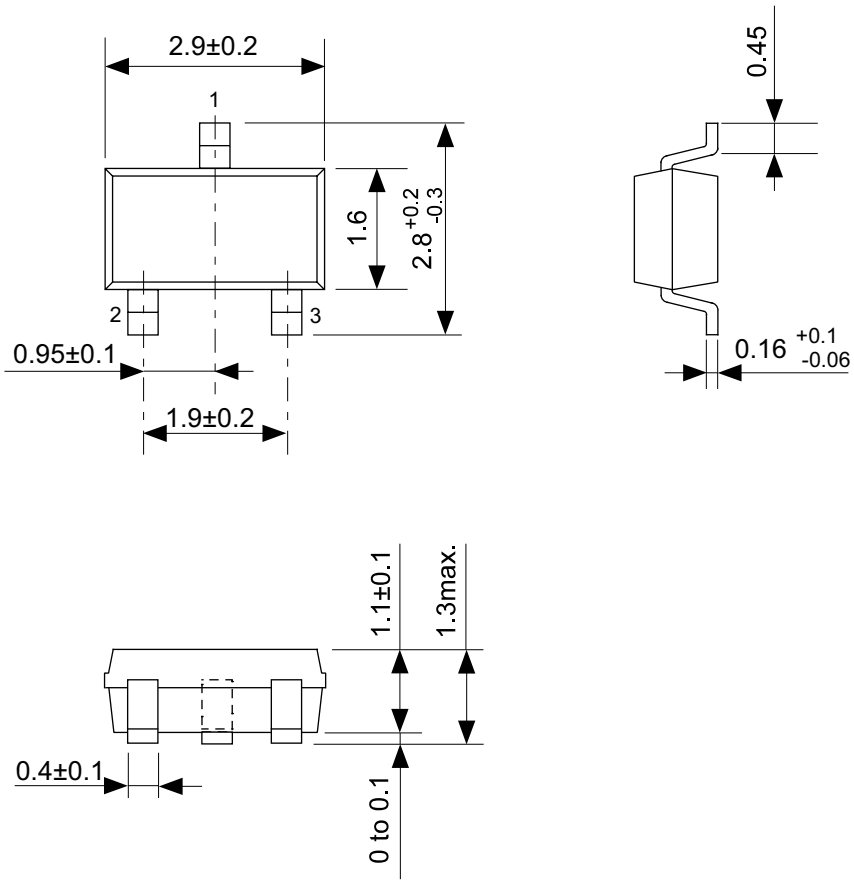
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



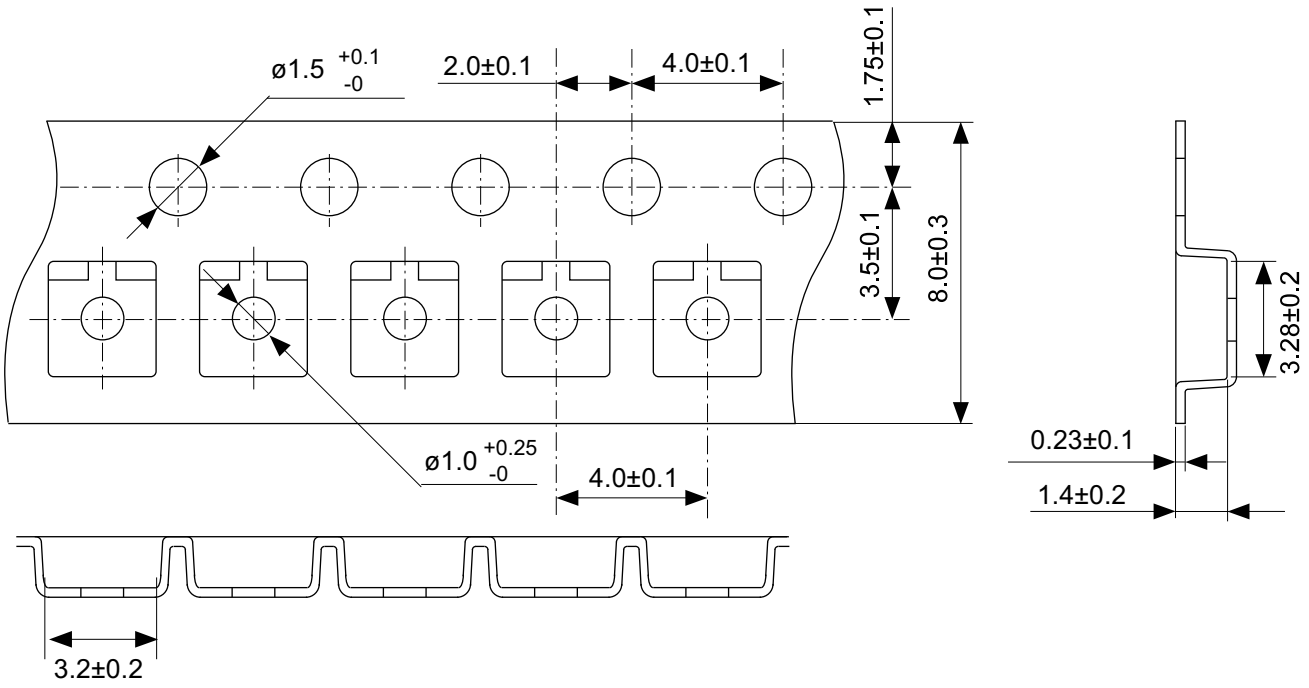
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

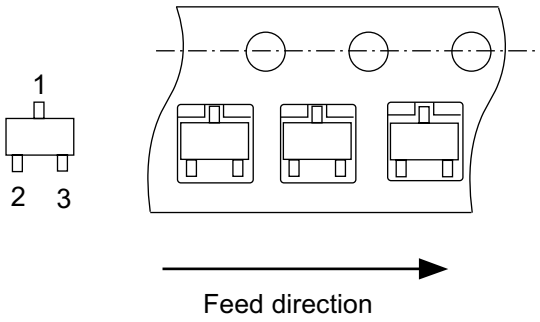
No. SNT4A-A-Board-SD-1.0



No. MP003-C-P-SD-1.1

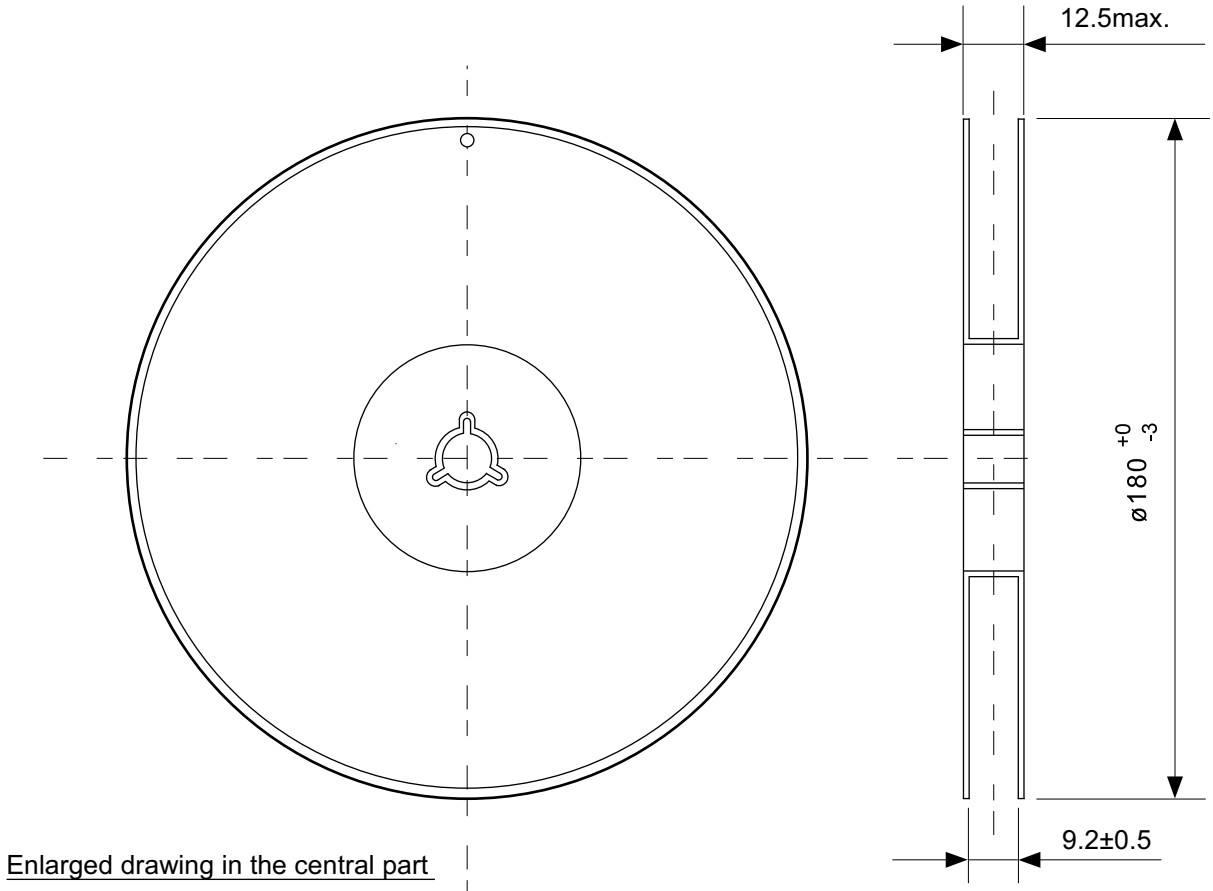
TITLE	SOT233-C-PKG Dimensions
No.	MP003-C-P-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	



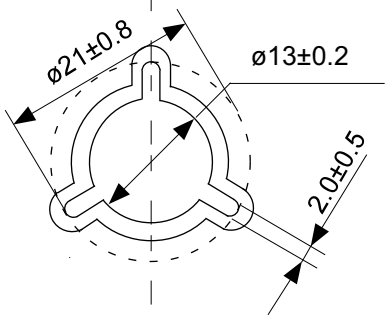


No. MP003-C-C-SD-2.0

TITLE	SOT233-C-Carrier Tape
No.	MP003-C-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

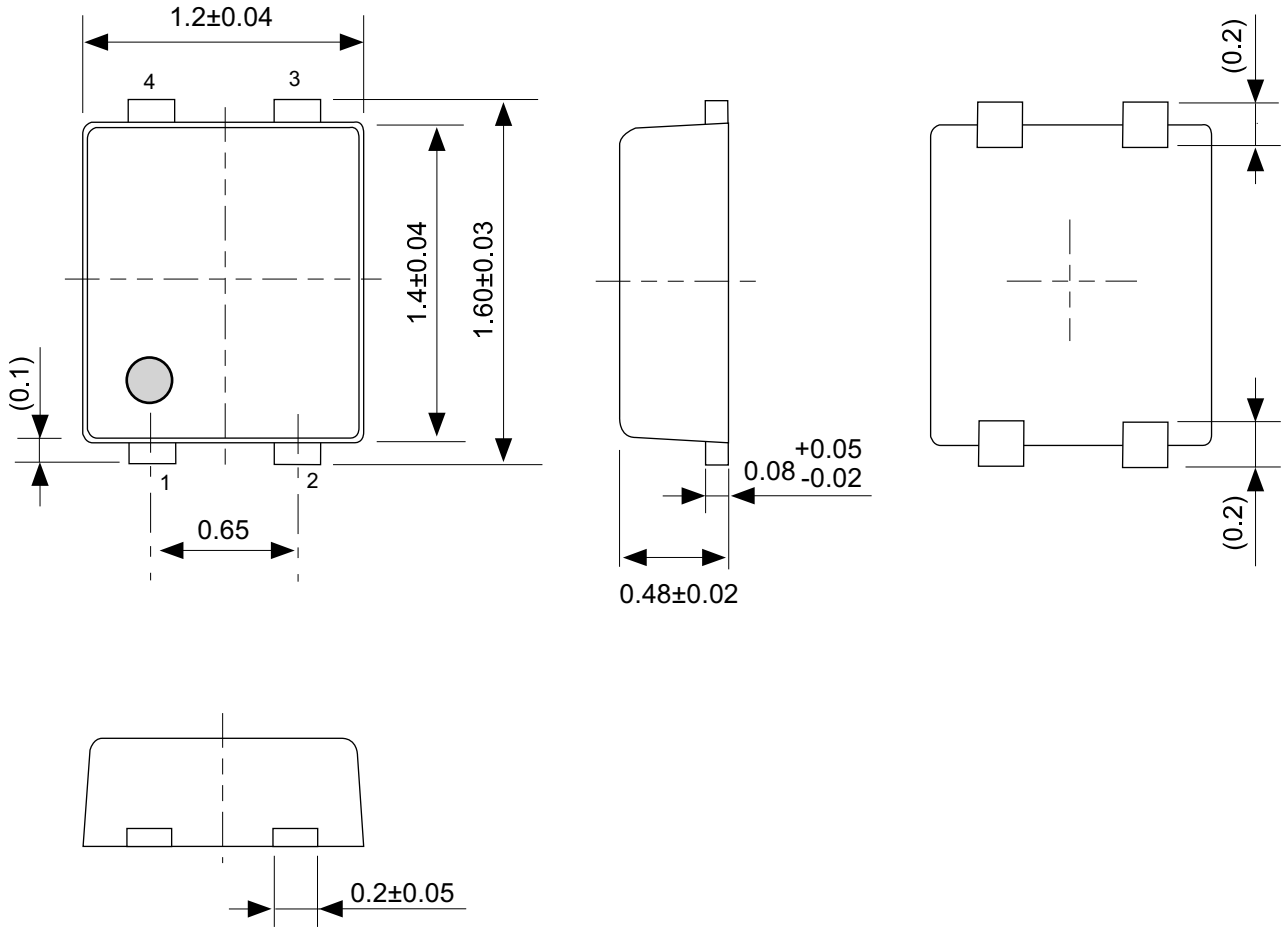


Enlarged drawing in the central part



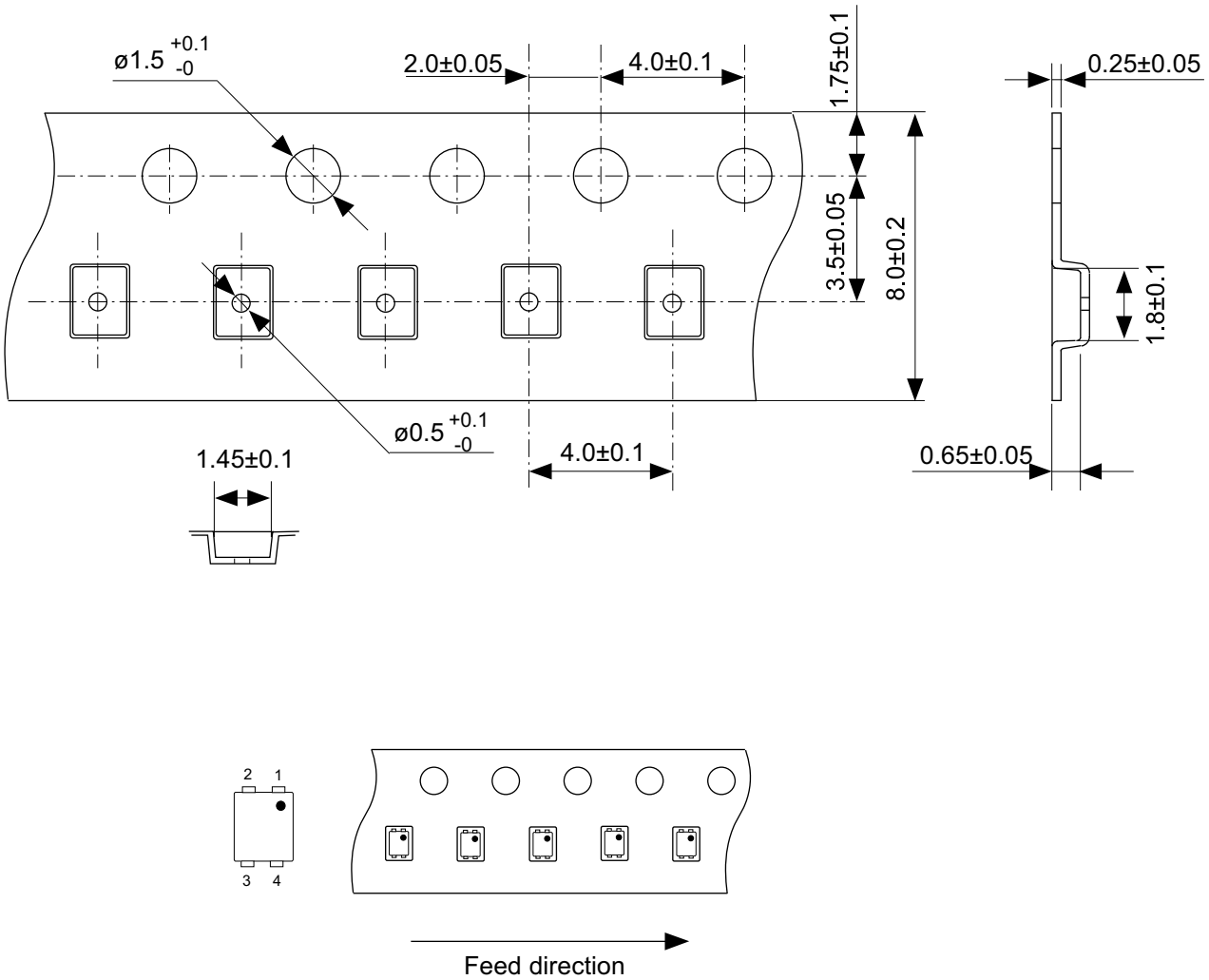
No. MP003-Z-R-SD-1.0

TITLE	SOT233-C-Reel		
No.	MP003-Z-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



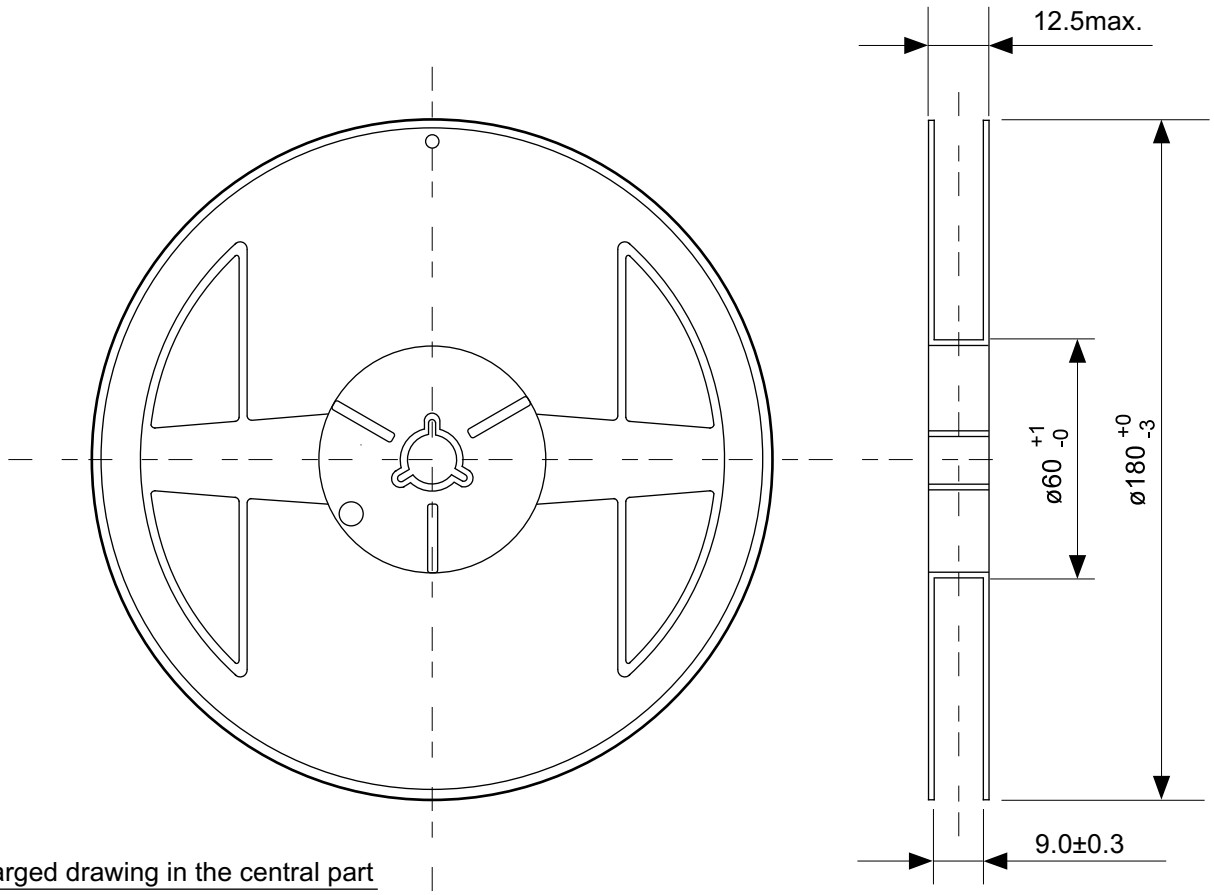
No. PF004-A-P-SD-6.0

TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm
ABLIC Inc.	

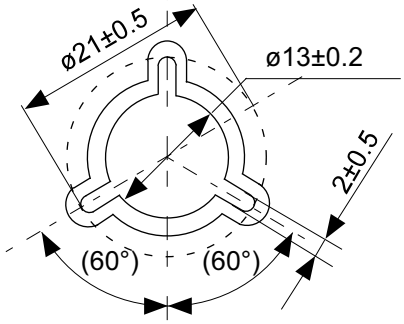


No. PF004-A-C-SD-2.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

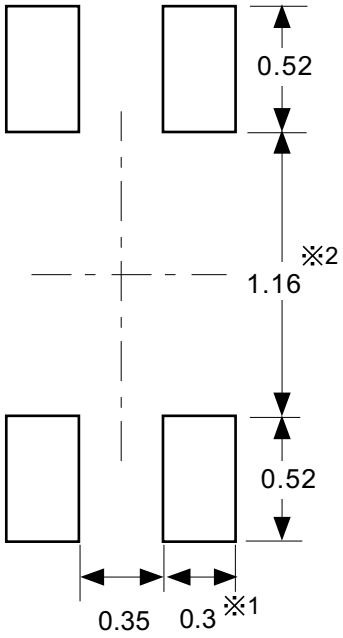


Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は ″SNTパッケージ活用の手引き″ を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.4-2019.07