Ordering Information

RT8077□□

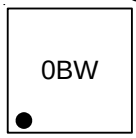
- Package Type
  QW : WDFN-8L 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

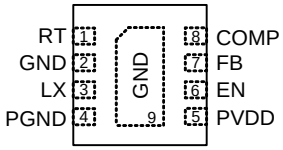


0B : Product Code

W : Date Code

Pin Configurations

(TOP VIEW)

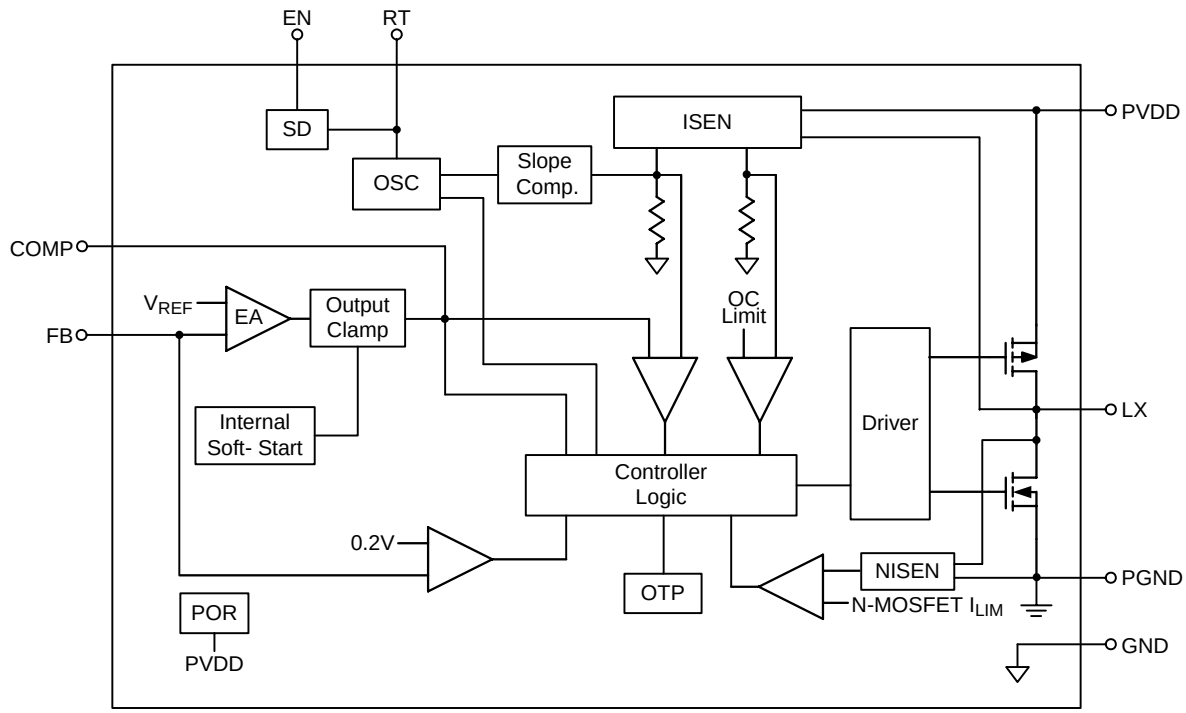


WDFN-8L 2x2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	RT	Switching Frequency Setting. Connecting a resistor to ground from this pin sets the switching frequency.
2, 9 (Exposed Pad)	GND	Signal Ground. All small-signal components and compensation components should be connected to this ground, which in turn connects to PGND at one point.
3	LX	Switch Node. Connect this pin to the inductor.
4	PGND	Power Ground. Connect this pin close to the negative terminal of C_{IN} and C_{OUT}.
5	PVDD	Power Input. Decouple this pin to PGND with a capacitor.
6	EN	Enable Control Input. A logic-high (1.2V < EN < 5.5V) enables the converter; logic-low forces the IC into shutdown mode.
7	FB	Feedback Voltage Input. This pin receives the feedback voltage from a resistive divider connected across the output.
8	COMP	Compensation Node. The current comparator threshold increases with this control voltage. Connect external compensation elements to this pin to stabilize the control loop.

Function Block Diagram



Operation

The RT8077 is a synchronous low voltage Buck converter that can support the input voltage range from 2.6V to 5.5V and the output current can be up to 2A. The RT8077 uses a constant frequency, current mode architecture. In normal operation, the high-side P-MOSFET is turned on when the logic controller is set by the oscillator (OSC) and is turned off when the current comparator resets the logic controller.

High-side MOSFET peak current is measured by internal R_{SENSE}. The Current Signal is where Slope Compensator works together with sensing voltage of R_{SENSE}. The error amplifier EA adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal 0.8V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, the COMP voltage then rises to allow higher inductor current to match the load current. UV Comparator If the feedback voltage (V_{FB}) is lower than threshold voltage 0.2V, the UV Comparator's output will go high and the Switch Controller will turn off the high-side MOSFET.

Oscillator (OSC)

The internal oscillator runs at the programmable frequency range : 300kHz to 2MHz

Enable Comparator

The EN pin can be connected to VIN through a 100kΩ external resistor for automatic startup.

Soft-Start (SS)

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 1ms.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, PVDD ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8L 2x2 ---------- 0.833W
- Package Thermal Resistance (Note 2)
  WDFN-8L 2x2, θ_{JA} ---------- 120°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, PVDD ---------- 2.6V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Reference Voltage		V_{REF}		0.788	0.8	0.812	V
EN Input Voltage	Logic-High	V_{EN_H}		1.2	--	5.5	V
	Logic-Low	V_{EN_L}		--	--	0.4	
Feedback Leakage Current		I_{FB}	V_{FB} = 3.3V	--	0.1	0.4	μA
Quiescent Current			V_{FB} = 0.85V	--	270	--	μA
			Shutdown, V_{EN} = 0V	--	--	1	
Output Voltage Line Regulation		ΔV_{LINE}	V_{IN} = 2.6V to 5.5V	--	0.1	--	%/V
Output Voltage Load Regulation		ΔV_{LOAD}	V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A	--	0.4	--	%
Error Amplifier Transconductance		gm		--	400	--	μA/V
Current Sense Transresistance		R_S		--	0.2	--	Ω
Switching Frequency			R_{OSC} = 180kΩ	1.44	1.8	2.16	MHz
			Adjustable Switching Frequency Range	0.3	--	2	
Switch On-Resistance	High-Side	$R_{DS(ON)\_P}$	I_{SW} = 0.3A, PVDD = 3.6V	--	90	130	mΩ
	Low-Side	$R_{DS(ON)\_N}$	I_{SW} = 0.3A, PVDD = 3.6V	--	90	130	
Peak Current Limit		I_{LIM}		3	--	--	A
Under-Voltage Lockout Threshold (Note 5)			V_{DD} Rising	--	2.4	--	V
			V_{DD} Falling	--	2.2	--	
Over Temperature Protection							
Thermal Shutdown		T_{SD}	Rising	--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Typical Application Circuit

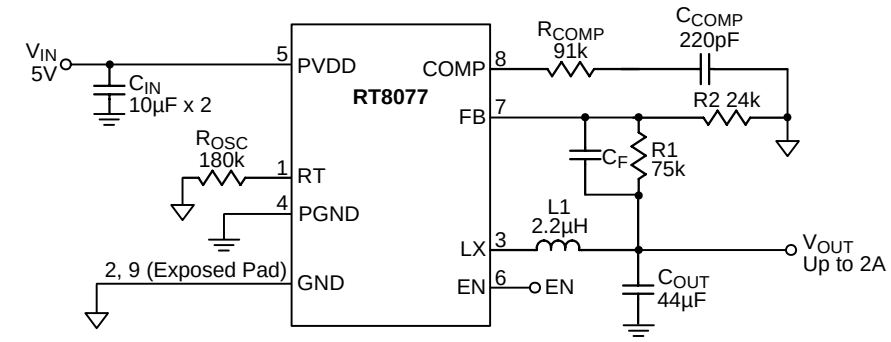
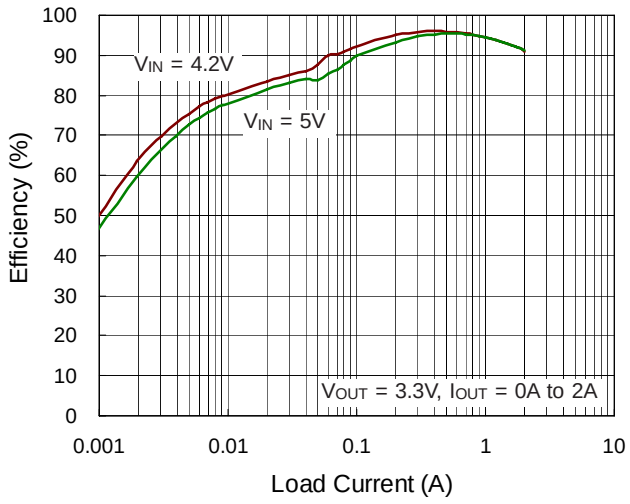


Table 1. Recommended Component Selection

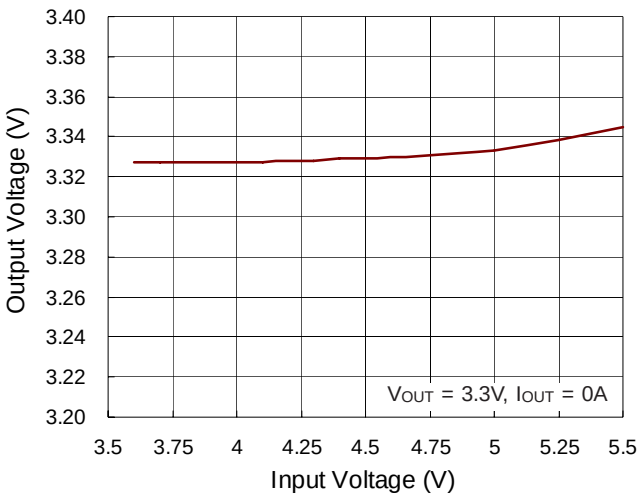
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_{COMP} (kΩ)	C_{COMP} (nF)	L1 (µH)	C_{OUT} (µF)
3.3	75	24	91	0.22	2.2	22x2
2.5	51	24	75	0.47	2.2	22x2
1.8	30	24	51	0.68	2.2	22x2
1.5	21	24	47	0.68	2.2	22x2
1.2	12	24	30	0.68	1	22x2
1	6	24	24	0.68	1	22x2

Typical Operating Characteristics

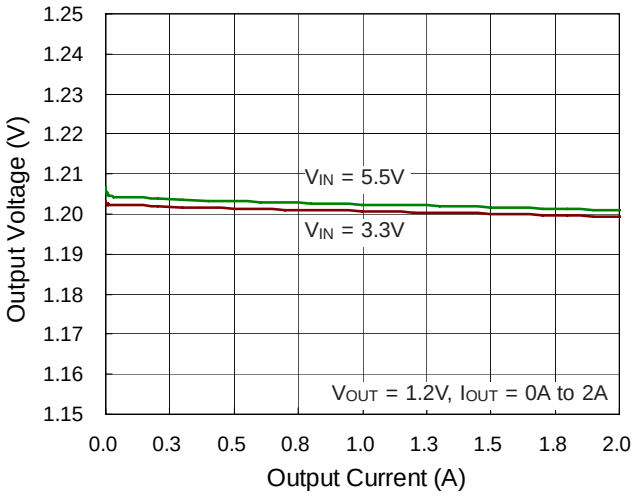
Efficiency vs. Load Current



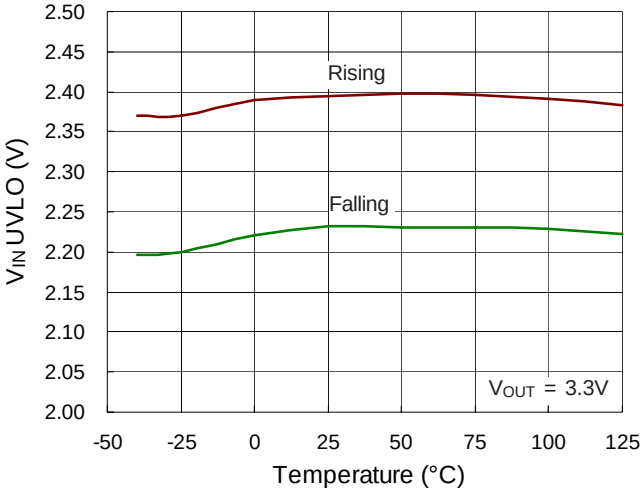
Output Voltage vs. Input Voltage



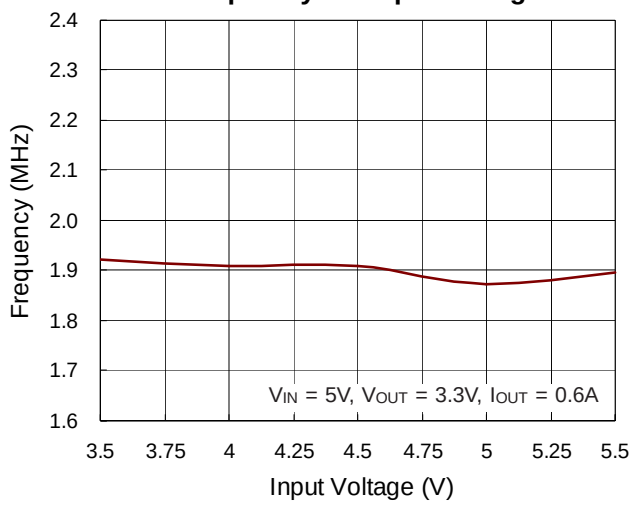
Output Voltage vs. Output Current



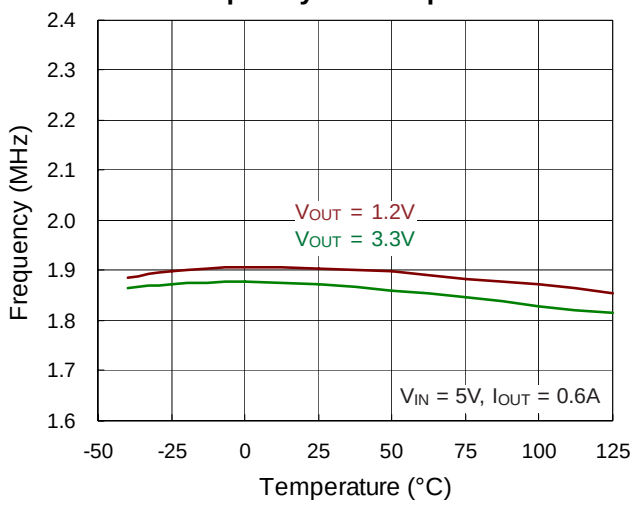
V_{IN} UVLO vs. Temperature



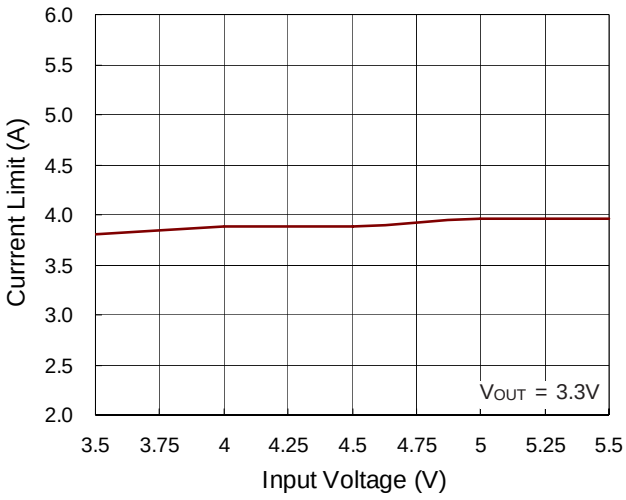
Frequency vs. Input Voltage



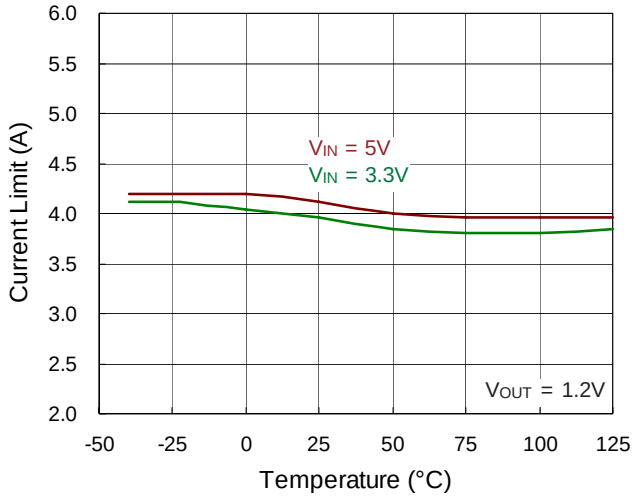
Frequency vs. Temperature



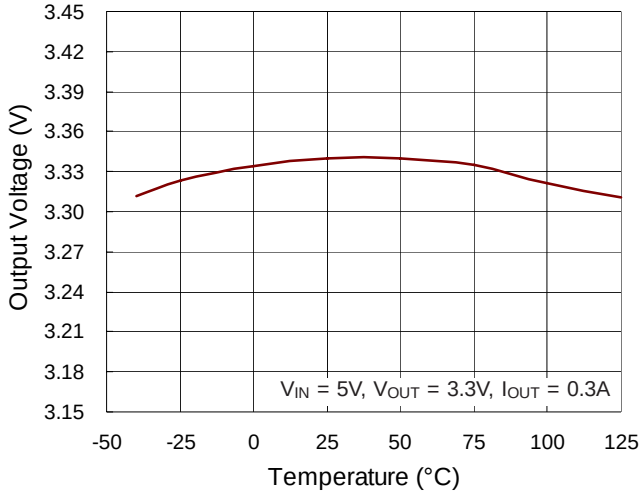
Currrent Limit vs. Input Voltage



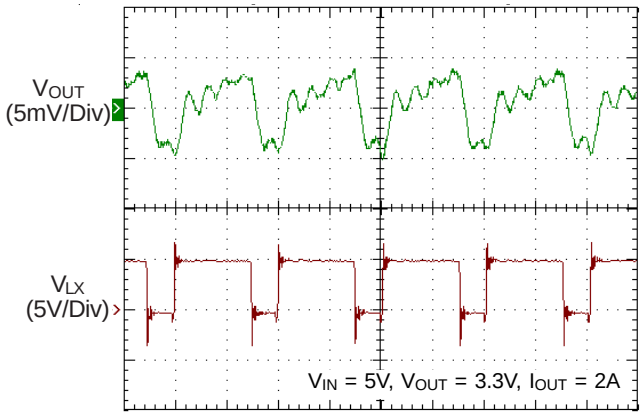
Current Limit vs. Temperature



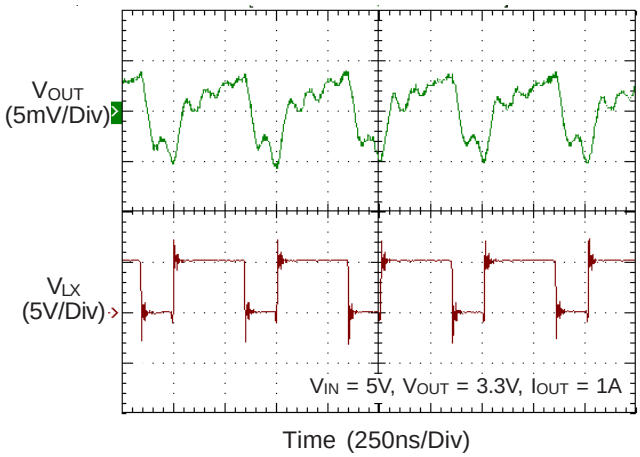
Output Voltage vs. Temperature



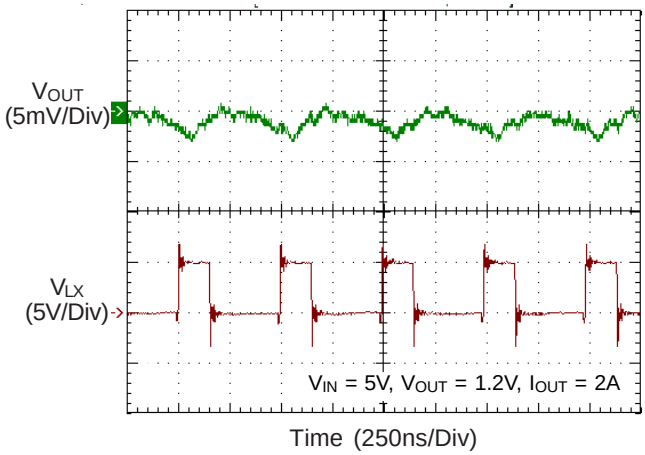
Output Ripple



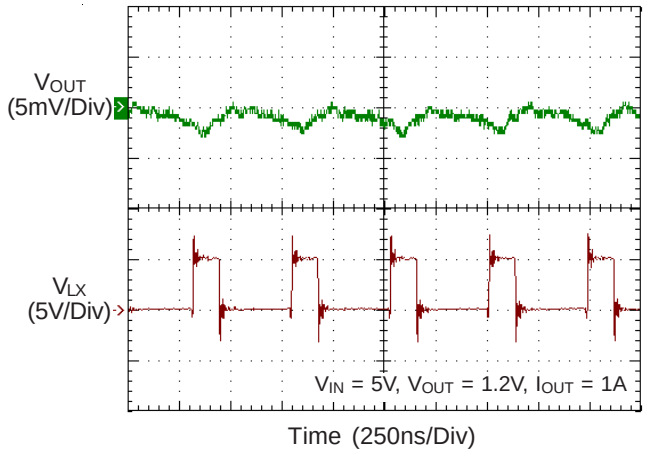
Output Ripple



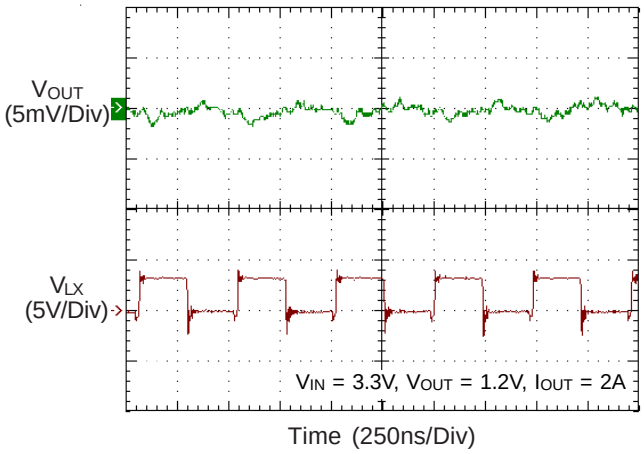
Output Ripple



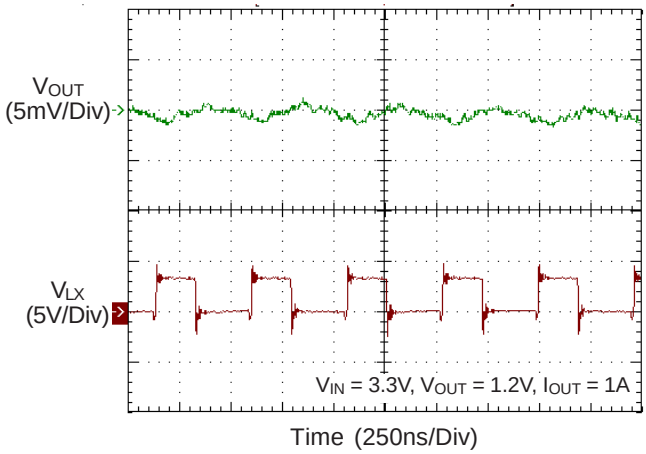
Output Ripple



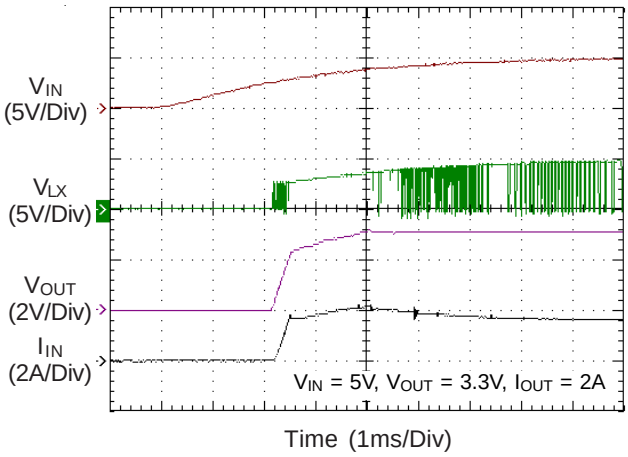
Output Ripple



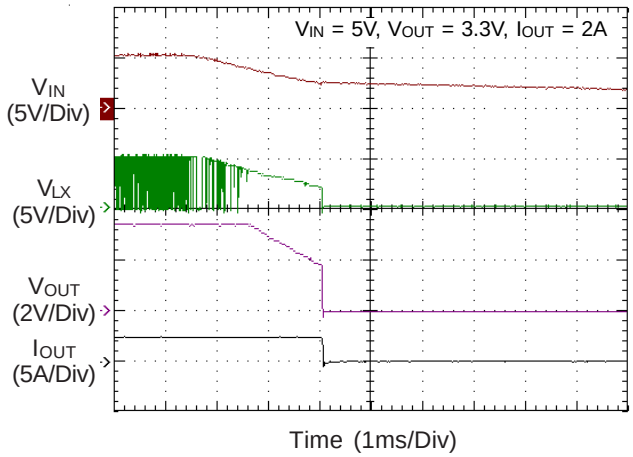
Output Ripple



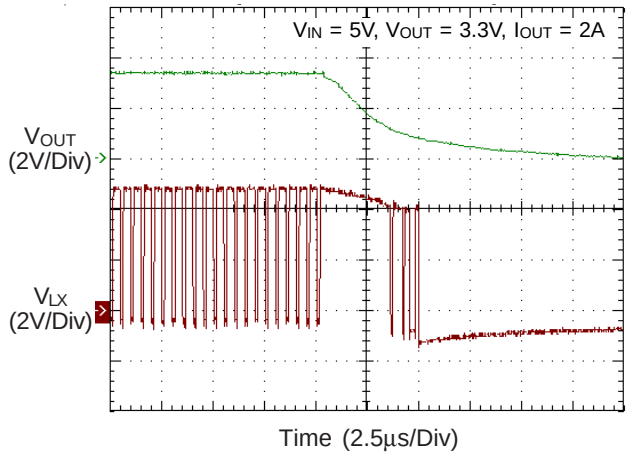
Power On from V_{IN}



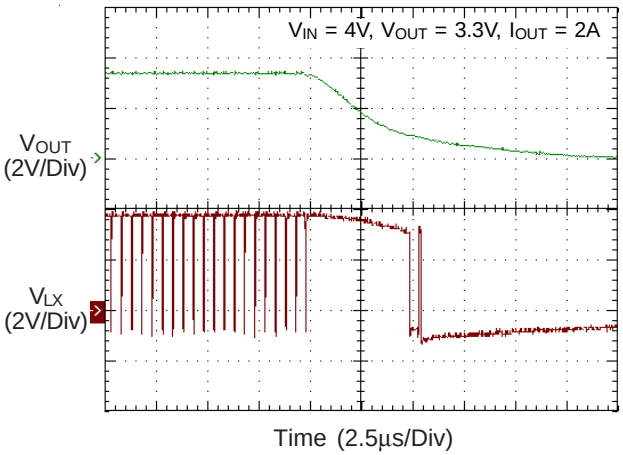
Power Off from V_{IN}



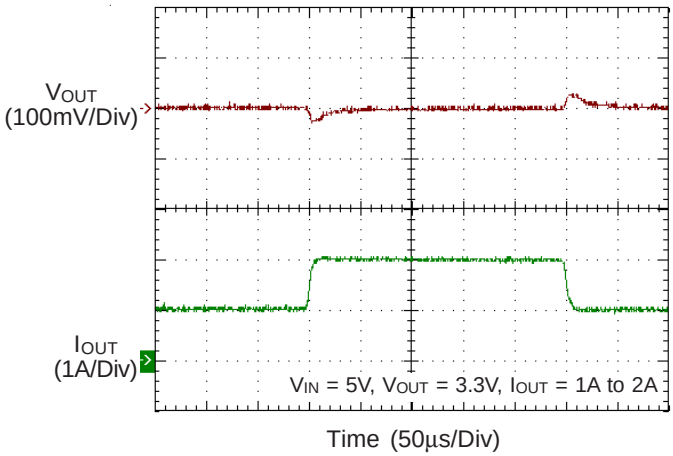
UVP Shutdown



UVP Shutdown



Load Transient Response



Application Information

The basic RT8077 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Soft-Start

The RT8077 contains an internal soft-start clamp that gradually raises the clamp on the COMP pin.

Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The operating frequency of the RT8077 is determined by an external resistor that is connected between the RT pin and GND. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator. The RT resistor value can be determined by examining the frequency vs. R_{OSC} curve. Although frequencies as high as 2MHz are possible, the minimum on-time of the RT8077 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 110ns. Therefore, the minimum duty cycle is equal to 110ns x f (Hz).

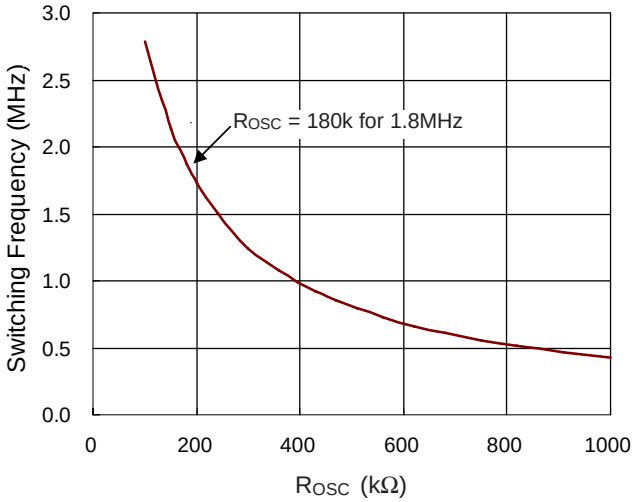


Figure 1

100% Duty Cycle Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle eventually reaching 100% duty cycle.

The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-MOSFET and the inductor.

Low Supply Operation

The RT8077 is designed to operate down to an input supply voltage of 2.6V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-Channel and N-Channel power switches increases. The user should calculate the power dissipation when the RT8077 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the RT8077, however, separated inductor current signals are used to monitor over-current condition. This keeps the maximum output current relatively constant regardless of duty cycle.

Short-Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. A current runaway detector is used to monitor inductor current. As current increasing beyond the control of current loop, switching cycles will be skipped to prevent current runaway from occurring.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.4(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{DD}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-8L 2x2 packages, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for WDFN-8L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

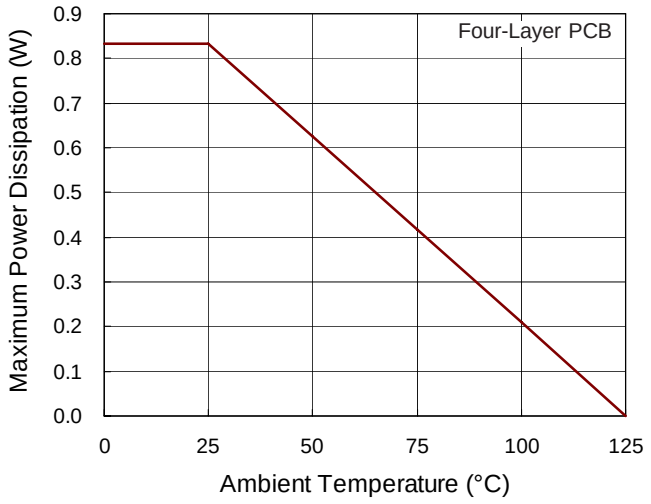


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8077.

- A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the GND pin at one point that is then connected to the PGND pin close to the IC. The exposed pad should be connected to GND.
- Connect the terminal of the input capacitor(s), C_{IN}, as close as possible to the PVDD pin. This capacitor provides the AC current into the internal power MOSFETs.
- LX node is with high frequency voltage swing and should be kept within small area. Keep all sensitive small-signal nodes away from the LX node to prevent stray capacitive noise pick-up.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components.

  You can connect the copper areas to any DC net (PVDD, PGND, GND, or any other DC rail in your system).
- Connect the FB pin directly to the feedback resistors. The resistor divider must be connected between V_{OUT} and GND.

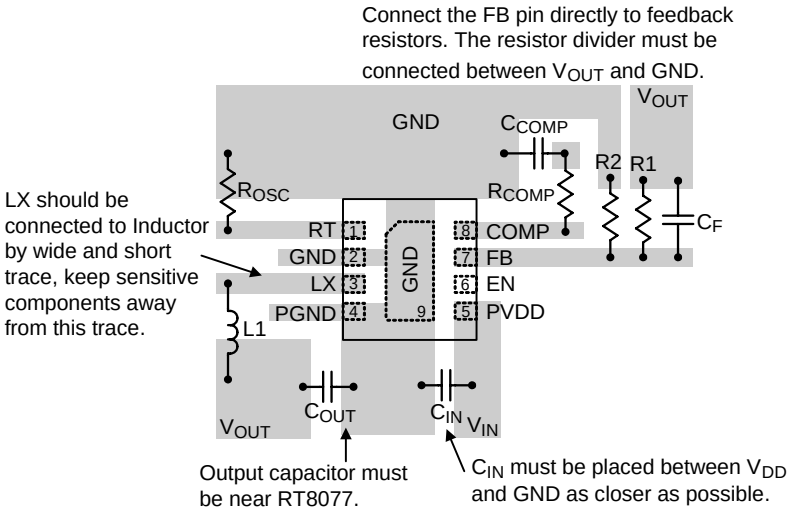


Figure 4. PCB Layout Guide

Recommended component selection for Typical Application.

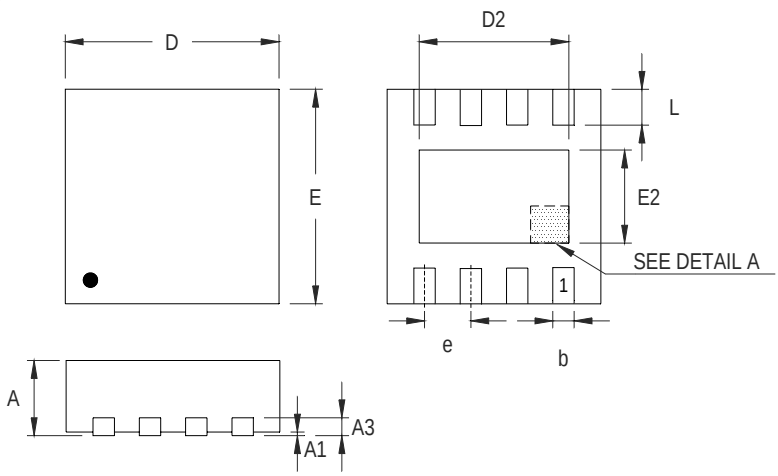
Table 2. Inductors

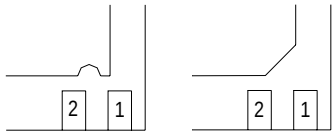
Component Supplier	Series	Inductance (μH)	DCR (mΩ)	Current Rating (mA)	Dimensions (mm)
TAIYO YUDEN	NRS8040	2	10	8100	8x8x4

Table 3. Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (μF)	Case Size
TDK	C3225X5R0J226M	22	1210
TDK	C2012X5R0J106M	10	0805
Panasonic	ECJ4YB0J226M	22	1210
Panasonic	ECJ4YB1A106M	10	1210
TAIYO YUDEN	LMK325BJ226ML	22	1210
TAIYO YUDEN	JMK316BJ226ML	22	1206
TAIYO YUDEN	JMK212BJ106ML	10	0805

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

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