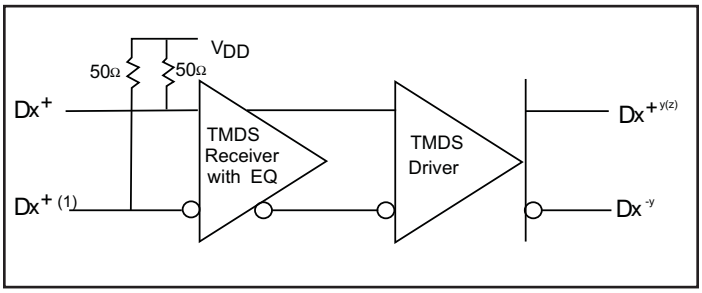
Function Block Description



Notes:
1. X = 0,1,2,3
2. Y = A,B

Maximum Ratings (Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....–65°C to +150°C
Supply Voltage to Ground Potential.....–0.5V to +5V
DC Input Voltage.....–0.5V to V_{DD}
DC Output Current.....120mA
Power Dissipation.....1.0W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Pin Description

Pin #	Pin Name	I/O	Description
2, 6, 11, 15, 22, 24, 36, 48	V_{DD}	Power	3.3V power supply
3, 14, 21, 23, 27, 30, 33, 39, 42, 45, 53	GND	Power	0V power supply
16	SEL_Out	O	Output bit, that provides information to user as to which port is active, if SEL_OUT = 'LOW', then Port A is active, if SEL_OUT = 'HIGH', then Port B is active. Only used when MS pin is 'HIGH'
19	SCL	I	I^2C Clock Input Signal
20	SDA	I/O	I^2C Data Input/Output Signal
18	NC	N/A	No Connect.
1	MS	I	Mode Select Pin. If MS = 'HIGH', then I^2C control is active. Pins 49-52 are I^2C address and pin 19 is SCL and pin 20 is SDA. If MS = 'LOW', then I^2C control is inactive and pin programmability is active. Pins 49-52 are control pins only for Port A, S4-S7 and pin 19 is S2 and pin 20 is S3. If 'MS' = "LOW", Port B cannot be configured and is left as default. Port B default value is 0dB pre-emphasis, 0dB de-emphasis, and 500mV output swing
55	SEL_IN	I	Output port select. (Logically similar to I^2C bit S1 - see page 3)
54	Test_in	I	Input pin for internal testing. Tie to GND for normal operation
56	OE	I	Output is enabled and normal when OE = 'HIGH'. If OE = 'LOW', both outputs, A and B, are disabled and at Hi-Z
17	Test_Out	O	Output pin for internal testing. Not used for normal operation
4, 5, 7, 8, 9, 10, 12, 13	Dx	I	Input TMDS high speed signals
28, 29, 31, 32, 34, 35, 40, 41, 43, 44, 46, 47, 25, 26, 37, 38	Dx y	O	Output TMDS high speed signals
49,50, 51, 52	A0, A1, A2, A3	I	I^2C address inputs if MS = 'HIGH'.
49,50, 51, 52	S4, S5, S6, S7	I	If MS = 'LOW', then pins 49-52 are control bits S4-S7 for port A only, as shown in truth table on page 3 of datasheet
19	S3	I	If MS = 'LOW', then pins 19 is control bit S3, as shown in the truth table on page 3
20	S2	I	If MS = 'LOW', then pins 20 is control bit S2, as shown in the truth table on page 3

I²C Truth Table

(At power up, default values are: Port A is active, signal swing is set to 500mV, pre-emphasis and de-emphasis are at 0dB, and equalization is at 1dB)

Byte 2: S[7:0]=00000001

Output Swing: 500mV
Pre-emphasis: 0dB
De-Emphasis: 0dB
Equalization: 1dB
Active Port: port A

Byte 3: S[7:0]=00000001

Output Swing: Defined by Byte 2
Pre-emphasis:
De-Emphasis:
Active Port: port A, in normal mode

BYTE 1 (Address Assignment)

Address	A6	A5	A4	A3	A2	A1	A0	R/W
Value	1	1	0	A3	A2	A1	A0	R=1/W=0

BYTE 2 (1st Data byte - Port A control and input control)

Port A and Input Control	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**	**Result**		
									Swing (mV)	**Pre-emphasis (dB)**	**De-emphasis (dB)**
Swing Control	0	0	0	0	x	x	x	x	500	0	0
	0	0	0	1	x	x	x	x	750	0	0
	0	0	1	0	x	x	x	x	1000	0	0
	0	0	1	1	x	x	x	x	N/A	N/A	N/A
Pre-Emphasis	0	1	0	0	x	x	x	x	500	0	0
	0	1	0	1	x	x	x	x	500	1.5	0
	0	1	1	0	x	x	x	x	500	3.5	0
	0	1	1	1	x	x	x	x	500	6.0	0
De-Emphasis	1	0	0	0	x	x	x	x	750	0	0
	1	0	0	1	x	x	x	x	750	0	-1.5
	1	0	1	0	x	x	x	x	750	0	-3.5
	1	0	1	1	x	x	x	x	750	0	-6.0
Output Port Select	x	x	x	x	x	x	0	1	Port A is active		
	x	x	x	x	x	x	1	1	Port B is active		
	x	x	x	x	x	x	x	0	Port A = Hi-Z		
Equalization (dB)	x	x	x	x	0	0	x	x	1		
	x	x	x	x	0	1	x	x	3.5		
	x	x	x	x	1	0	x	x	6		
	x	x	x	x	1	1	x	x	8		

BYTE 3 (2nd Data byte - Port B control)

Port B Control only	S7	S6	S5	S4	S3	S2	S1	S0	Result		
									Swing (mV)	Pre-emphasis (dB)	De-emphasis (dB)
Swing Control	0	0	0	0	x	x	x	x	500	0	0
	0	0	0	1	x	x	x	x	750	0	0
	0	0	1	0	x	x	x	x	1000	0	0
	0	0	1	1	x	x	x	x	N/A	N/A	N/A
Pre-Emphasis	0	1	0	0	x	x	x	x	500	0	0
	0	1	0	1	x	x	x	x	500	1.5	0
	0	1	1	0	x	x	x	x	500	3.5	0
	0	1	1	1	x	x	x	x	500	6.0	0
De-Emphasis	1	0	0	0	x	x	x	x	750	0	0
	1	0	0	1	x	x	x	x	750	0	-1.5
	1	0	1	0	x	x	x	x	750	0	-3.5
	1	0	1	1	x	x	x	x	750	0	-6.0
Output Port Select	x	x	x	x	x	x	0	1	Normal		
	x	x	x	x	x	x	1	1	TEST MODE		
	x	x	x	x	x	x	x	0	Port B = Hi-Z		

TMDS Compliance Test Results

Item	HDMI™ 1.3 Spec	Pericom TMDS Product Spec
Operating Conditions		
Termination Supply Voltage, A_{VDD}	3.3V ≤ 5%	3.30 ± 5%
Terminal Resistance	50 Ohm ≤ 10%	45 to 55 Ohm
Source DC Characteristics at TP1		
Single-ended high level output voltage, V_H	A_{VDD} ≤ 10mV	A_{VDD} ≤ 10mV
Single-ended low level output voltage, V_L	(A_{VDD} - 600mV) ≤ VL ≤ (A_{VDD} - 400mV)	(A_{VDD} - 600mV) ≤ VL ≤ (A_{VDD} - 400mV)
Single-ended output swing voltage, V_{swing}	400mV ≤ V_{swing} ≤ 600mV	400mV ≤ V_{swing} ≤ 600mV
Single-ended standby (off) output voltage, V_{off}	A_{VDD} ± 10mV	A_{VDD} ± 10mV
Single-ended standby (off) output current, I_{off}	| I_{OFF} | < 10uA	| I_{OFF} | <10uA
Transmitter AC Characteristics at TP1		
Risetime/Falltime (20%-80%)	75ps ≤ Risetime/Falltime ≤ 0.4 Tbit (75ps ≤ tr/tf ≤ 242ps) @ 1.65Gbps	240ps
Intra-Pair Skew at Transmitter Connector, max	0.15 Tbit (90.9ps @ 1.65Gbps)	60ps max
Inter-Pair Skew at Transmitter Connector, max	0.2 Tpixel (1.2ns @ 1.65Gbps)	100ps max
Clock Jitter, max	0.25 Tbit (151.5ps @ 1.65Gbps)	82ps max
Sink Operating DC Characteristics at TP2		
Input Differential Voltage Level, V_{diff}	150 ≤ Vdiff ≤ 1200mV	150mV ≤ V_{DIFF} ≤ 1200mV
Input Common Mode Voltage Level, V_{ICM}	A_{VDD} -300mV ≤ V_{ICM} < A_{VDD} -37.5mV or A_{VDD} ±10%	A_{VDD} -300mV ≤ V_{ICM} < A_{VDD} - 37.5mV or A_{VDD} ±10%
Sink DC Characteristics When Source Disabled or Disconnected at TP2		
Differential Voltage Level	A_{VDD} ± 10mV	A_{VDD} ± 10mV

DC Electrical Characteristics (T_A = –40°C to +85°C, unless otherwise noted. V_{DD} = 3.3V ±0.3V)

Symbol	Parameter	Test Condition[1]	Min.	Typ.[2]	Max.	Units
V_H	Single-ended high level output voltage		V_{DD} – 10mV	V_{DD}	V_{DD} + 10mV	V
V_L	Single-ended low level output voltage		V_{DD} – 600mV		V_{DD} - 400mV	V
Vswing	Single-ended output swing voltage		400		600	mV
V_{OFF}	Single-ended standby (off) output voltage		V_{DD} – 10mV	V_{DD}	V_{DD} + 10mV	V
I_{OFF}	Single-ended standby (off) output current				10	µs
V_{OS}	Offset Voltage				V_{DD} – 250mV	V
V_{IH}	Minimum Input High Voltage		1.8			V
V_{IL}	Minimum Input Low Voltage				0.8	
I_{CC}	Power Supply Current				280	mA

AC Electrical Characteristics (T_A = –40°C to +85°C, V_{DD} = 3.3V ±0.3V)

Symbol	Paramter	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
T_{20-80}	Rise time/fall time (20% - 80%)		75		240	ps
	Overshoot				15% of V_{swing} * 2	
	Undershoot				25% of V_{swing} * 2	
	Intra-Pair Skew at Source Connector				60	ps
	Inter-Pair Skew at Connector				100	ps
	Clock duty cycle		40%	50%	60%	
	Through connection impedance		85	100	115	ps
	TMDS differential clock Jitter				82	ps
	At Termination impedance		90	100	110	ps
t_{PHLD}	Differenital Propagation Delay High to Low			1.0		ns
t_{PLHD}	Differential Propagation Delay Low to High			1.0		ns
t_{SKD}	Differential Skew | t_{PHLD} - t_{PLHD} |			25		ps
t_{PHZ}	Disable Time High to Z			5		ns
t_{PLZ}	Disable Time Low to Z			5		
t_{PZH}	Enable Time Z to High			1		µs
t_{PZL}	Enable Time Z to Low			1		

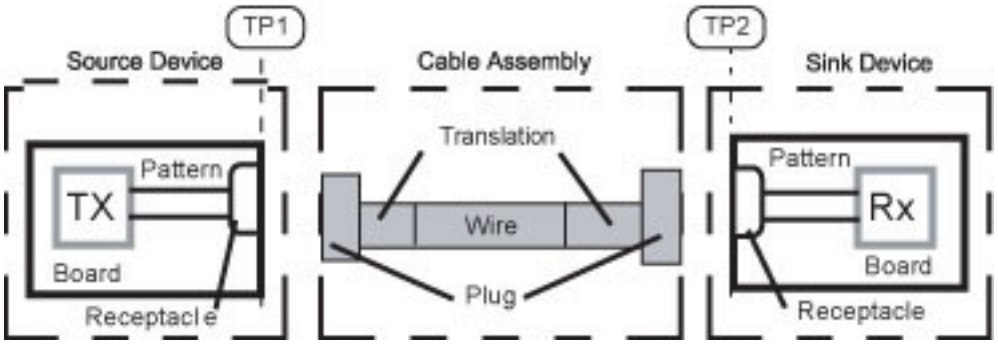
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Power Supply Characteristics

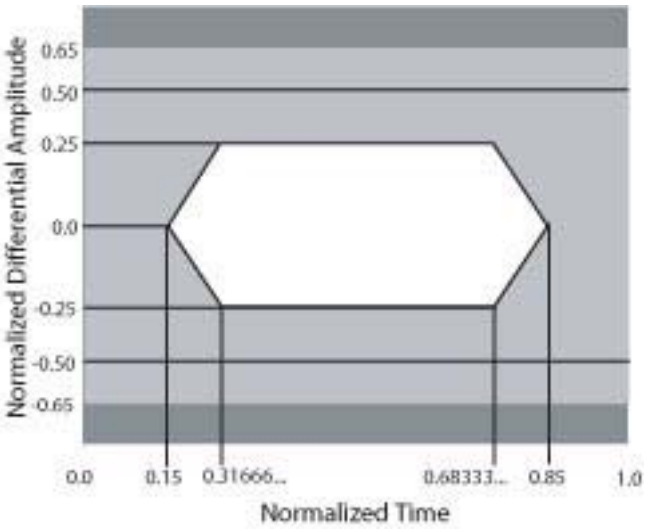
Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{DD} = Max., V_{IN} = V_{DD}, OE = 'LOW'		1		mA

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

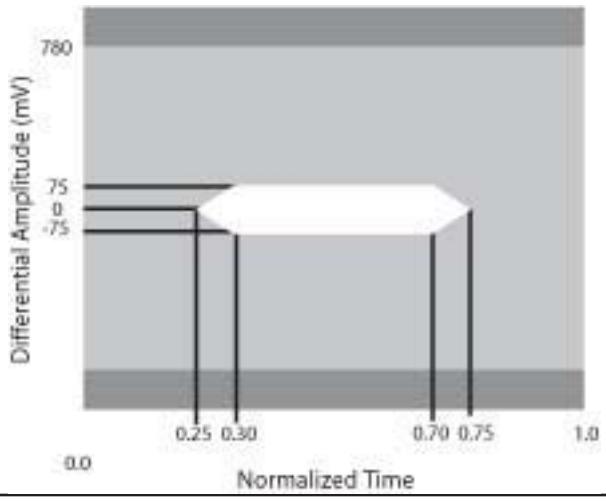
TMDS Link Test Points



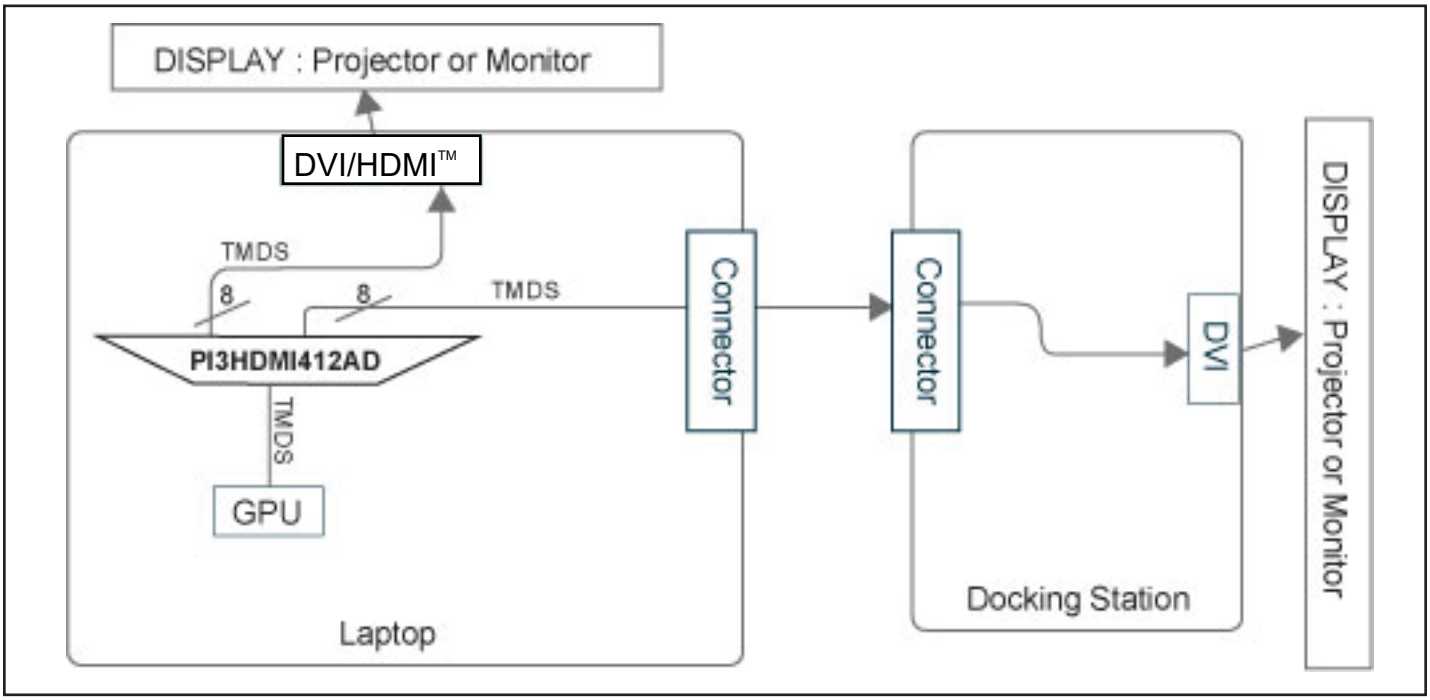
Normalized Eye Diagram Mask at TP1 for Source Requirements



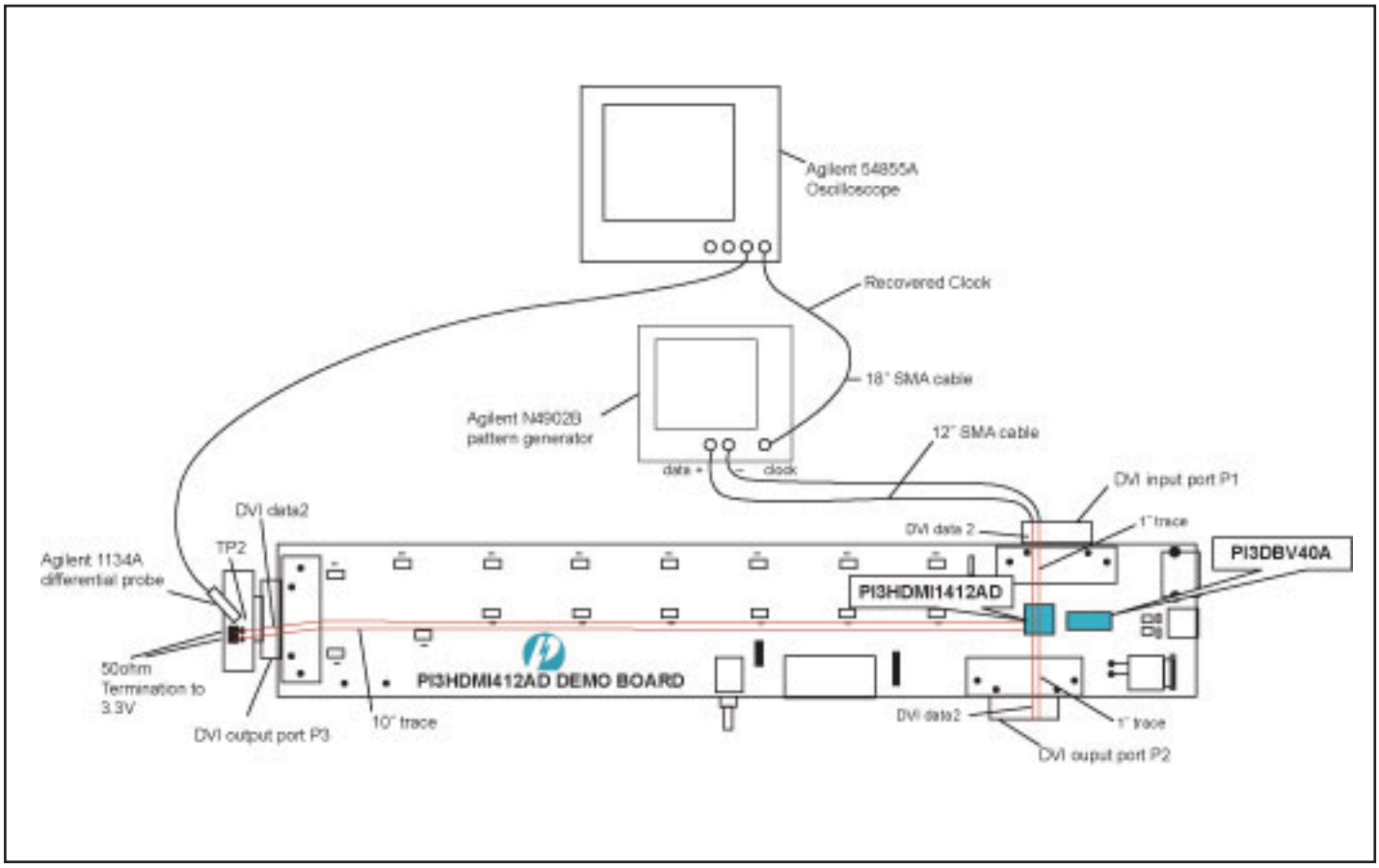
Absolute Eye Diagram Mask at TP2 for Sink Requirements



Application Information (Please see application note for important design information.)

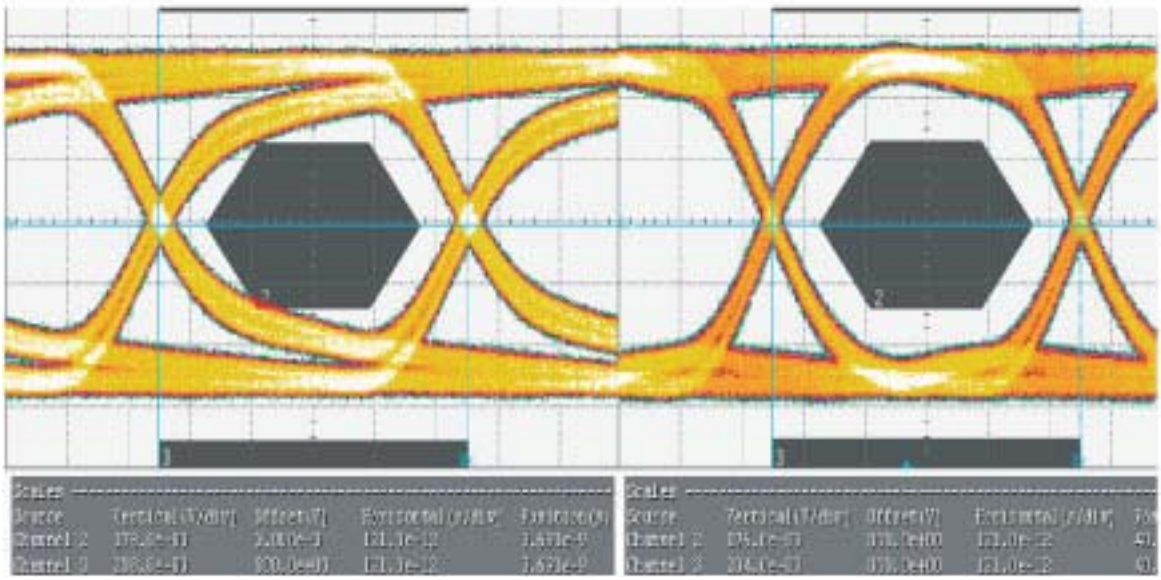


DVI TP2 (Tx) Compliance Test Setup



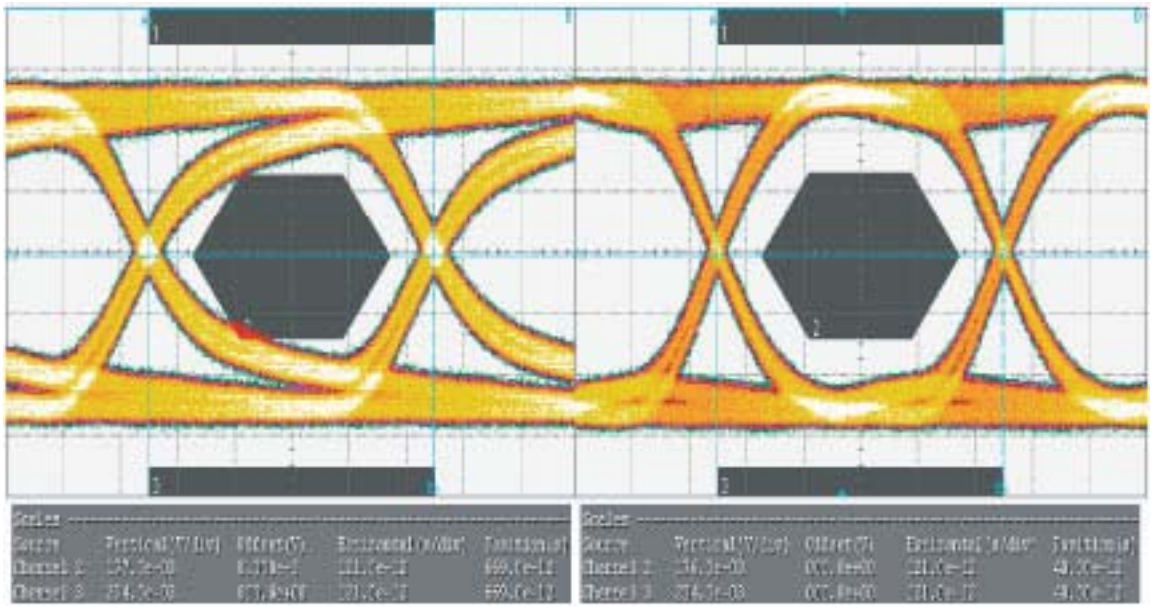
Pre-Emphasis Validation

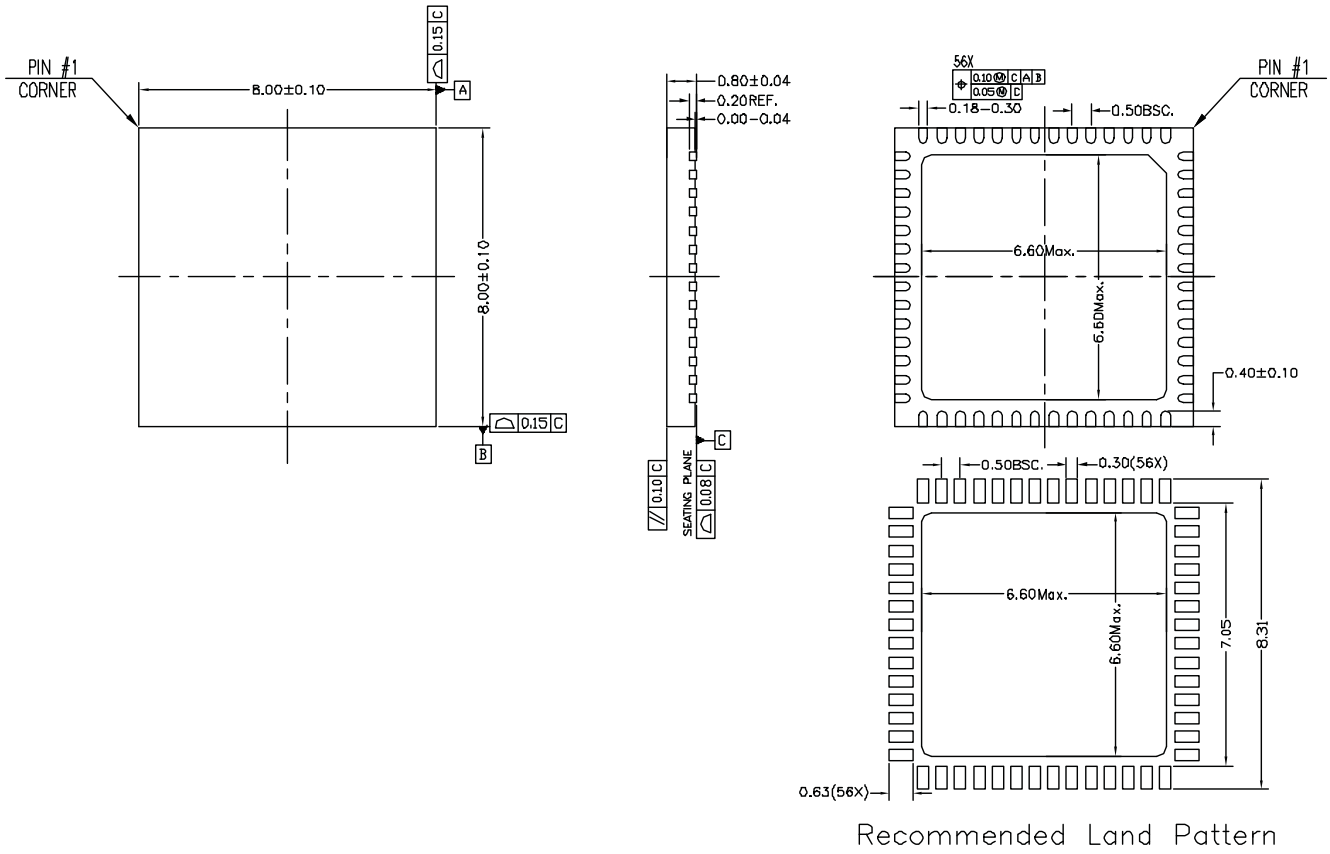
Measured at ouput DVI port, P3; Right eye is with pre-emphasis, left eye is without pre-emphasis



De-Emphasis Validation

Measured at ouput DVI port, P3; Right eye is with de-emphasis, left eye is without de-emphasis





Notes:
1) All dimensions are in millimeters, angles in Degrees.
2) Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
3) Refer JEDEC MO-220 modified
4) Thermal Via Diameter. Recommended 0.2~0.33mm
5) Thermal Via Pitch. Recommended 1.27mm

PERICOM Semiconductor Corporation — DATE: 02/17/06

DESCRIPTION: 56-contact, Thin Fine Pitch Quad Flat No-lead (TQFN)

PACKAGE CODE: ZB56

DOCUMENT CONTROL #: PD-2008 — REVISION: C

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI412ADZBE	ZB	56-pin, Pb-free & Green TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel
- HDMI & Deep Color are trademarks of Silicon Image

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