Table 1. Electrical Specifications @ +25 °C, V_{DD} = 2.6 V (Z_S = Z_L = 50 Ω)

Parameter	Condition	Min	Typ	Max	Unit
Operational Frequency		100		3000	MHz
Insertion Loss	ANT - TX - 850 / 900 MHz ANT - TX - 1800 / 1900 MHz ANT - RX - 850 / 900 MHz ANT - RX - 1800 / 1900 MHz		0.6 0.8 0.9 1.1	0.75 0.95 1.15 1.35	dB dB dB dB
Isolation	TX - RX - 850 / 900 MHz TX - RX - 1800 / 1900 MHz TX1 - TX2 - 850 / 900 MHz TX1 - TX2 - 1800 / 1900 MHz	46 38 28 22	50 42 30 24		dB dB dB dB
Return Loss	850 / 900 MHz 1800 / 1900 MHz	17 15	20 18		dB dB
2nd Harmonic[1]	35 dBm TX Input - 850 / 900 MHz 33 dBm TX Input - 1800 / 1900 MHz		-84 -80	-78 -77	dBc dBc
3rd Harmonic[1]	35 dBm TX Input - 850 / 900 MHz 33 dBm TX Input - 1800 / 1900 MHz		-70 -66	-68 -63	dBc dBc
IP3	RX Input		40		dBm
1dB Compression	RX Input	20			dBm
Switching time	(10-90%) (90-10%) RF		2	3	µs

Note : 1. Harmonics are characterized with a source that is 50 Ω at the fundamental and reflective at the harmonics. Contact Applications Support at help@psemi.com for more information.

Figure 3. Pin Configuration (Top View)

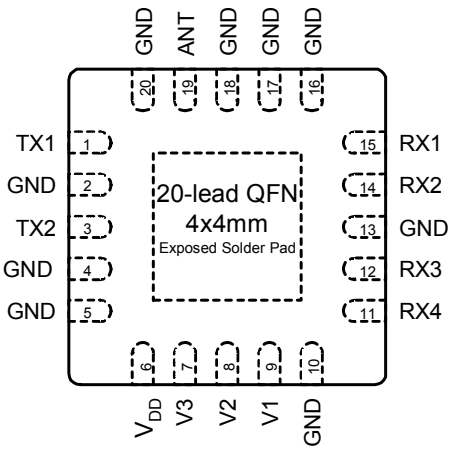


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1[1]	TX1	RF I/O - TX1
2	GND	Ground
3[1]	TX2	RF I/O – TX2
4	GND	Ground
5	GND	Ground
6	VDD	Supply
7	V3	Switch control input, CMOS logic level
8	V2	Switch control input, CMOS logic level
9	V1	Switch control input, CMOS logic level
10	GND	Ground
11[1]	RX4	RF I/O - RX4
12[1]	RX3	RF I/O - RX3
13	GND	Ground
14[1]	RX2	RF I/O - RX2
15[1]	RX1	RF I/O - RX1
16	GND	Ground
17	GND	Ground
18	GND	Ground
19[1]	ANT	RF Common – Antenna Input
20	GND	Ground

Note 1: Blocking capacitors needed only when connected to an external non-zero DC voltage.

Table 3. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Supply Voltage	2.4	2.6	2.8	V
I_{DD} Power Supply Current (V_{DD} = 2.6V)		13	20	µA
Control Voltage High	0.7 x V_{DD}			V
Control Voltage Low			0.3 x V_{DD}	V

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	+150	°C
T_{OP}	Operating temperature range	-40	+85	°C
P_{IN}	TX input power (50 Ω)		+38	dBm
	RX input power (50 Ω)		+23	
V_{ESD}[1]	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V
	ESD Voltage (CDM, JEDEC, JESD22-C101-A)		2000	V

Note 1: ANT port rated higher per applications section, see page 4.

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 5. Truth Table

Path	V3	V2	V1
ANT – RX1	0	0	0
ANT – RX2	0	0	1
ANT – RX3	0	1	0
ANT – RX4	0	1	1
ANT - TX1	1	0	x
ANT - TX2	1	1	x

Evaluation Kit

The SP6T Evaluation Kit board was designed to ease customer evaluation of the PE4268 RF switch.

The PE4268 has two high power TX ports and four high isolation RX ports. The TX ports are symmetric and are designed as paths for the 850, 900, 1800, or 1900 MHz bands. The RX ports are also symmetric and can be assigned to any of these frequency bands.

The ANT port connects through a 50 Ω transmission line to the top SMA connector, J1. The RX and TX ports connect through 50 Ω transmission lines to SMA connectors J2 – J7. A through 50 Ω transmission line between SMA connectors J9 and J10 allows estimation of the PCB losses over environmental conditions. An open transmission line connected to J11 is also provided.

J8 supplies DC power to the pin marked V_{DD} and the bottom row of pins, which is GND. 1 MΩ pull-up resistors are connected from V_{DD} to each of the three control logic inputs: V1, V2, and V3. These pull-up resistors are provided for ease of evaluation on this board and are not required for the PE4268 to operate.

Adding a jumper between a control pin and the adjacent GND pin on the bottom row of J8 will set a logic-0 on that control pin. Removing the jumper will set a logic-1. To evaluate the PE4268, add or remove jumpers according to the truth table in Table 5.

Figure 4. Evaluation Board Layout
Peregrine Specification 101/0205

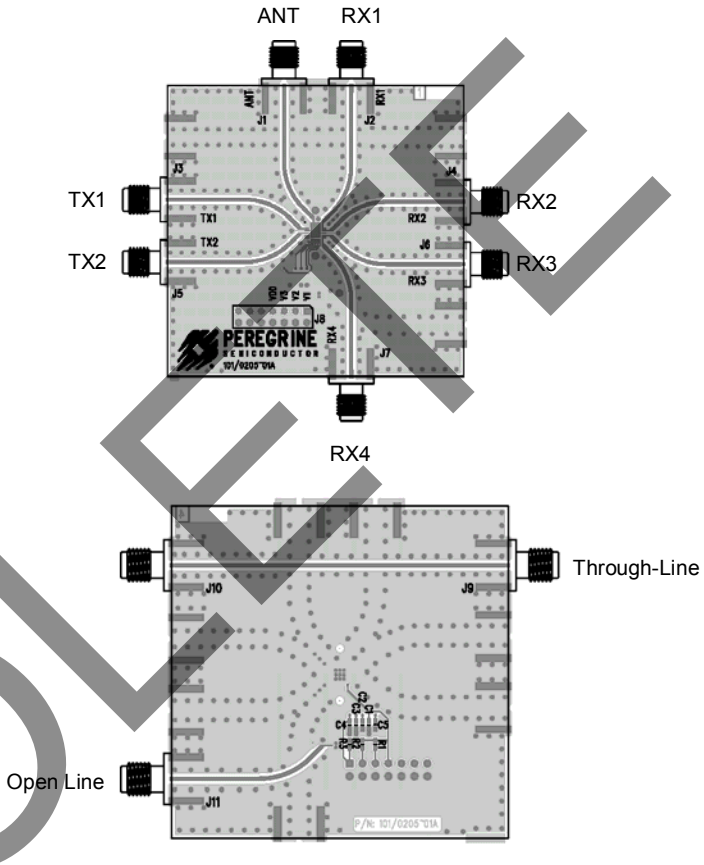
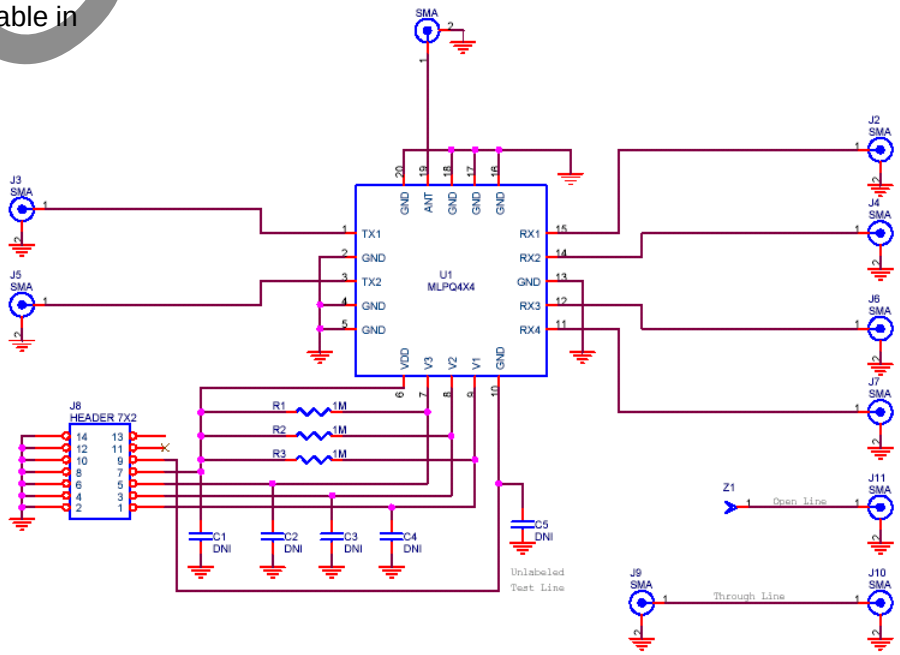


Figure 5. Evaluation Board Schematic
Peregrine Specification 102/0267



Typical Performance Data @ V_{DD} = 2.6 V, 25 °C (Unless otherwise noted)

Figure 6. Insertion Loss: All Ports

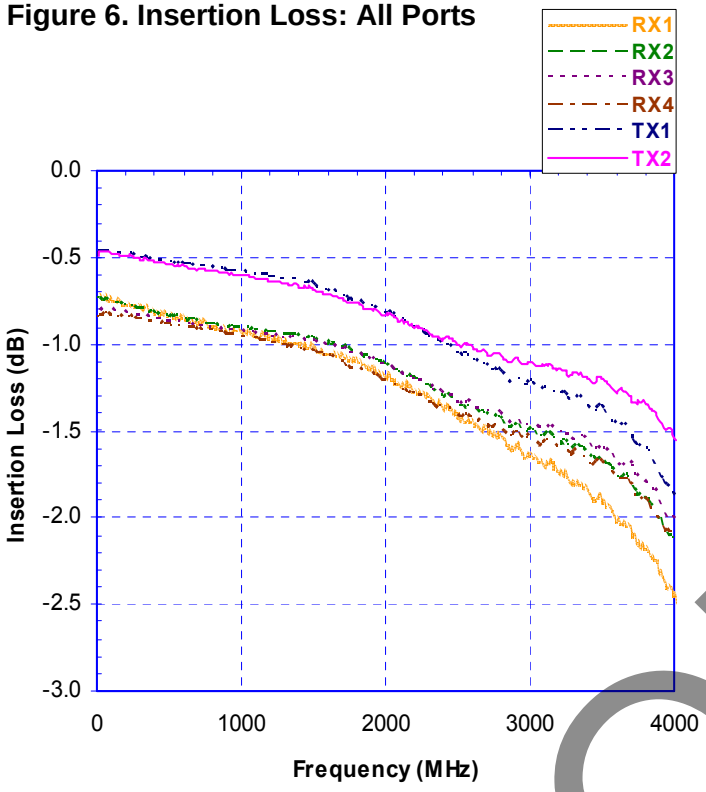


Figure 7. Insertion Loss: TX Over V_{DD}

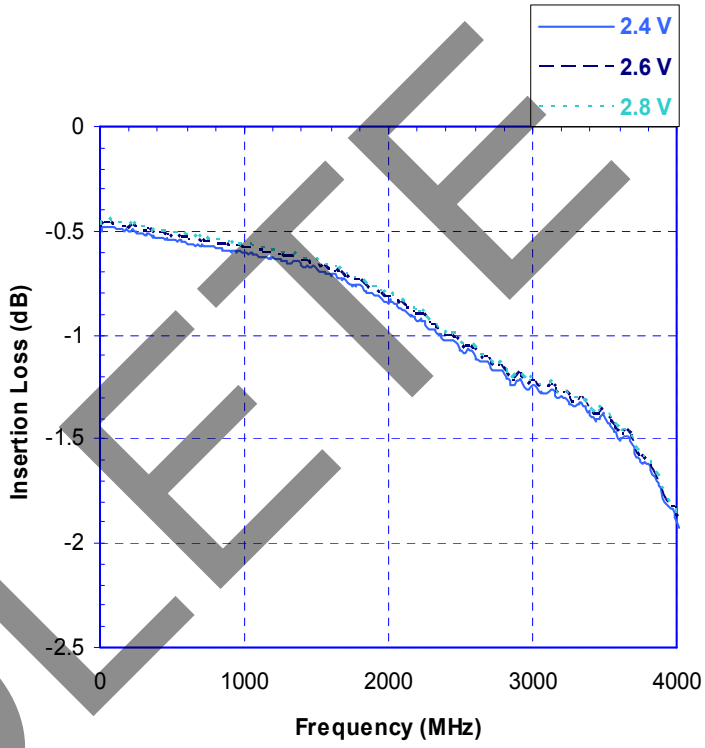


Figure 8. Insertion Loss: TX Over Temp

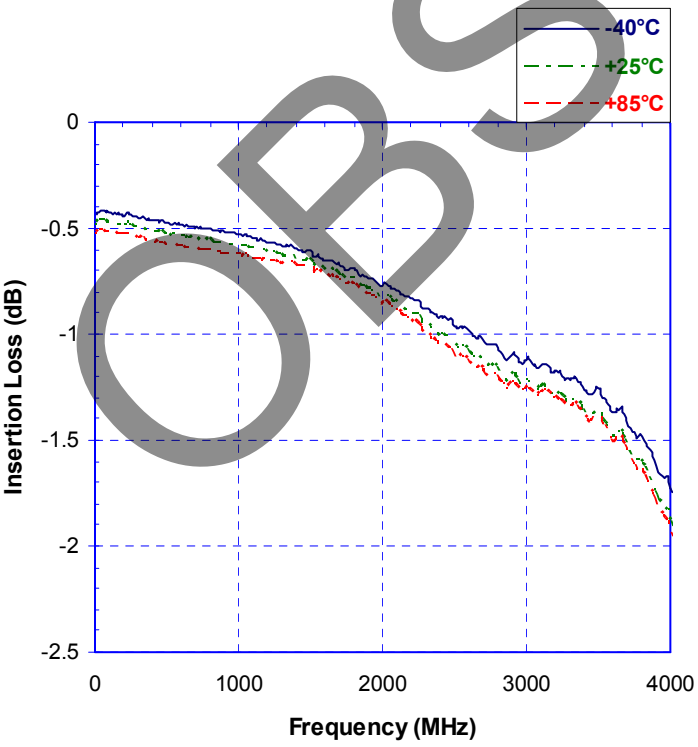
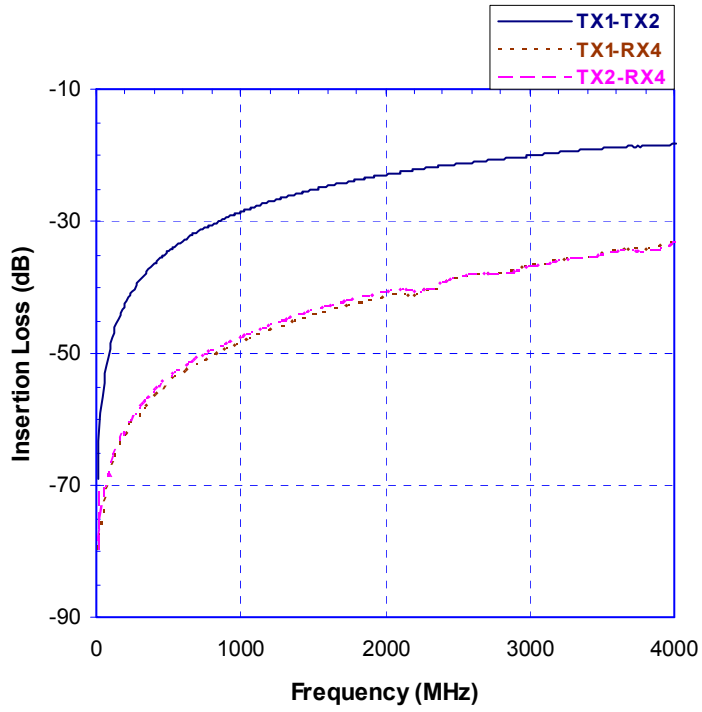


Figure 9. Isolation: Worst Case Paths



Typical Performance Data @ V_{DD} = 2.6 V, 25 °C (Unless otherwise noted)°

Figure 10. Return Loss: Worse Case Paths

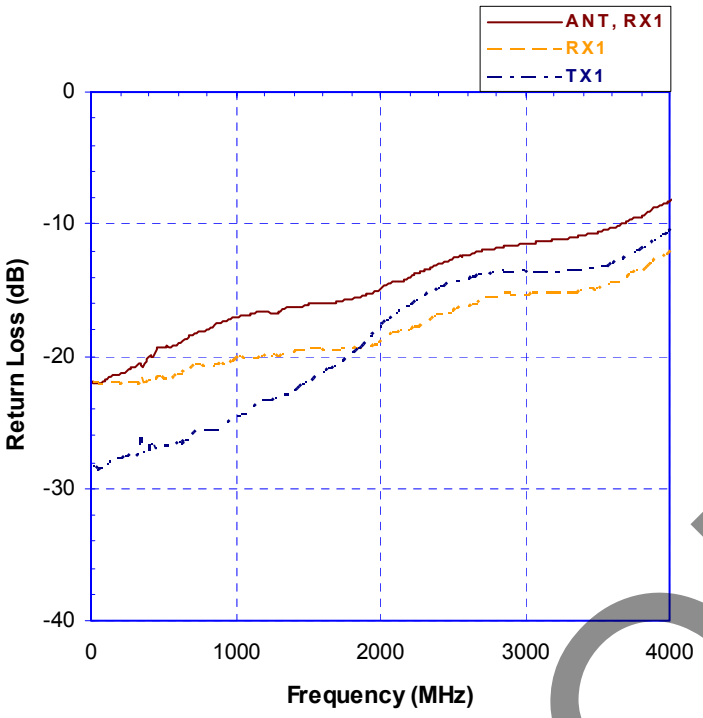


Figure 11. TX Harmonics 915MHz Over V_{DD}

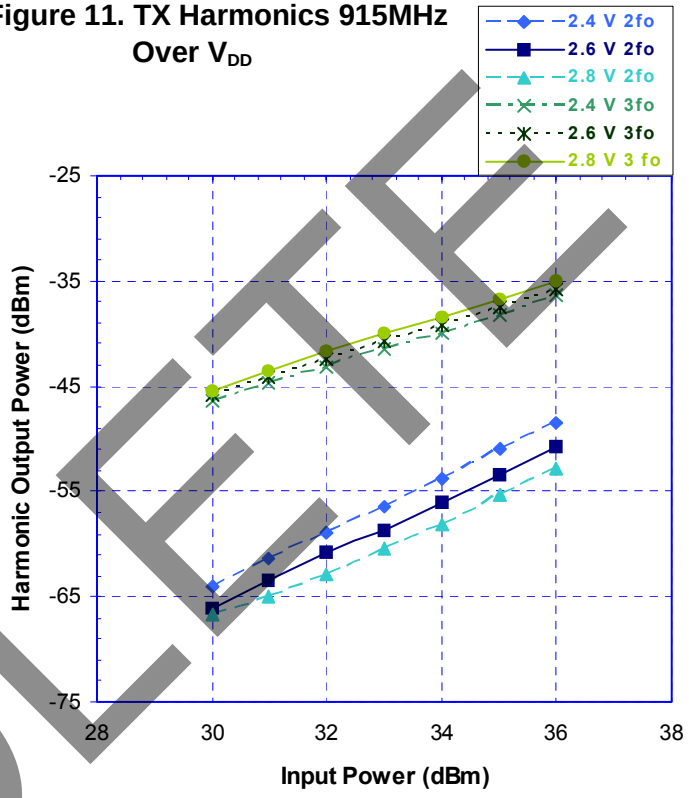


Figure 12. TX Harmonics 915MHz Over Temp

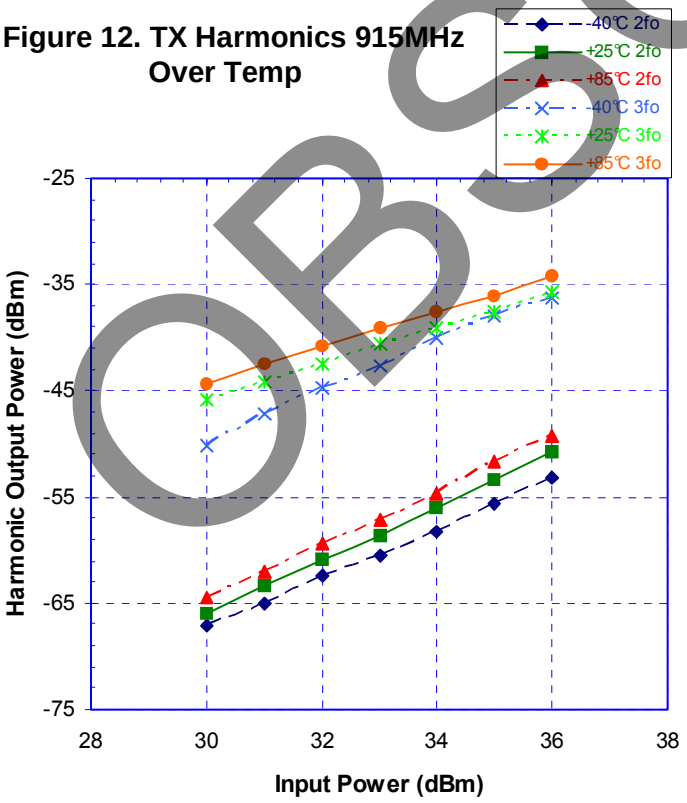
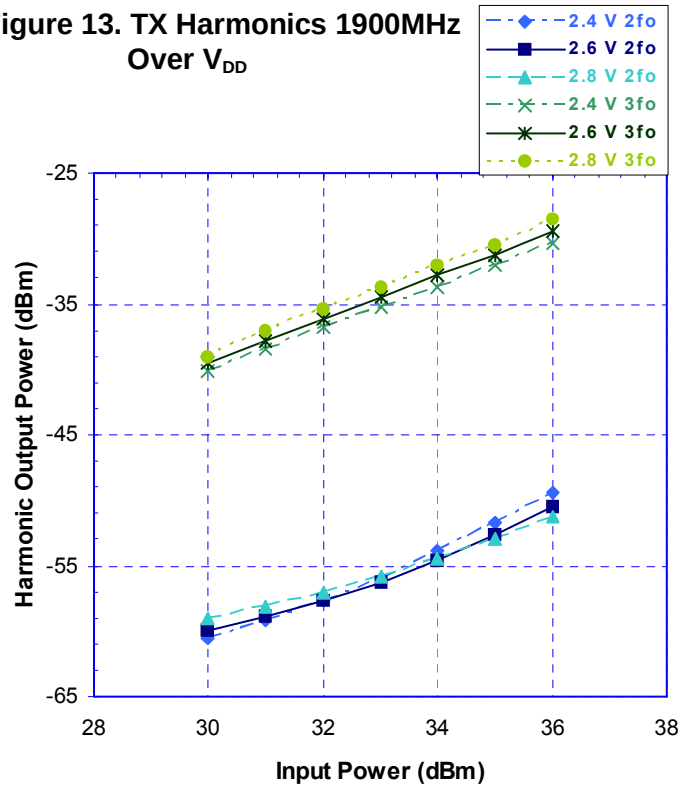


Figure 13. TX Harmonics 1900MHz Over V_{DD}



Typical Performance Data @ V_{DD} = 2.6 V, 25 °C (Unless otherwise noted)

Figure 14. TX Harmonics 1900MHz Over Temp

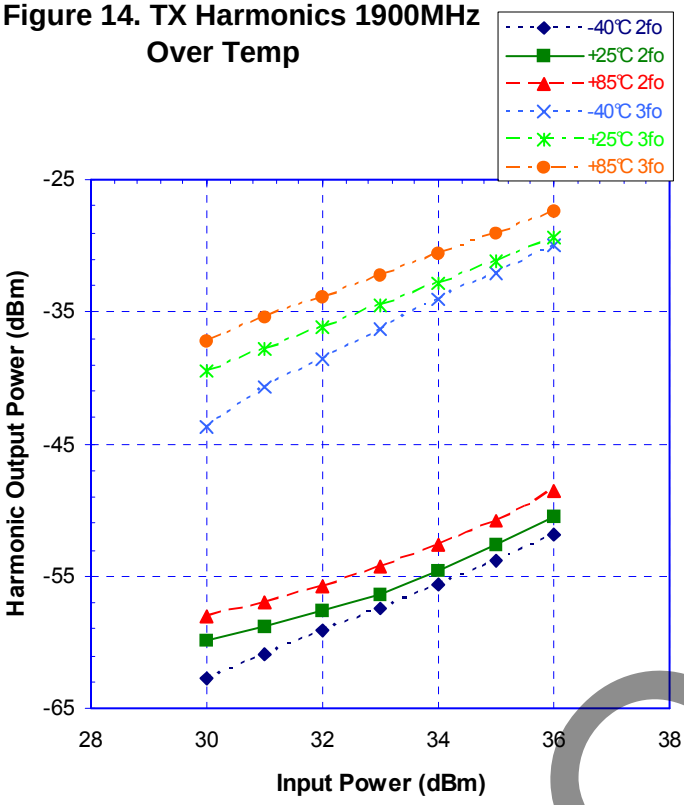
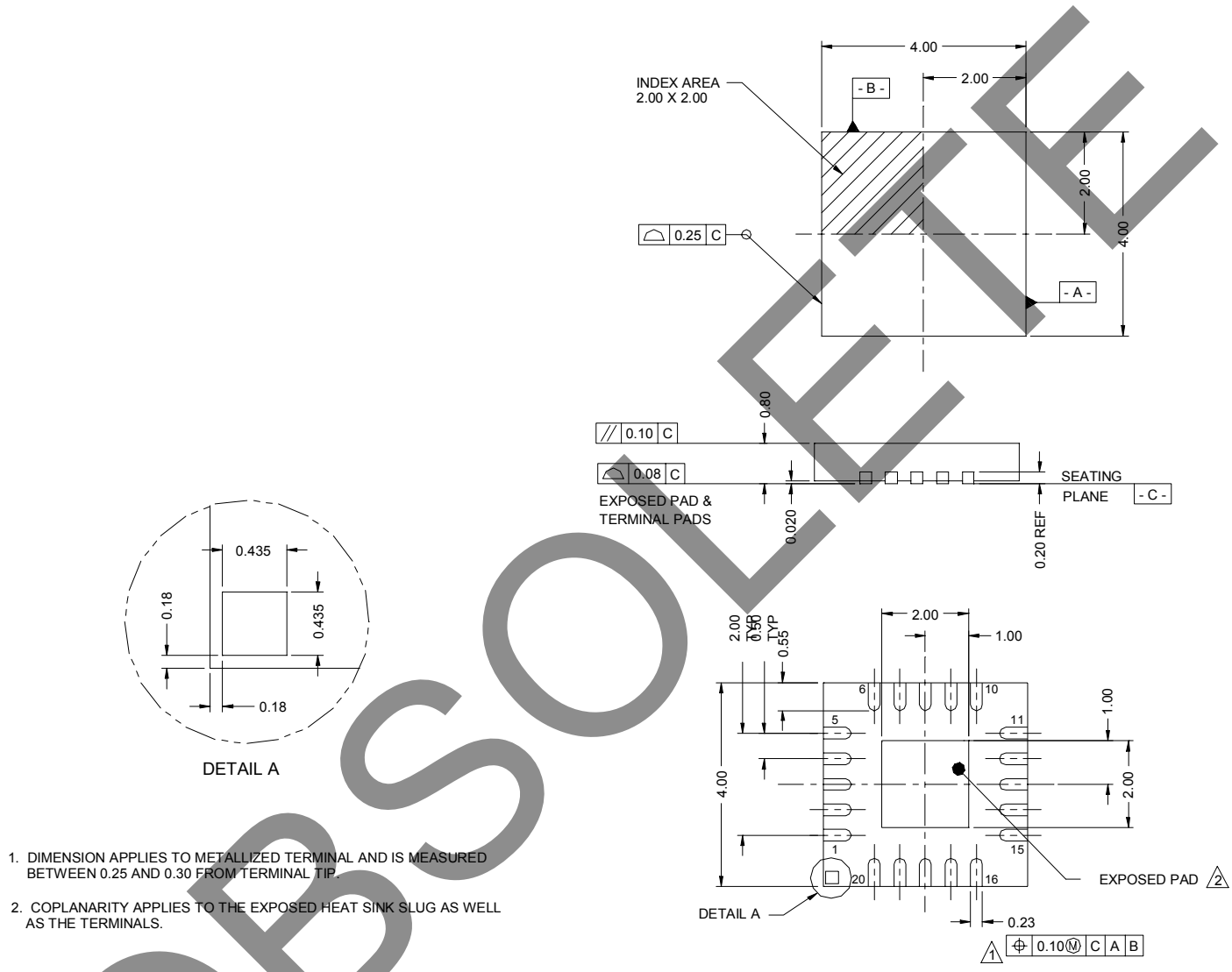


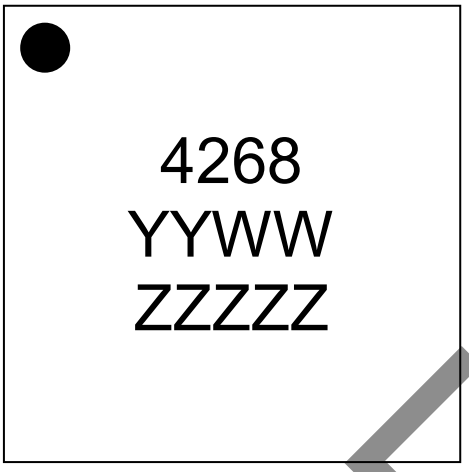
Figure 15. Package Drawing (mm)

20-lead 4x4 mm QFN



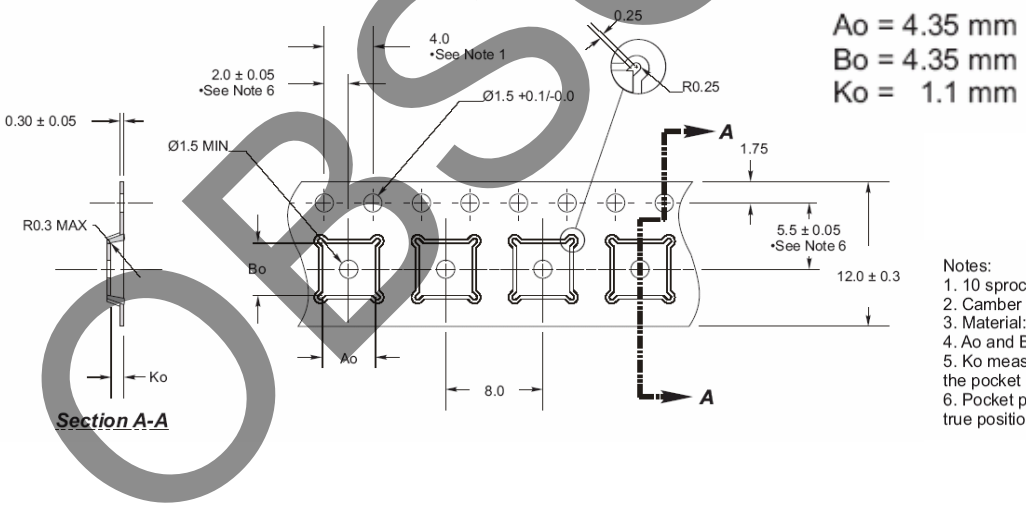
1. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 FROM TERMINAL TIP.
2. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 16. Marking Specification



YYWW = Date Code (Year, Work Week)
ZZZZZ = Last five digits of PSC Lot Number

Figure 17. Tape and Reel Drawing

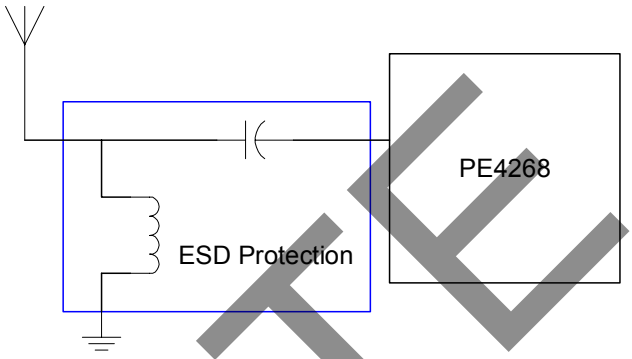


Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

ESD Protection Circuit

Handset products must tolerate large ESD surges at the antenna interface without damage. The IEC 61000-4-2 standard specifies both 8 kV contact and 16 kV air discharges that typical handsets must survive. By itself, the PE4268 offers protection to 1.5 kV but with the addition of two inexpensive passive components, the switch can meet the levels as specified in the IEC spec. Figure 18 is the suggested solution for compliance with the IEC standards.

Figure 18. ESD Protection Circuit



L = 27 nH (muRata: LQG1127NJ00),

C = 33 pF (muRata: GRM33C0G330J50)

Table 6. PE4268 Antenna Application Test Results (C=150 pF, R=330 Ω, IEC 61000-4-2 Standard)

Test Condition	Results
+8 kV contact discharge, 10 times with 1s intervals	Pass
-8 kV contact discharge, 10 times with 1s intervals	Pass
+16 kV air discharge, 10 times with 1s intervals	Pass
-16 kV air discharge, 10 times with 1s intervals	Pass

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4268-01	4268	PE4268-20QFN 4x4mm-75A	20-lead 4x4mm QFN	75 units / Tube
4268-02	4268	PE4268-20QFN 4x4mm-3000C	20-lead 4x4mm QFN	3000 units / T&R
4268-00	PE4268-EK	PE4268-20QFN 4x4mm-EK	Evaluation Kit	1 / Box
4268-51	4268	PE4268G-20QFN 4x4mm-75A	Green 20-lead 4x4mm QFN	75 units / Tube
4268-52	4268	PE4268G-20QFN 4x4mm-3000C	Green 20-lead 4x4mm QFN	3000 units / T&R

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Data Sheet Identification

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