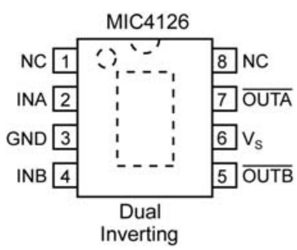
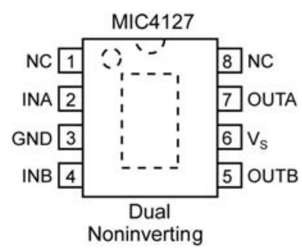
Ordering Information

Part Number	Configuration	Package	Junction Temp. Range[1]	Lead Finish
MIC4126YME	Dual Inverting	EPAD 8-lead SOIC	–40° to +125°C	Pb-Free
MIC4126YMME	Dual Inverting	EPAD 8-lead MSOP	–40° to +125°C	Pb-Free
MIC4126YML	Dual Inverting	8-lead MLF	–40° to +125°C	Pb-Free
MIC4127YME	Dual Non-inverting	EPAD 8-lead SOIC	–40° to +125°C	Pb-Free
MIC4127YMME	Dual Non-inverting	EPAD 8-lead MSOP	–40° to +125°C	Pb-Free
MIC4127YML	Dual Non-inverting	8-lead MLF	–40° to +125°C	Pb-Free
MIC4128YME	Inverting + Non-inverting	EPAD 8-lead SOIC	–40° to +125°C	Pb-Free
MIC4128YMME	Inverting + Non-inverting	EPAD 8-lead MSOP	–40° to +125°C	Pb-Free
MIC4128YML	Inverting + Non-inverting	8-lead MLF	–40° to +125°C	Pb-Free

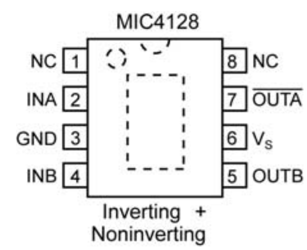
Pin Configuration



EPAD SOIC-8L (ME)
EPAD MSOP-8L (MME)
MLF-8L (ML)



EPAD SOIC-8L (ME)
EPAD MSOP-8L (MME)
MLF-8L (ML)



EPAD SOIC-8L (ME)
EPAD MSOP-8L (MME)
MLF-8L (ML)

Pin Description

Pin Number	Pin Name	Pin Function
1, 8	NC	Not internally connected
2	INA	Control Input A: TTL/CMOS compatible logic input
3	GND	Ground
4	INB	Control Input B: TTL/CMOS compatible logic input.
5	OUTB	Output B: CMOS totem-pole output.
6	V_S	Supply Input: +4.5V to +20V
7	OUTA	Output A: CMOS totem-pole output.
EP	GND	Ground, backside pad.

Absolute Maximum Ratings [1]

Supply Voltage (V_S)........................+24V
Input Voltage (V_{IN})..........V_S + 0.3V to GND – 5V
Junction Temperature (T_J) .... 150°C
Storage Temperature..............–65°C to +150°C
Lead Temperature (10 sec.) .... 300°C
ESD Rating, **Note 3**

Operating Ratings [2]

Supply Voltage (V_S) .... +4.5V to +20V
Temperature Range (T_J).......... –40°C to +125°C
Package Thermal Resistance
3X3 MLF™ θ_{JA} .... 60°C/W
EPAD MSOP-8L θ_{JA} .... 60°C/W
EPAD SOIC-8L θ_{JA} .... 58°C/W

Electrical Characteristics [4]

4.5V ≤ V_S ≤ 20V; Input voltage slew rate >1V/µs; C_{OUT} = 1000pF. T_A = 25°C, **bold** values indicate full specified temperature range; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Input						
V_{IH}	Logic 1 Input Voltage		2.4 **2.4**	1.4 **1.6**		V
V_{IL}	Logic 0 Input Voltage			1.1 **1.3**	0.8 **0.8**	V
I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	**–1**		**1**	µA
Output						
V_{OH}	High Output Voltage		**V_S–0.025**			V
V_{OL}	Low Output Voltage				**0.025**	V
R_O	Output Resistance	I_{OUT} = 10mA, V_S = 20V		6 **8**	10 **12**	Ω
I_{PK}	Peak Output Current			**1.5**		A
I	Latch-Up Protection	Withstand reverse current	**>200**			mA
Switching Time						
t_R	Rise Time	Test Figure 1		13 **20**	30 **40**	ns
t_F	Fall Time	Test Figure 1		15 **18**	25 **40**	ns
t_{D1}	Delay Time	Test Figure 1		37 **43**	50 **60**	ns
t_{D2}	Delay Time	Test Figure 1		40 **45**	60 **70**	ns
Power Supply						
I_S	Power Supply Current	V_{INA} = V_{INB} = 3.0V		1.4 **1.5**	4.5 **8**	mA
I_S	Power Supply Current	V_{INA} = V_{INB} = 0.0V		0.18 **0.19**	0.4 **0.6**	mA

Notes:
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5kΩ in series with 100pF.
4. Specification for packaged product only.

Test Circuit

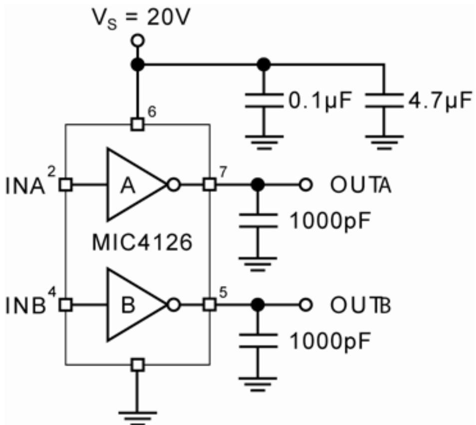


Figure 1a. Inverting Configuration

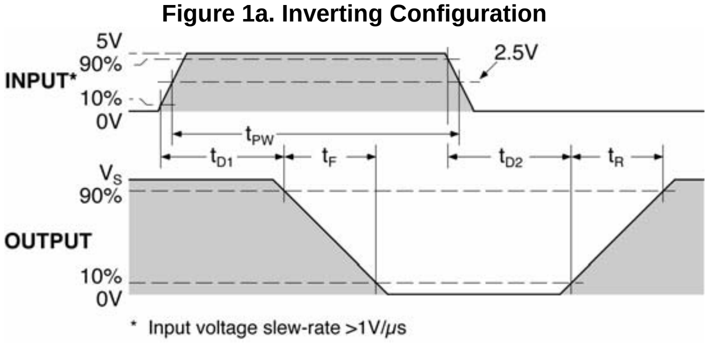


Figure 1b. Inverting Timing

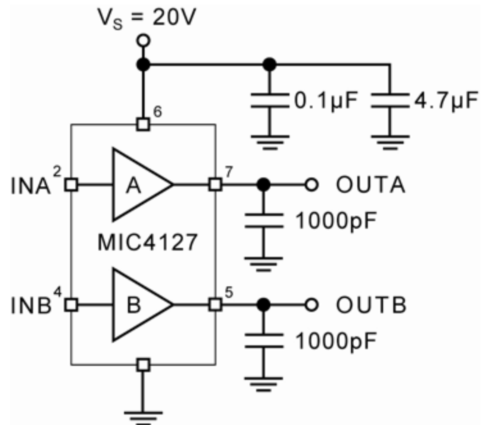


Figure 2a. Non-inverting Configuration

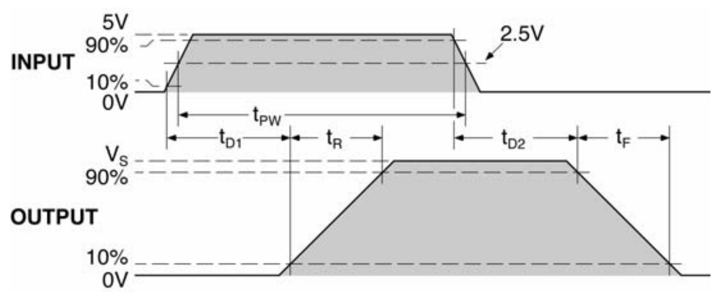
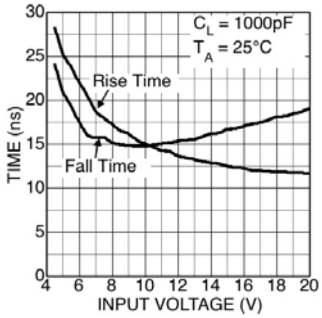


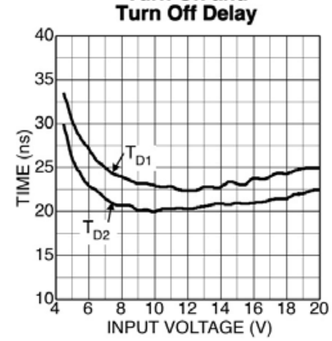
Figure 2b. Non-inverting Timing

Typical Characteristics

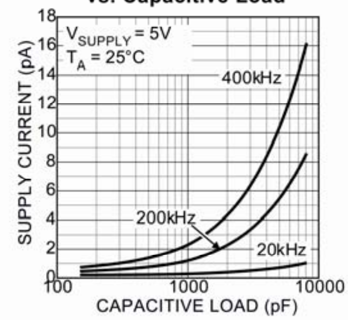
Rise and Fall Time



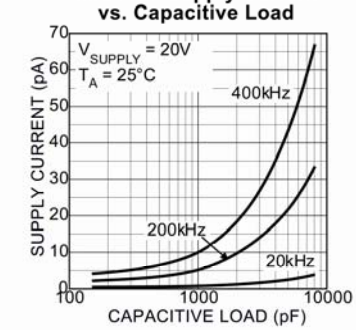
Turn On and Turn Off Delay



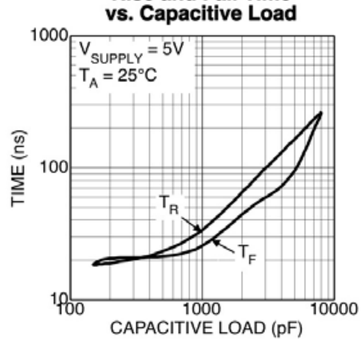
MIC4127 Supply Current vs. Capacitive Load



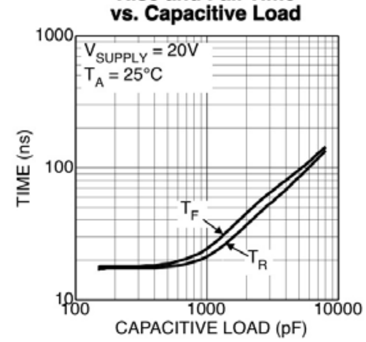
MIC4127 Supply Current vs. Capacitive Load



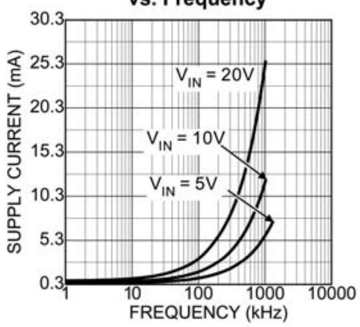
Rise and Fall Time vs. Capacitive Load



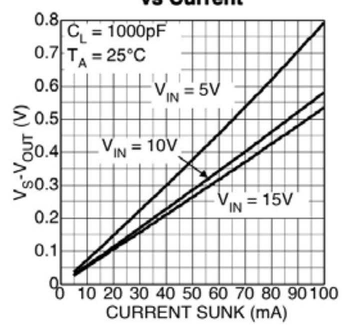
Rise and Fall Time vs. Capacitive Load



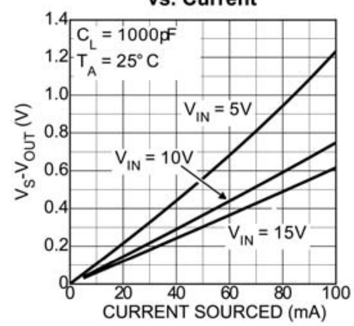
Supply Current vs. Frequency



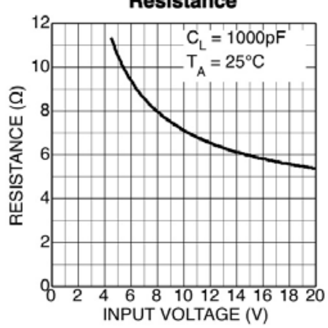
Low Output vs Current



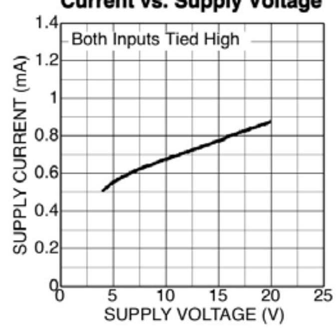
High Output vs. Current



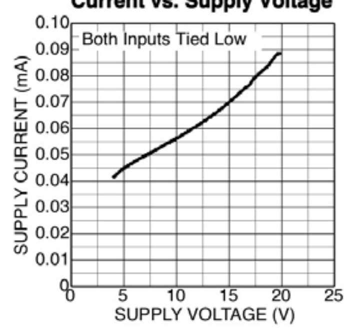
MIC4126 Output Resistance



Quiescent Power Supply Current vs. Supply Voltage



Quiescent Power Supply Current vs. Supply Voltage



Application Information

Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, changing a 1000pF load by 16V in 25ns requires 0.8A from the supply input.

To guarantee low supply impedance over a wide frequency range, parallel capacitors are recommended for power supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (< 0.5") should be used. A 1.0µF film capacitor in parallel with one or two 0.1µF ceramic MLC capacitors normally provides adequate bypassing.

Grounding

When using the inverting drivers in the MIC4126 or MIC4128, individual ground returns for the input and output circuits or a ground plane are recommended for optimum switching speed. The voltage drop that occurs between the driver's ground and the input signal ground, during normal high-current switching, will behave as negative feedback and degrade switching speed.

The E-pad and MLF packages have an exposed pad under the package. It's important for good thermal performance that this pad is connected to a ground plane.

Control Input

Unused driver inputs must be connected to logic high (which can be V_S) or ground. For the lowest quiescent current (< 500µA), connect unused inputs-to-ground. A logic-high signal will cause the driver to draw up to 9mA.

The control input voltage threshold is approximately 1.5V. The control input recognizes 1.5V up to V_S as a logic high and draws less than 1µA within this range.

Power Dissipation

Power dissipation should be calculated to make sure that the driver is not operated beyond its thermal ratings. Quiescent power dissipation is negligible. A practical value for total power dissipation is the sum of the dissipation caused by the load and the transition power dissipation ($P_L + P_T$).

Load Dissipation

Power dissipation caused by continuous load current (when driving a resistive load) through the driver's output resistance is:

$$P_L = I_L^2 R_O$$

For capacitive loads, the dissipation in the driver is:

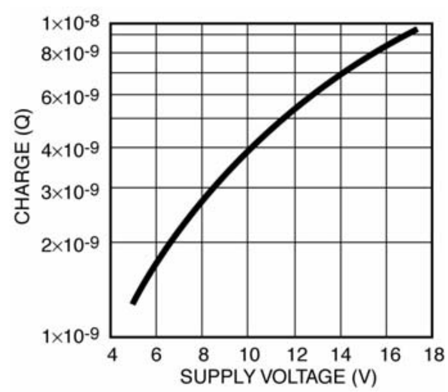
$$P_L = f C_L V_S^2$$

Transition Dissipation

In applications switching at a high frequency, transition power dissipation can be significant. This occurs during switching transitions when the P-channel and N-channel output FETs are both conducting for the brief moment when one is turning on and the other is turning off.

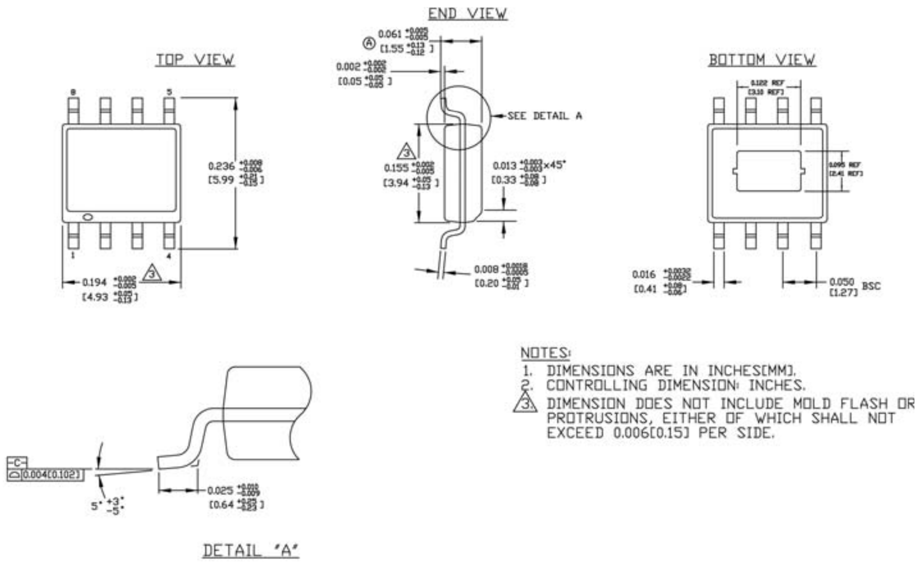
$$P_T = 2 f V_S Q$$

Charge (Q) is read from the following graph:

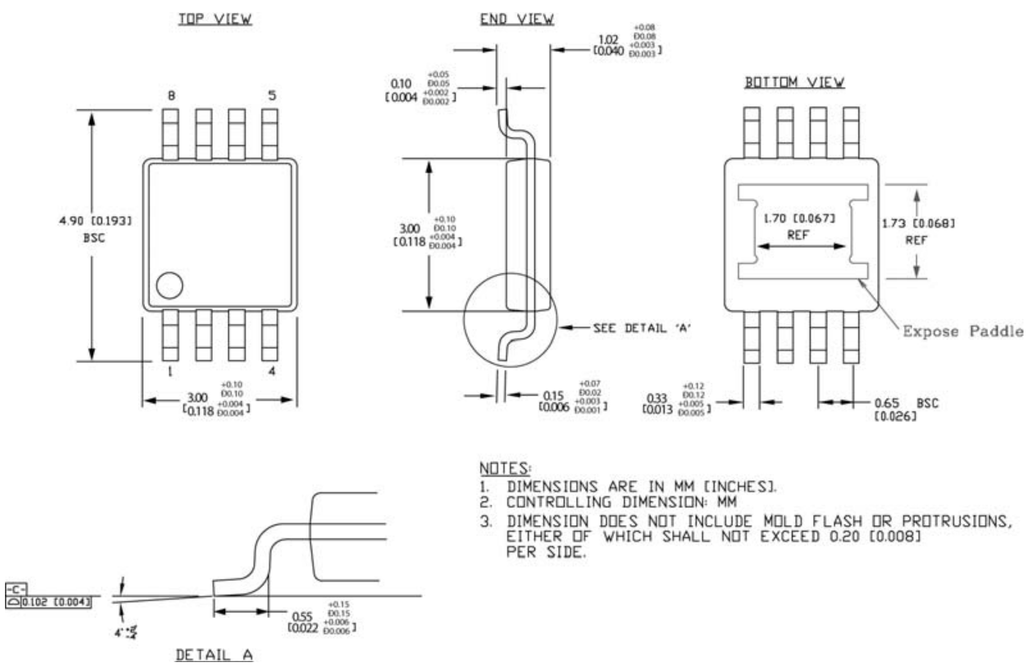


Crossover Energy Loss per Transition

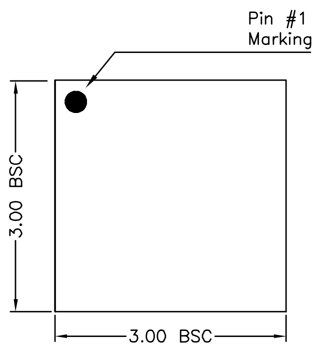
Package Information



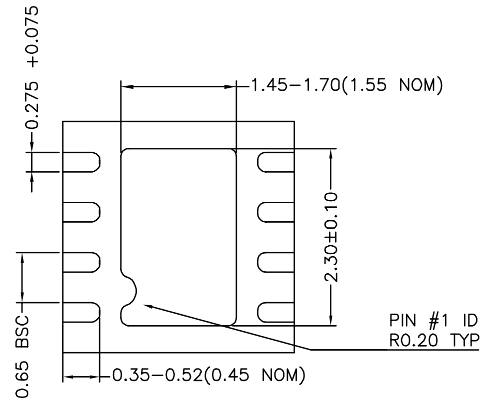
8-Pin Exposed Pad SOIC (M)



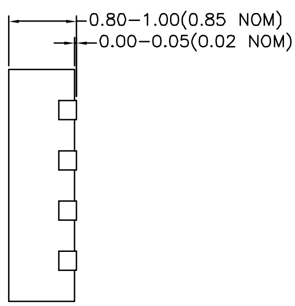
8-Pin Exposed Pad MSOP (MM)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

8-Pin MLF (ML)

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