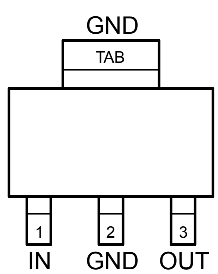
Ordering Information

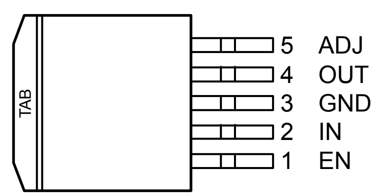
Part Number		Voltage	Temperature Range	Package
Standard	Pb-Free / RoHS Compliant			
MIC37100-1.5BS	MIC37100-1.5WS*	1.5V	–40° to +125°C	SOT-223
MIC37100-1.65BS	MIC37100-1.65WS*	1.65V	–40° to +125°C	SOT-223
MIC37100-1.8BS	MIC37100-1.8WS*	1.8V	–40° to +125°C	SOT-223
MIC37100-2.5BS	MIC37100-2.5WS*	2.5V	–40° to +125°C	SOT-223
MIC37100-3.3BS	MIC37100-3.3WS*	3.3V	–40° to +125°C	SOT-223
MIC37101-1.5BM	MIC37101-1.5YM	1.5V	–40° to +125°C	8-Pin SOIC
MIC37101-1.65BM	MIC37101-1.65YM	1.65V	–40° to +125°C	8-Pin SOIC
MIC37101-1.8BM	MIC37101-1.8YM	1.8V	–40° to +125°C	8-Pin SOIC
Contact Factory	MIC37101-2.1YM	2.1V	–40° to +125°C	8-Pin SOIC
MIC37101-2.5BM	MIC37101-2.5YM	2.5V	–40° to +125°C	8-Pin SOIC
MIC37101-3.3BM	MIC37101-3.3YM	3.3V	–40° to +125°C	8-Pin SOIC
MIC37102BM	MIC37102YM	Adj.	–40° to +125°C	8-Pin SOIC
MIC37102BR	MIC37102WR*	Adj.	–40° to +125°C	5-Pin S-PAK

* RoHS compliant with 'high-melting solder' exemption.

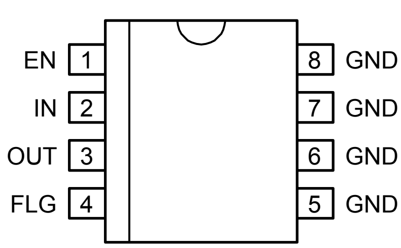
Pin Configuration



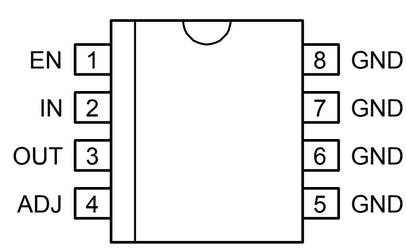
SOT-223 (S)
MIC37100-x.x (Fixed)



5-Pin S-PAK (R)
MIC37102 (Adjustable)



8-Pin SOIC
MIC37101-x.x (Fixed)



8-Pin SOIC
MIC37102 (Adjustable)

Pin Description

Pin Number MIC37100 SOT-223	Pin Number MIC37101 SOIC-8	Pin Number MIC37102 SOIC-8	Pin Number MIC37102 S-PAK	Pin Name	Pin Description
–	1	1	1	EN	Enable (Input): CMOS-compatible control input. Logic high = enable, logic low or open = shutdown.
1	2	2	2	IN	Supply (Input).
3	3	3	4	OUT	Regulator Output.
–	4	–	–	FLG	Flag (Output): Open-collector error flag output. Active low = output under voltage.
–	–	4	5	ADJ	Adjustment Input: Feedback input. Connect to resistive voltage-divider network.
2, TAB	5–8	5–8	3, TAB	GND	Ground.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) .... 0V to +6.5V
Enable Voltage (V_{EN}) .... +6.5V
Lead Temperature (soldering, 5 sec.) .... 260°C
Storage Temperature (T_s) .... –65°C to +150°C
ESD Rating[3]

Operating Ratings[2]

Supply Voltage (V_{IN}) .... +2.25V to +6V
Enable Voltage (V_{EN}) .... 0V to +6V
Maximum Power Dissipation ($P_{D(max)}$)[4]
Junction Temperature (T_J) .... –40°C to +125°C
Package Thermal Resistance
SOT-223 (θ_{JC}) .... 15°C/W
SOIC-8 (θ_{JC}) .... 20°C/W
S-PAK-5 (θ_{JC}) .... 2°C/W

Electrical Characteristics

$V_{IN} = V_{OUT} + 1V$; $V_{EN} = 2.25V$; $T_J = 25°C$, **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted.

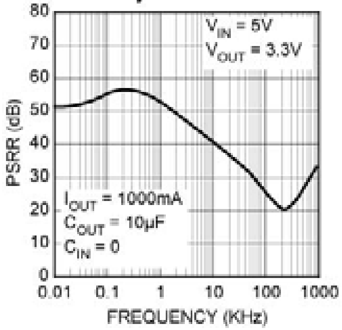
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage	10mA 10mA ≤ I_{OUT} ≤ 1A, V_{OUT} + 1V ≤ V_{IN} ≤ 6V	–1 **–2**		1 **2**	% %
	Line Regulation	I_{OUT} = 10mA, V_{OUT} + 1V ≤ V_{IN} ≤ 6V		0.06	0.5	%
	Load Regulation	V_{IN} = V_{OUT} + 1V, 10mA ≤ I_{OUT} ≤ 1A		0.2	1	%
$\Delta V_{OUT}/\Delta T$	Output Voltage Temp. Coefficient[6]			40		pm/°C
V_{DO}	Dropout Voltage[6]	I_{OUT} = 100mA, ΔV_{OUT} = –1%		125	**200**	mV
		I_{OUT} = 500mA, ΔV_{OUT} = –1%		210	**350**	mV
		I_{OUT} = 750mA, ΔV_{OUT} = –1%		250	**400**	mV
		I_{OUT} = 1A, ΔV_{OUT} = –1%		280	**500**	mV
I_{GND}	Ground Current[7]	I_{OUT} = 100mA, V_{IN} = V_{OUT} + 1V		650		µA
		I_{OUT} = 500mA, V_{IN} = V_{OUT} + 1V		3.5		mA
		I_{OUT} = 750mA, V_{IN} = V_{OUT} + 1V		6.7		mA
		I_{OUT} = 1A, V_{IN} = V_{OUT} + 1V		11	**25**	mA
$I_{OUT(lim)}$	Current Limit	V_{OUT} = 0V, V_{IN} = V_{OUT} + 1V		1.6	2.5	A
Enable Input						
V_{EN}	Enable Input Voltage	logic low (off)			**0.8**	V
		logic high (on)	**2.25**			V
I_{EN}	Enable Input Current	V_{EN} = 2.25V	1	10	**30**	µA
		V_{EN} = 0.8V			2 **4**	µA µA
Flag Output						
$I_{FLG(leak)}$	Output Leakage Current	V_{OH} = 6V		0.01	1 **2**	µA µA
$V_{FLG(do)}$	Output Low Voltage	V_{IN} = 2.250V, $I_{OL,}$ = 250µA		210	**500**	mV
V_{FLG}	Low Threshold	% of V_{OUT}	93			%
	High Threshold	% of V_{OUT}			99.2	%
	Hysteresis			1		%
MIC37102 Only						
	Reference Voltage		1.228 **1.215**	1.240	1.252 **1.265**	V V
	Adjust Pin Bias Current			40	80 **120**	nA nA

Notes:

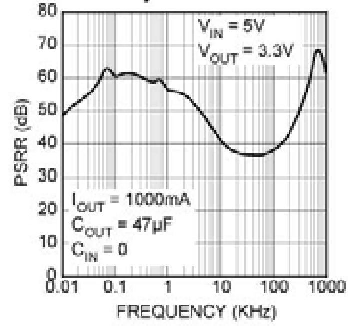
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended.
4. $P_{D(max)} = (T_{J(max)} – T_A) ÷ θ_{JA}$, where $θ_{JA}$ depends upon the printed circuit layout. See "Applications Information" section.
5. Output voltage temperature coefficient is $ΔV_{OUT}$(worst case) ÷ $(T_{J(max)} – T_{J(min)})$ where $T_{J(max)}$ is +125°C and $T_{J(min)}$ is –40°C.
6. $V_{DO} = V_{IN} – V_{OUT}$ when V_{OUT} decreases to 98% of its nominal output voltage with $V_{IN} = V_{OUT} + 1V$. For output voltages below 2.25V, dropout voltage is the input-to-output voltage differential with the minimum input voltage being 2.25V. Minimum input operating voltage is 2.25V.
7. I_{GND} is the quiescent current. $I_{IN} = I_{GND} + I_{OUT}$.
8. $V_{EN} ≤ 0.8V$, $V_{IN} ≤ 6V$, and $V_{OUT} = 0V$.

Typical Characteristics

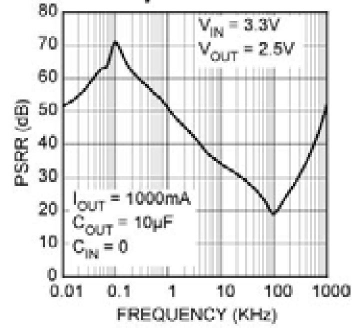
Power Supply Rejection Ratio



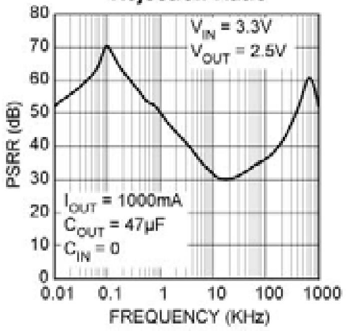
Power Supply Rejection Ratio



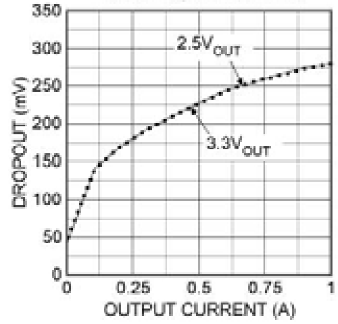
Power Supply Rejection Ratio



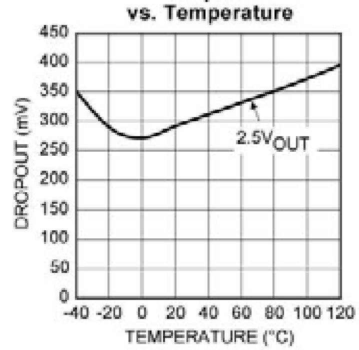
Power Supply Rejection Ratio



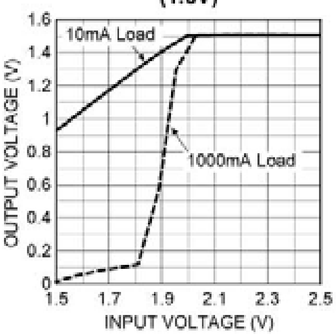
Dropout vs. Output Current



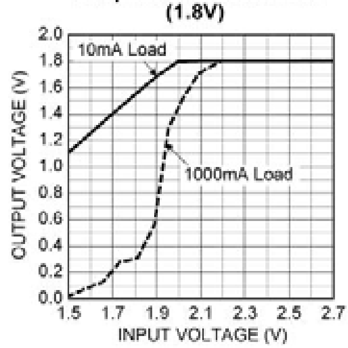
Dropout vs. Temperature



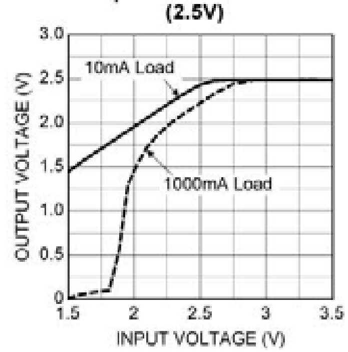
Dropout Characteristics (1.5V)



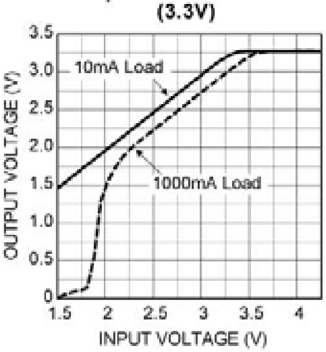
Dropout Characteristics (1.8V)



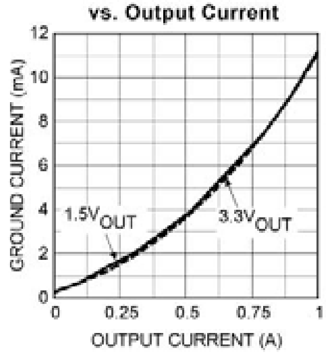
Dropout Characteristics (2.5V)



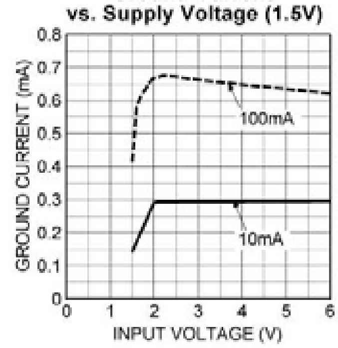
Dropout Characteristics (3.3V)



Ground Current vs. Output Current

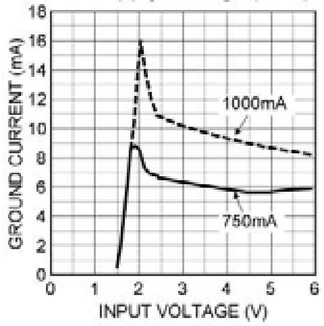


Ground Current vs. Supply Voltage (1.5V)

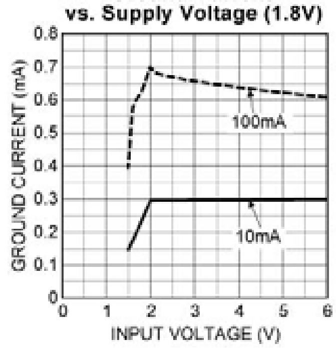


Typical Characteristics (continued)

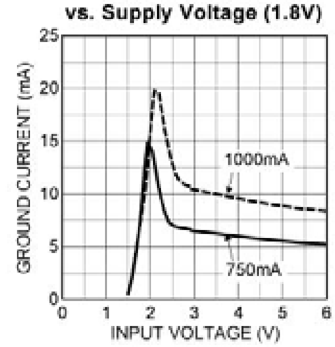
Ground Current vs. Supply Voltage (1.5V)



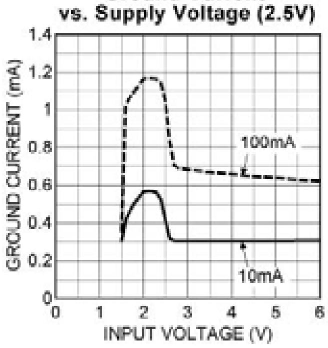
Ground Current vs. Supply Voltage (1.8V)



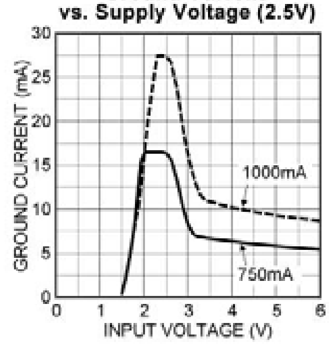
Ground Current vs. Supply Voltage (1.8V)



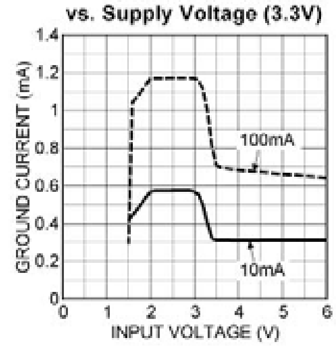
Ground Current vs. Supply Voltage (2.5V)



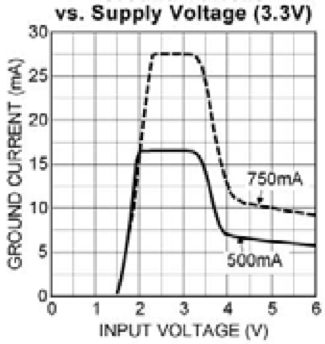
Ground Current vs. Supply Voltage (2.5V)



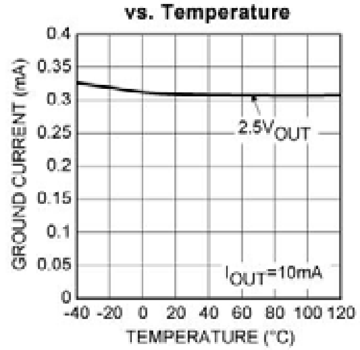
Ground Current vs. Supply Voltage (3.3V)



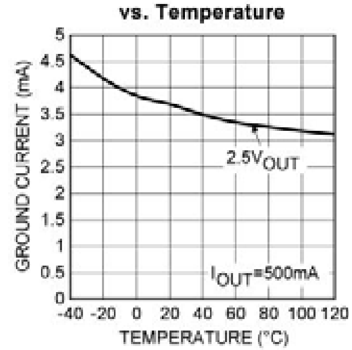
Ground Current vs. Supply Voltage (3.3V)



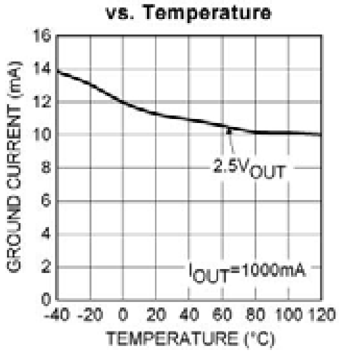
Ground Current vs. Temperature



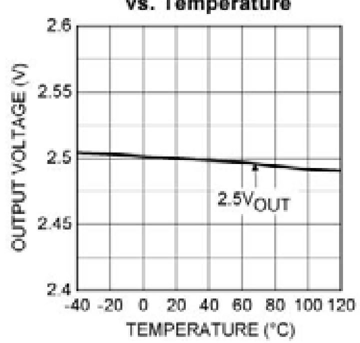
Ground Current vs. Temperature



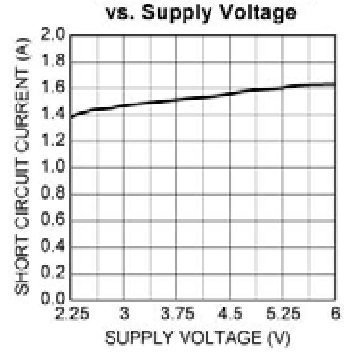
Ground Current vs. Temperature



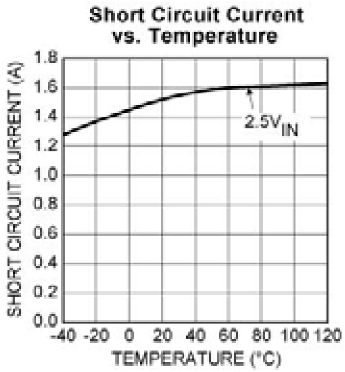
Output Voltage vs. Temperature

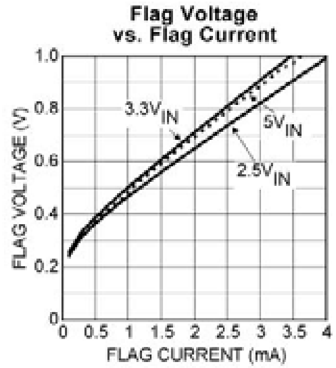


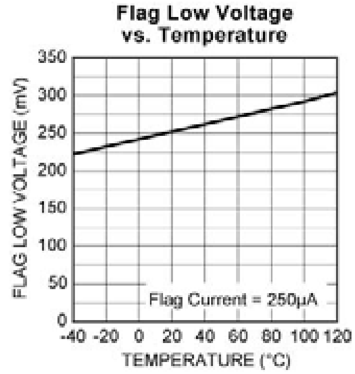
Short Circuit Current vs. Supply Voltage

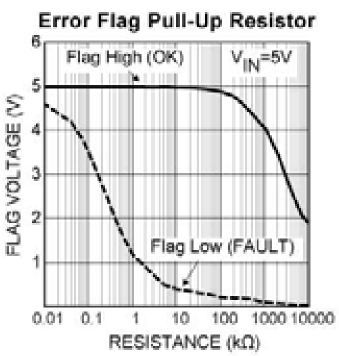


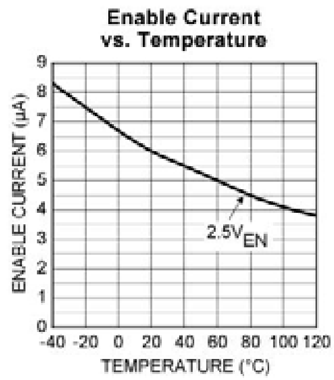
Typical Characteristics (continued)



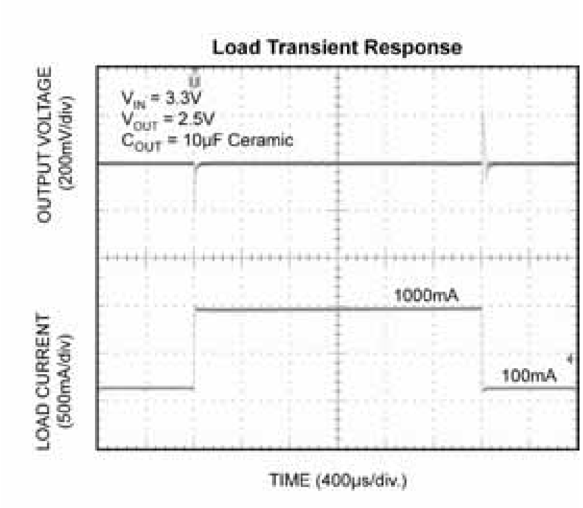


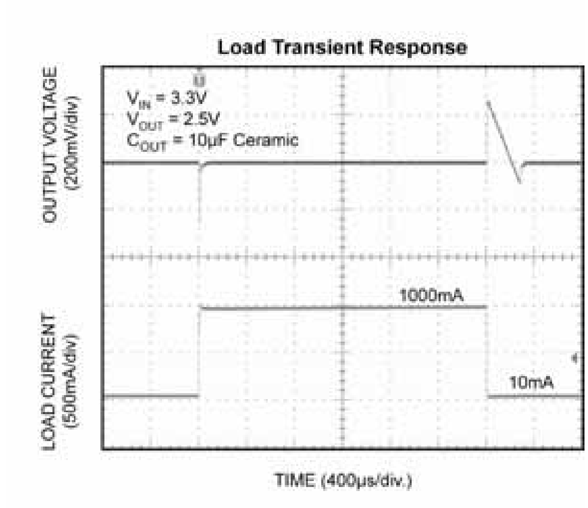


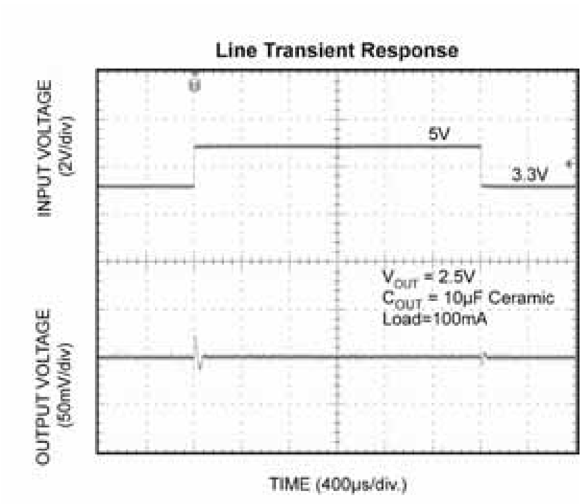


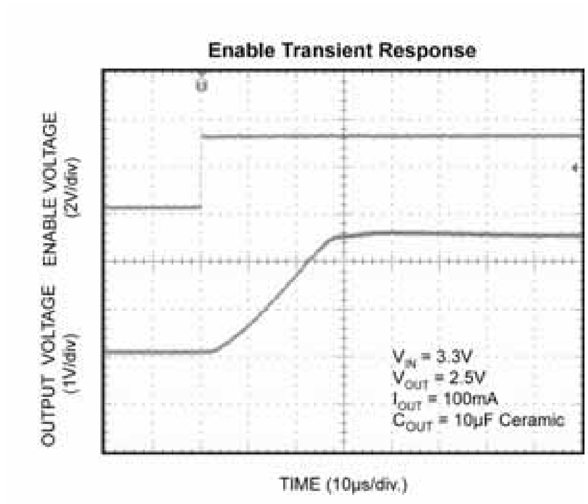


Functional Characteristics

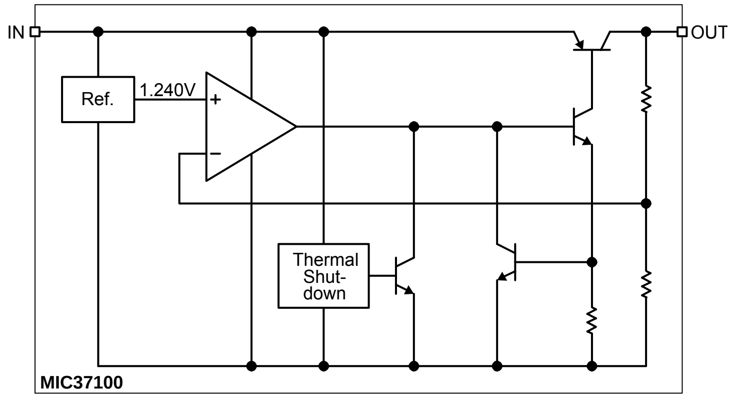




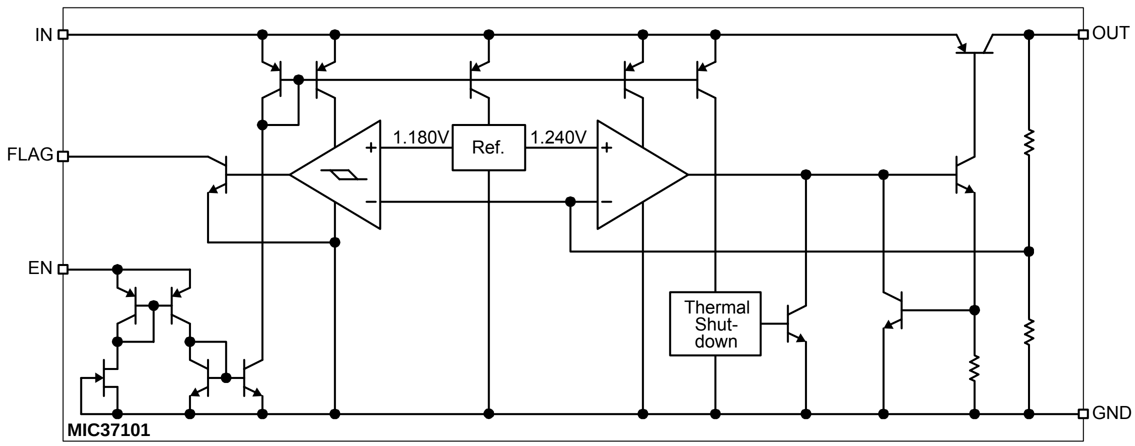




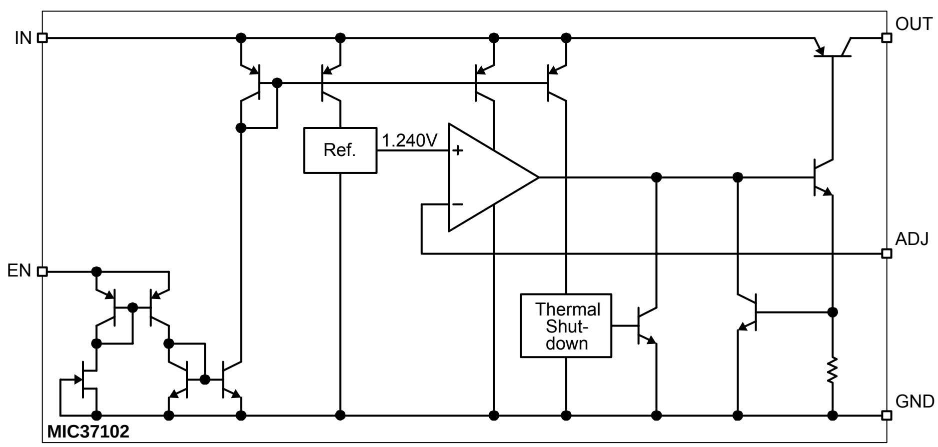
Functional Diagrams



MIC37100 Fixed Regulator Block Diagram



MIC37101 Fixed Regulator with Flag and Enable Block Diagram



MIC37102 Adjustable Regulator Block Diagram

Application Information

The MIC37100/01/02 is a high-performance low-dropout voltage regulator suitable for moderate to high-current voltage regulator applications. Its 500mV dropout voltage at full load and overtemperature makes it especially valuable in battery-powered systems and as high-efficiency noise filters in post-regulator applications. Unlike older NPN-pass transistor designs, where the minimum dropout voltage is limited by the base-to-emitter voltage drop and collector-to-emitter saturation voltage, dropout performance of the PNP output of these devices is limited only by the low VCE saturation voltage.

A trade-off for the low dropout voltage is a varying base drive requirement. Micrel's Super βeta PNP® process reduces this drive requirement to only 2% of the load current.

The MIC37100/01/02 regulator is fully protected from damage due to fault conditions. Linear current limiting is provided. Output current during overload conditions is constant. Thermal shutdown disables the device when the die temperature exceeds the maximum safe operating temperature. The output structure of these regulators allows voltages in excess of the desired output voltage to be applied without reverse current flow.

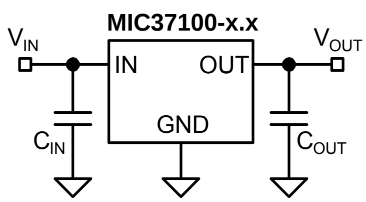


Figure 1. Capacitor Requirements

Output Capacitor

The MIC37100/01/02 requires an output capacitor to maintain stability and improve transient response. As a µCap LDO, the MIC37100/01/02 can operate with ceramic output capacitors as long as the amount of capacitance is 10µF or greater. For values of output capacitance lower than 10µF, the recommended ESR range is 200mΩ to 2Ω. The minimum value of output capacitance recommended for the MIC37100/01/02 is 4.7µF.

For 10µF or greater the ESR range recommended is less than 1Ω. Ultra-low ESR ceramic capacitors are recommended for output capacitance of 10µF or greater to help improve transient response and noise reduction at high frequency. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60% respectively over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

Input Capacitor

An input capacitor of 1µF or greater is recommended when the device is more than 4 inches away from the bulk ac supply capacitance or when the supply is a battery. Small, surface mount, ceramic chip capacitors can be used for bypassing. Larger values will help to improve ripple rejection by bypassing the input to the regulator, further improving the integrity of the output voltage.

Error Flag

The MIC37101 features an error flag (FLG), which monitors the output voltage and signals an error condition when this voltage drops 5% below its expected value. The error flag is an open-collector output that pulls low under fault conditions and may sink up to 10mA. Low output voltage signifies a number of possible problems, including an overcurrent fault (the device is in current limit) or low input voltage. The flag output is inoperative during overtemperature conditions. A pull-up resistor from FLG to either V_{IN} or V_{OUT} is required for proper operation. For information regarding the minimum and maximum values of pull-up resistance, refer to the graph in the "Typical Characteristics" section of the data sheet.

Enable Input

The MIC37101 and MIC37102 versions feature an active-high enable input (EN) that allows on-off control of the regulator. Current drain reduces to "zero" when the device is shutdown, with only microamperes of leakage current. The EN input has TTL/CMOS compatible thresholds for simple logic interfacing. EN may be directly tied to V_{IN} and pulled up to the maximum supply voltage

Transient Response and 3.3V to 2.5V or 2.5V to 1.8V, 1.65V or 1.5V Conversion

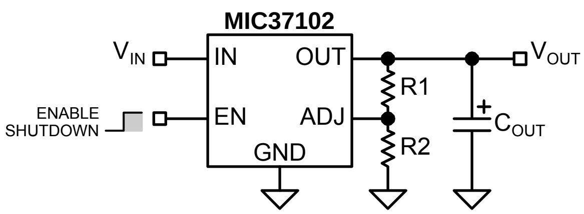
The MIC37100/01/02 has excellent transient response to variations in input voltage and load current. The device has been designed to respond quickly to load current variations and input voltage variations. Large output capacitors are not required to obtain this performance. A standard 10µF output capacitor, is all that is required. Larger values help to improve performance even further.

By virtue of its low-dropout voltage, this device does not saturate into dropout as readily as similar NPN-based designs. When converting from 3.3V to 2.5V or 2.5V to 1.8V, or lower, the NPN based regulators are already operating in dropout, with typical dropout requirements of 1.2V or greater. To convert down to 2.5V or 1.8V without operating in dropout, NPN-based regulators require an input voltage of 3.7V at the very least. The MIC37100 regulator will provide excellent performance with an input as low as 3.0V or 2.5V respectively. This gives the PNP based regulators a distinct advantage over older, NPN based linear regulators.

Minimum Load Current

The MIC37100/01/02 regulator is specified between finite loads. If the output current is too small, leakage currents dominate and the output voltage rises. A 10mA minimum load current is necessary for proper regulation.

Adjustable Regulator Design



$$V_{OUT} = 1.240V\left(1 + \frac{R1}{R2}\right)$$

Figure 2. Adjustable Regulator with Resistors

The MIC37102 allows programming the output voltage anywhere between 1.24V and the 6V maximum operating rating of the family. Two resistors are used. Resistors can be quite large, up to 1MΩ, because of the very high input impedance and low bias current of the sense comparator. The resistor values are calculated by:

$$R1 = R2\left(\frac{V_{OUT}}{1.240} - 1\right)$$

Where V_O is the desired output voltage. Figure 2 shows component definition. Applications with widely varying load currents may scale the resistors to draw the minimum load current required for proper operation (see above).

Power SOIC-8 Thermal Characteristics

One of the secrets of the MIC37101/02's performance is its power SO-8 package featuring half the thermal resistance of a standard SO-8 package. Lower thermal resistance means more output current or higher input voltage for a given package size.

Lower thermal resistance is achieved by joining the four ground leads with the die attach paddle to create a single-piece electrical and thermal conductor. This concept has been used by MOSFET manufacturers for years, proving very reliable and cost effective for the user.

Thermal resistance consists of two main elements, θ_{JC} (junction-to-case thermal resistance) and θ_{CA} (case-to-ambient thermal resistance). See Figure 3. θ_{JC} is the resistance from the die to the leads of the package. θ_{CA} is the resistance from the leads to the ambient air and it includes θ_{CS} (case-to-sink thermal resistance) and θ_{SA} (sink-to-ambient thermal resistance).

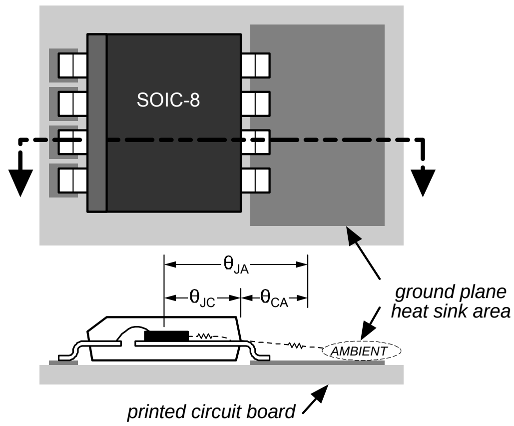


Figure 3. Thermal Resistance

Using the power SOIC-8 reduces the θ_{JC} dramatically and allows the user to reduce θ_{CA}. The total thermal resistance, θ_{JA} (junction-to-ambient thermal resistance) is the limiting factor in calculating the maximum power dissipation capability of the device. Typically, the power SOIC-8 has a θ_{JC} of 20°C/W, this is significantly lower than the standard SOIC-8 which is typically 75°C/W. θ_{CA} is reduced because pins 5 through 8 can now be soldered directly to a ground plane which significantly reduces the case-to-sink thermal resistance and sink to ambient thermal resistance.

Low-dropout linear regulators from Micrel are rated to a maximum junction temperature of 125°C. It is important not to exceed this maximum junction temperature during operation of the device. To prevent this maximum junction temperature from being exceeded, the appropriate ground plane heat sink must be used.

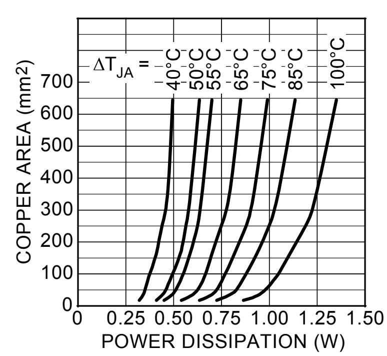


Figure 4. Copper Area vs. Power SO-8 Power Dissipation

Figure 4 shows copper area versus power dissipation with each trace corresponding to a different temperature rise above ambient.

From these curves, the minimum area of copper necessary for the part to operate safely can be determined. The maximum allowable temperature rise must be calculated to determine operation along which curve.

$$\Delta T = T_{J(max)} - T_{A(max)}$$

$$T_{J(max)} = 125°C$$

$T_{A(max)}$ = maximum ambient operating temperature.

For example, the maximum ambient temperature is 50°C, the ΔT is determined as follows:

$$\Delta T = 125°C - 50°C$$

$$\Delta T = 75°C$$

Using Figure 4, the minimum amount of required copper can be determined based on the required power dissipation. Power dissipation in a linear regulator is calculated as follows:

$$P_D = (V_{IN} - V_{OUT})\, I_{OUT} + V_{IN} \times I_{GND}$$

If we use a 2.5V output device and a 3.3V input at an output current of 1A, then our power dissipation is as follows:

$$P_D = (3.3V - 2.5V) \times 1A + 3.3V \times 11mA$$

$$P_D = 800mW + 36mW$$

$$P_D = 836mW$$

From Figure 4, the minimum amount of copper required to operate this application at a ΔT of 75°C is 160mm^2.

Quick Method

Determine the power dissipation requirements for the design along with the maximum ambient temperature at which the device will be operated. Refer to Figure 5, which shows safe operating curves for three different ambient temperatures: 25°C, 50°C and 85°C. From these curves, the minimum amount of copper can be determined by knowing the maximum power dissipation required. If the maximum ambient temperature is 50°C and the power dissipation is as above, 836mW, the curve in Figure 5 shows that the required area of copper is 160mm^2.

The θ_{JA} of this package is ideally 63°C/W, but it will vary depending upon the availability of copper ground plane to which it is attached.

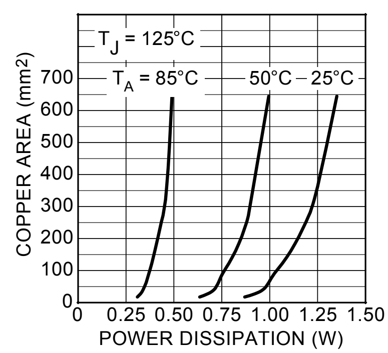
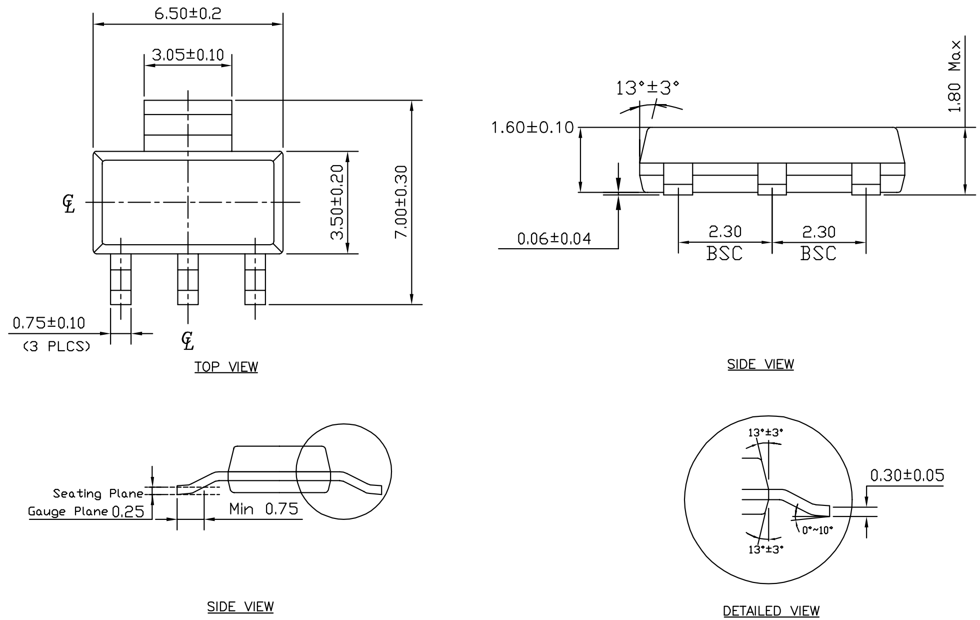


Figure 5. Copper Area vs. Power-SOIC Power Dissipation

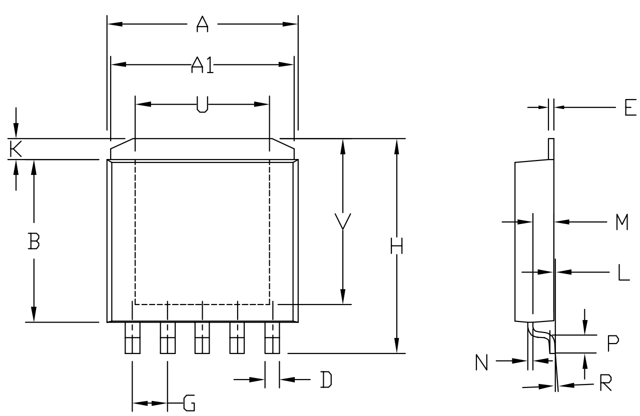
Package Information



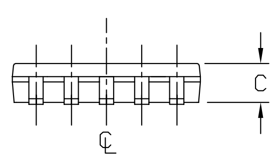
NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Controlling dimension: Millimeters.
3. Dimensions are exclusive of mold flash and gate burr.
4. All specification comply to Jedec spec TO261 Issue C.

SOT-223 (S)

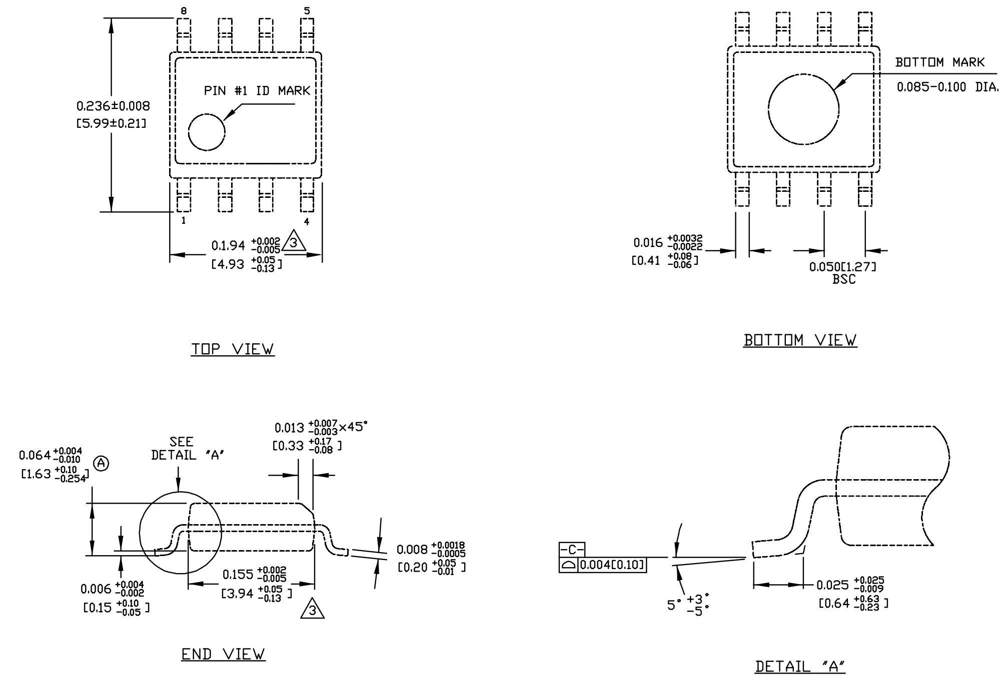


	INCHES		MILLIMETERS	
A	0.365	0.375	9.27	9.52
A1	0.350	0.360	8.89	9.14
B	0.310	0.320	7.87	8.13
C	0.070	0.080	1.78	2.03
D	0.025	0.031	0.63	0.79
E	0.010	BSC	0.25	BSC
G	0.067	BSC	1.70	BSC
H	0.410	0.420	10.41	10.67
K	0.030	0.050	0.76	1.27
L	0.001	0.005	0.03	0.13
M	0.035	0.045	0.89	1.14
N	0.010	BSC	0.25	BSC
P	0.031	0.041	0.79	1.04
R	0°	6°	0°	6°
U	0.256	BSC	6.50	BSC
V	0.316	BSC	8.03	BSC



1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. DIMENSION INCLUDES PLATING THICKNESS

5-Pin S-PAK (R)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

8-Pin SOIC (M)

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