

MCP6561/1R/1U/2/4

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

$V_{DD} - V_{SS}$	6.5V
Analog Input (V_{IN})††	$V_{SS} - 1.0V$ to $V_{DD} + 1.0V$
All Other Inputs and Outputs	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input voltage	$ V_{DD} - V_{SS} $
Output Short-Circuit Current	± 25 mA
Current at Input Pins	± 2 mA
Current at Output and Supply Pins	± 50 mA
Storage Temperature	-65°C to $+150^{\circ}\text{C}$
Ambient Temp. with Power Applied	-40°C to $+125^{\circ}\text{C}$
Junction Temp.	$+150^{\circ}\text{C}$
ESD Protection on All Pins (HBM/MM)	≥ 4 kV/300V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See [Section 4.1.2 “Input Voltage and Current Limits”](#).

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = \text{GND}$, $T_A = +25^{\circ}\text{C}$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = V_{SS}$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ (see [Figure 1-1](#)).

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Comparator	I_Q	60	100	130	μA	$I_{OUT} = 0$
Power Supply Rejection Ratio	PSRR	63	70	—	dB	$V_{CM} = V_{SS}$
Input						
Input Offset Voltage	V_{OS}	-10	± 3	+10	mV	$V_{CM} = V_{SS}$ (Note 1)
Input Offset Drift	$\Delta V_{OS}/\Delta T$	—	± 2	—	$\mu\text{V}/^{\circ}\text{C}$	$V_{CM} = V_{SS}$
Input Offset Current	I_{OS}	—	± 1	—	pA	$V_{CM} = V_{SS}$
Input Bias Current	I_B	—	1	—	pA	$T_A = +25^{\circ}\text{C}$, $V_{IN-} = V_{DD}/2$
		—	60	—	pA	$T_A = +85^{\circ}\text{C}$, $V_{IN-} = V_{DD}/2$
		—	1500	5000	pA	$T_A = +125^{\circ}\text{C}$, $V_{IN-} = V_{DD}/2$
Input Hysteresis Voltage	V_{HYST}	1.0	—	5.0	mV	$V_{CM} = V_{SS}$ (Notes 1, 2)
Input Hysteresis Linear Temp. Co.	TC_1	—	10	—	$\mu\text{V}/^{\circ}\text{C}$	
Input Hysteresis Quadratic Temp. Co.	TC_2	—	0.3	—	$\mu\text{V}/^{\circ}\text{C}^2$	
Common-Mode Input Voltage Range	V_{CMR}	$V_{SS} - 0.2$	—	$V_{DD} + 0.2$	V	$V_{DD} = 1.8V$
		$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	$V_{DD} = 5.5V$
Common-Mode Rejection Ratio	CMRR	54	66	—	dB	$V_{CM} = -0.3V$ to $V_{DD} + 0.3V$, $V_{DD} = 5.5V$
		50	63	—	dB	$V_{CM} = V_{DD}/2$ to $V_{DD} + 0.3V$, $V_{DD} = 5.5V$
		54	65	—	dB	$V_{CM} = -0.3V$ to $V_{DD}/2$, $V_{DD} = 5.5V$
Common-Mode Input Impedance	Z_{CM}	—	$10^{13} 4$	—	ΩpF	
Differential Input Impedance	Z_{DIFF}	—	$10^{13} 2$	—	ΩpF	
Push-Pull Output						
High-Level Output Voltage	V_{OH}	$V_{DD} - 0.7$	—	—	V	$I_{OUT} = -3\text{ mA}/-8\text{ mA}$ with $V_{DD} = 1.8V/5.5V$ (Note 3)
Low-Level Output Voltage	V_{OL}	—	—	0.6	V	$I_{OUT} = 3\text{ mA}/8\text{ mA}$ with $V_{DD} = 1.8V/5.5V$ (Note 3)
Short-Circuit Current	I_{SC}	—	± 30	—	mA	Note 3
Output Pin Capacitance	C_{OUT}	—	8	—	pF	

Note 1: The input offset voltage is the center of the input referred trip points. The input hysteresis is the difference between the input referred trip points.

2: V_{HYST} at different temperatures is estimated using $V_{HYST}(T_A) = V_{HYST} @ +25^{\circ}\text{C} + (T_A - 25^{\circ}\text{C}) TC_1 + (T_A - 25^{\circ}\text{C})^2 TC_2$.

3: Limit the output current to the absolute maximum rating of 50 mA.

MCP6561/1R/1U/2/4

AC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = V_{SS}$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 25\text{ pF}$ (see [Figure 1-1](#)).

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Propagation Delay						
High-to-Low, 100 mV Overdrive	t_{PHL}	—	56	80	ns	$V_{CM} = V_{DD}/2$, $V_{DD} = 1.8V$
		—	34	80	ns	$V_{CM} = V_{DD}/2$, $V_{DD} = 5.5V$
Low-to-High, 100 mV Overdrive	t_{PLH}	—	49	80	ns	$V_{CM} = V_{DD}/2$, $V_{DD} = 1.8V$
		—	47	80	ns	$V_{CM} = V_{DD}/2$, $V_{DD} = 5.5V$
Skew ⁽¹⁾	t_{PDS}	—	± 10	—	ns	
Output						
Rise Time	t_R	—	20	—	ns	
Fall Time	t_F	—	20	—	ns	
Maximum Toggle Frequency	f_{TG}	—	4	—	MHz	$V_{DD} = 5.5V$
		—	2	—	MHz	$V_{DD} = 1.8V$
Input Voltage Noise ⁽²⁾	E_{NI}	—	350	—	μV_{P-P}	10 Hz to 10 MHz

Note 1: Propagation delay skew is defined as: $t_{PDS} = t_{PLH} - t_{PHL}$.

Note 2: ENI is based on SPICE simulation.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated: $V_{DD} = +1.8V$ to $+5.5V$ and $V_{SS} = GND$.						
Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	$^\circ C$	
Operating Temperature Range	T_A	-40	—	+125	$^\circ C$	
Storage Temperature Range	T_A	-65	—	+150	$^\circ C$	
Thermal Package Resistances						
Thermal Resistance, 5-Lead SC70	θ_{JA}	—	331	—	$^\circ C/W$	
Thermal Resistance, 5-Lead SOT-23	θ_{JA}	—	220.7	—	$^\circ C/W$	
Thermal Resistance, 8-Lead SOIC	θ_{JA}	—	149.5	—	$^\circ C/W$	
Thermal Resistance, 8-Lead MSOP	θ_{JA}	—	211	—	$^\circ C/W$	
Thermal Resistance, 14-Lead SOIC	θ_{JA}	—	95.3	—	$^\circ C/W$	
Thermal Resistance, 14-Lead TSSOP	θ_{JA}	—	100	—	$^\circ C/W$	

1.2 Test Circuit Configuration

This test circuit configuration is used to determine the AC and DC specifications.

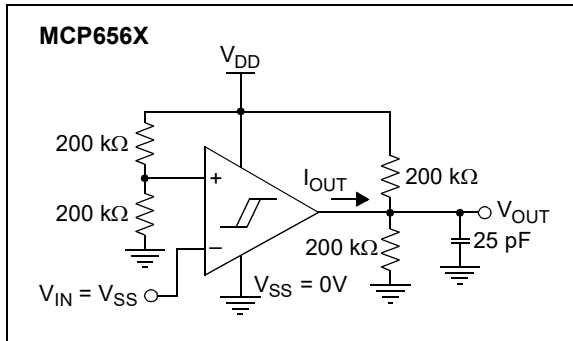


FIGURE 1-1: AC and DC Test Circuit for the Push-Pull Output Comparators.

MCP6561/1R/1U/2/4

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 25\text{ pF}$.

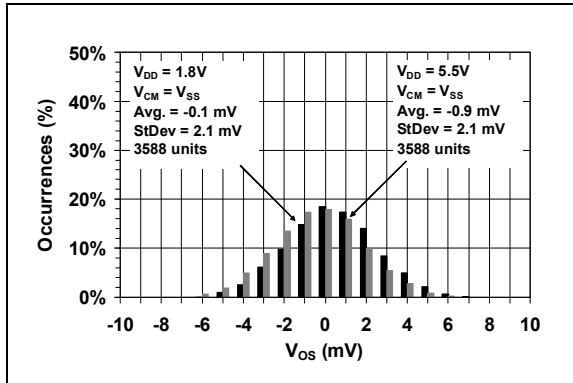


FIGURE 2-1: Input Offset Voltage.

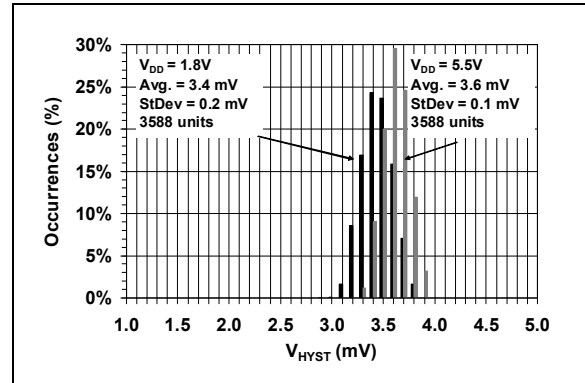


FIGURE 2-4: Input Hysteresis Voltage.

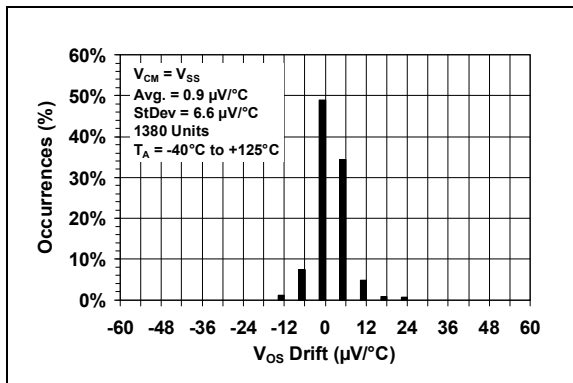


FIGURE 2-2: Input Offset Voltage Drift.

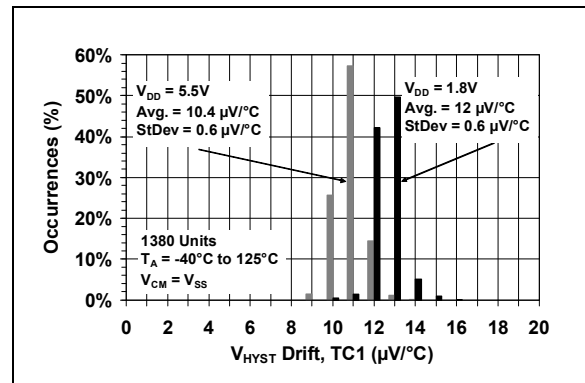


FIGURE 2-5: Input Hysteresis Voltage Drift – Linear Temp. Co. (TC1).

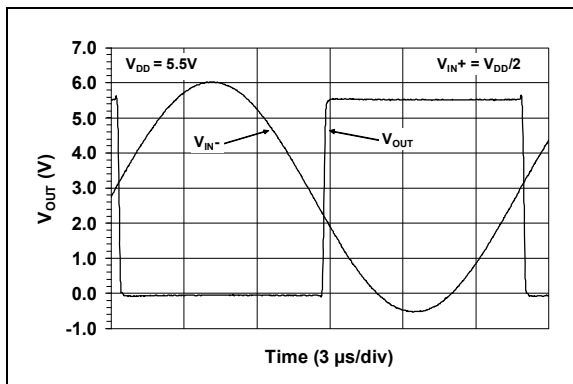


FIGURE 2-3: Input vs. Output Signal, No Phase Reversal.

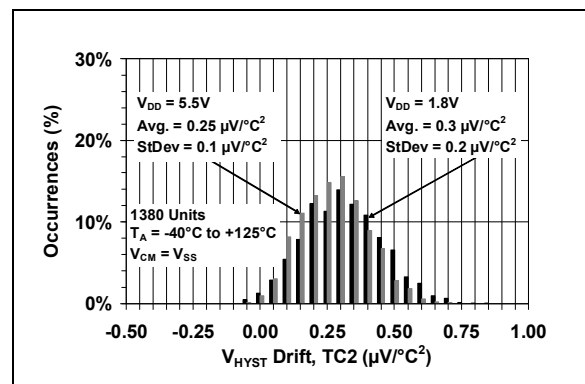


FIGURE 2-6: Input Hysteresis Voltage Drift – Quadratic Temp. Co. (TC2).

MCP6561/1R/1U/2/4

Note: Unless otherwise indicated: $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $T_A = +25^\circ\text{C}$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = \text{GND}$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 25\text{ pF}$.

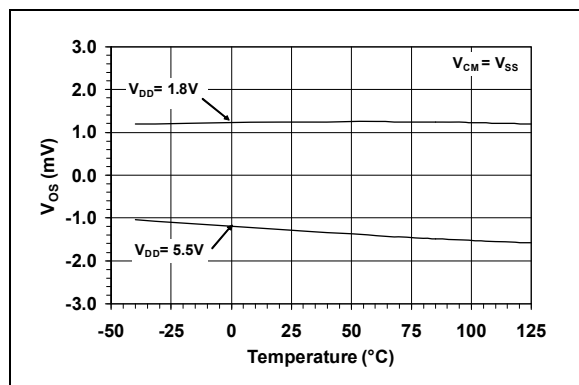


FIGURE 2-7: Input Offset Voltage vs. Temperature.

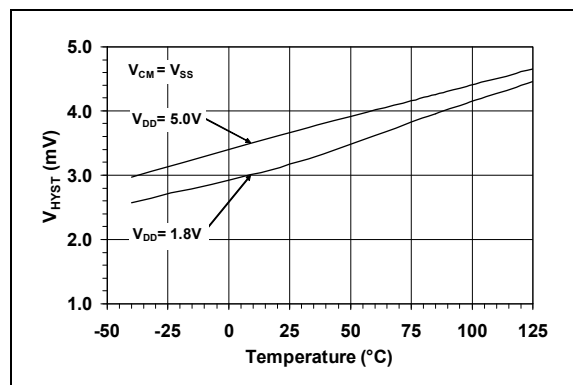


FIGURE 2-10: Input Hysteresis Voltage vs. Temperature.

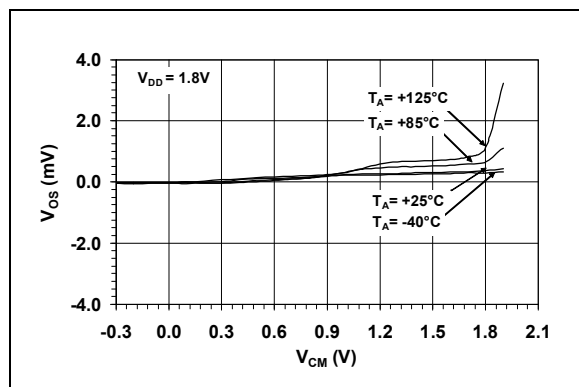


FIGURE 2-8: Input Offset Voltage vs. Common-Mode Input Voltage.

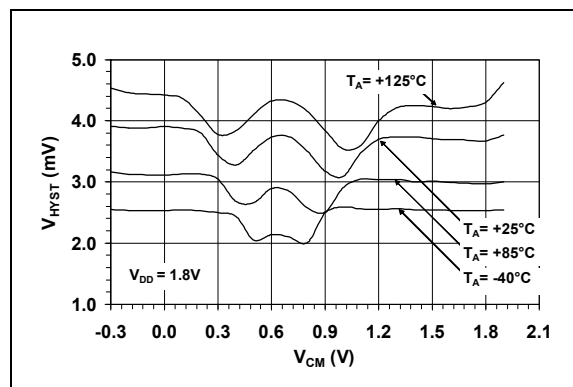


FIGURE 2-11: Input Hysteresis Voltage vs. Common-Mode Input Voltage.

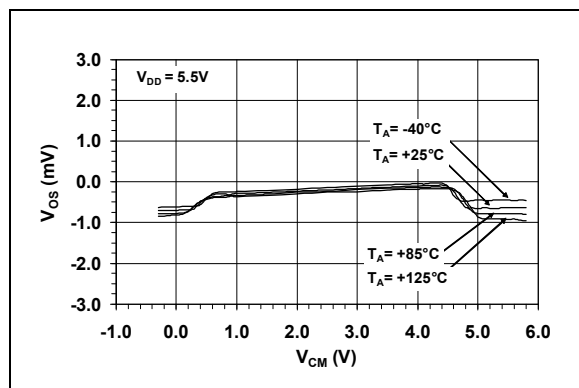


FIGURE 2-9: Input Offset Voltage vs. Common-Mode Input Voltage.

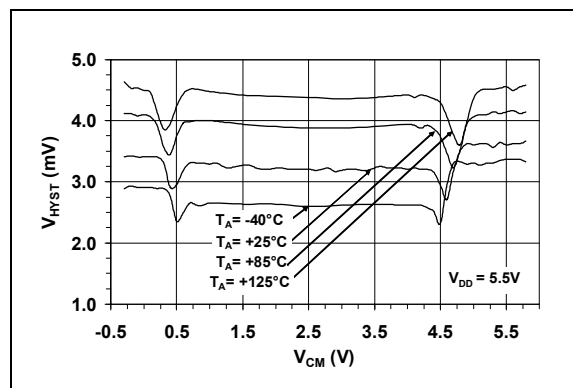


FIGURE 2-12: Input Hysteresis Voltage vs. Common-Mode Input Voltage.

Note: Unless otherwise indicated: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 25\text{ pF}$.

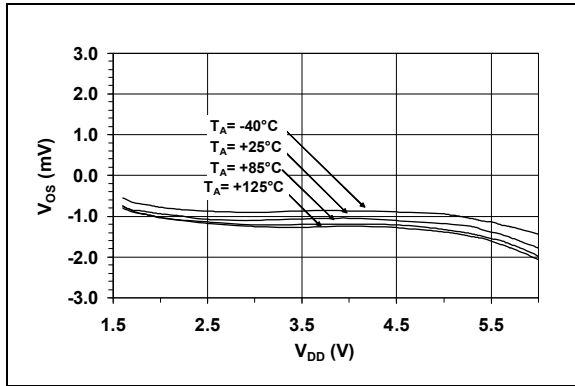


FIGURE 2-13: Input Offset Voltage vs. Supply Voltage vs. Temperature.

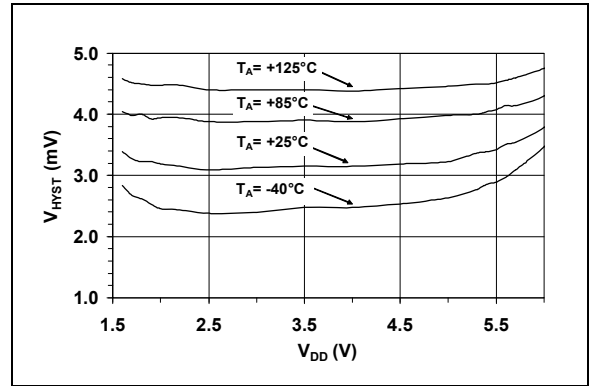


FIGURE 2-16: Input Hysteresis Voltage vs. Supply Voltage vs. Temperature.

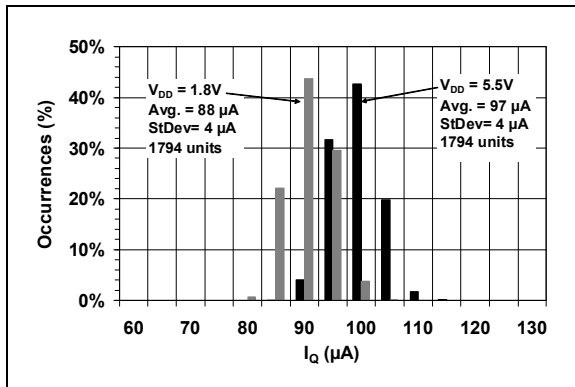


FIGURE 2-14: Quiescent Current.

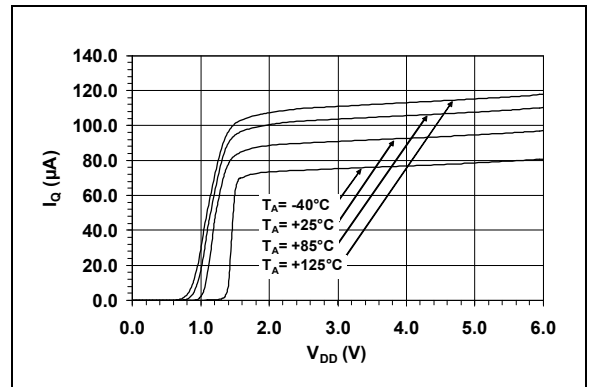


FIGURE 2-17: Quiescent Current vs. Supply Voltage vs. Temperature.

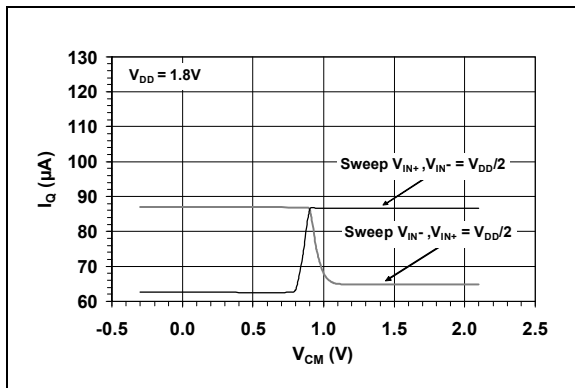


FIGURE 2-15: Quiescent Current vs. Common-Mode Input Voltage.

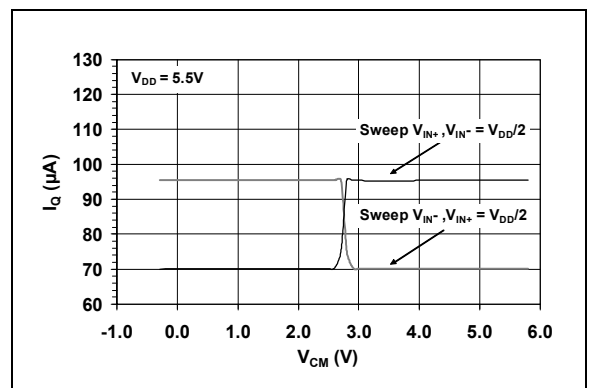


FIGURE 2-18: Quiescent Current vs. Common-Mode Input Voltage.

MCP6561/1R/1U/2/4

Note: Unless otherwise indicated: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 25\text{ pF}$.

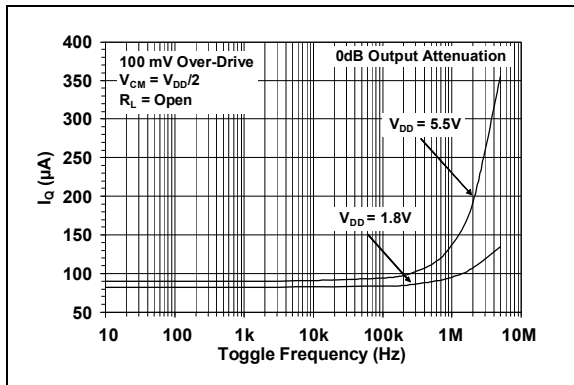


FIGURE 2-19: Quiescent Current vs. Toggle Frequency.

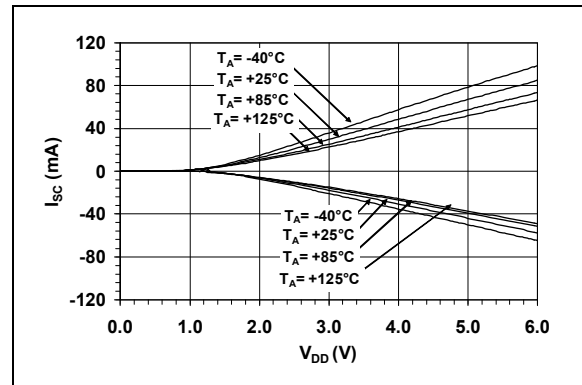


FIGURE 2-22: Short-Circuit Current vs. Supply Voltage vs. Temperature.

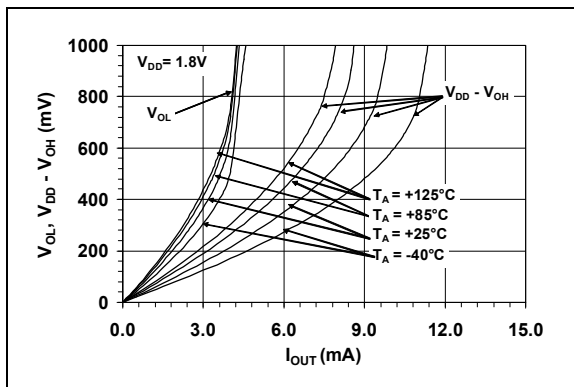


FIGURE 2-20: Output Headroom vs. Output Current.

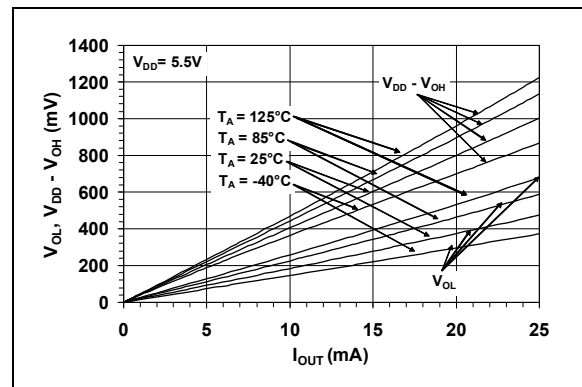


FIGURE 2-23: Output Headroom vs. Output Current.

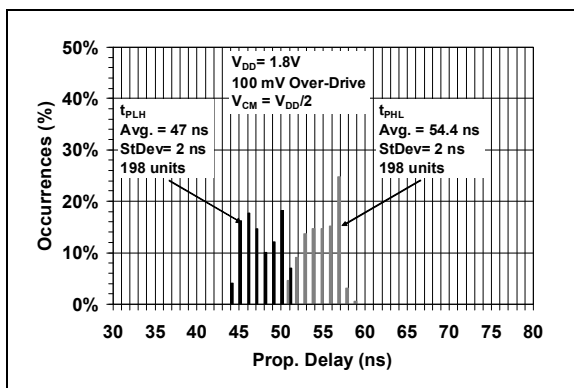


FIGURE 2-21: Low-to-High and High-to-Low Propagation Delays.

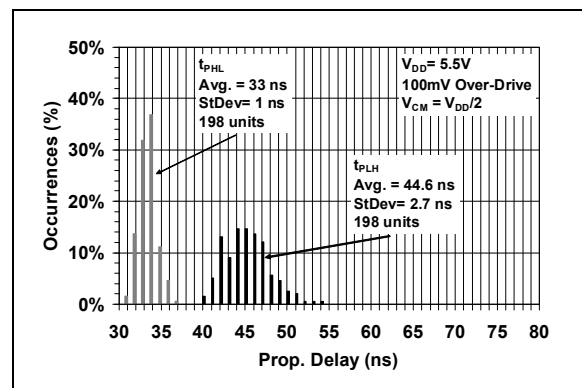


FIGURE 2-24: Low-to-High and High-to-Low Propagation Delays.

Note: Unless otherwise indicated: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 25\text{ pF}$.

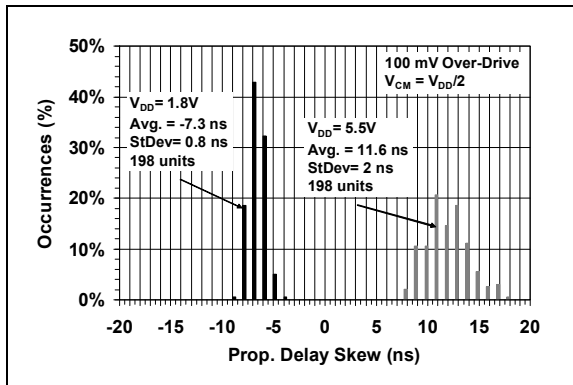


FIGURE 2-25: Propagation Delay Skew.

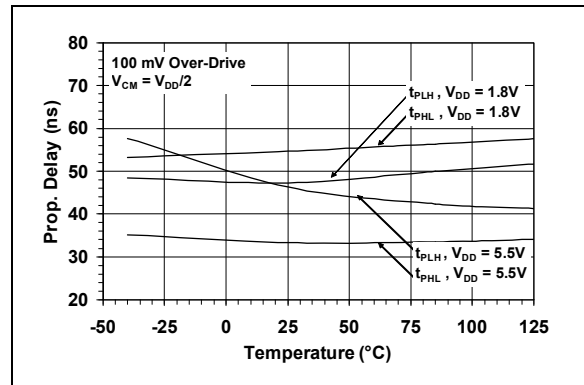


FIGURE 2-28: Propagation Delay vs. Temperature.

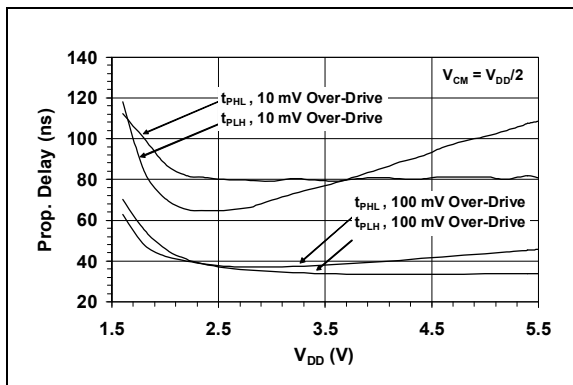


FIGURE 2-26: Propagation Delay vs. Supply Voltage.

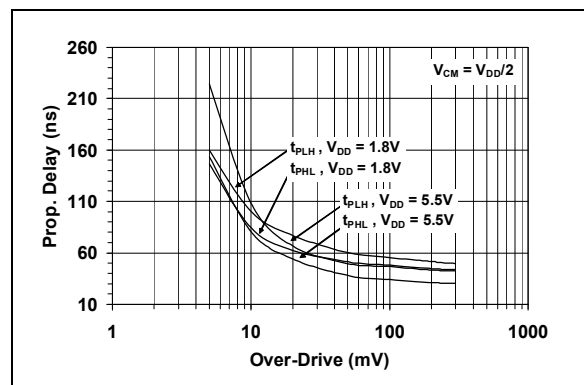


FIGURE 2-29: Propagation Delay vs. Input Overdrive.

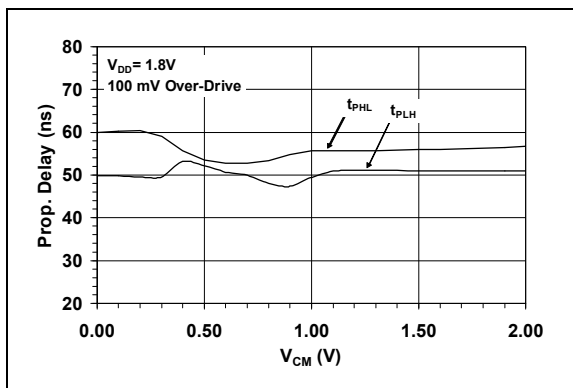


FIGURE 2-27: Propagation Delay vs. Common-Mode Input Voltage.

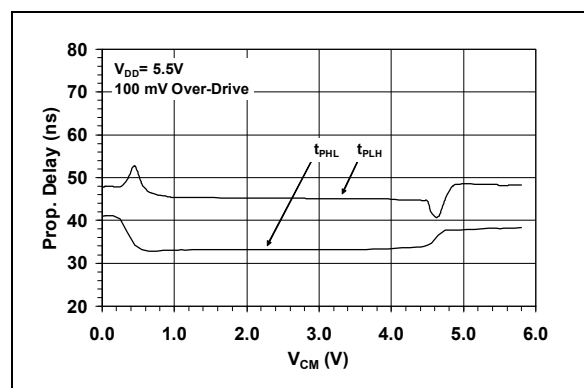


FIGURE 2-30: Propagation Delay vs. Common-Mode Input Voltage.

MCP6561/1R/1U/2/4

Note: Unless otherwise indicated: $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $T_A = +25^\circ\text{C}$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = \text{GND}$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 25\text{ pF}$.

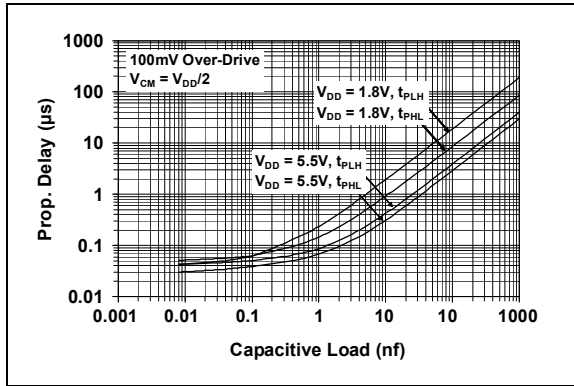


FIGURE 2-31: Propagation Delay vs. Capacitive Load.

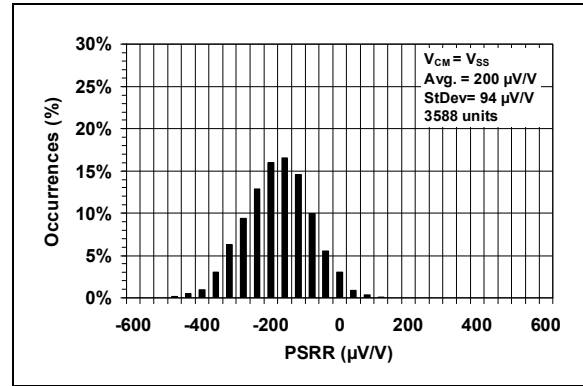


FIGURE 2-34: Power Supply Rejection Ratio (PSRR).

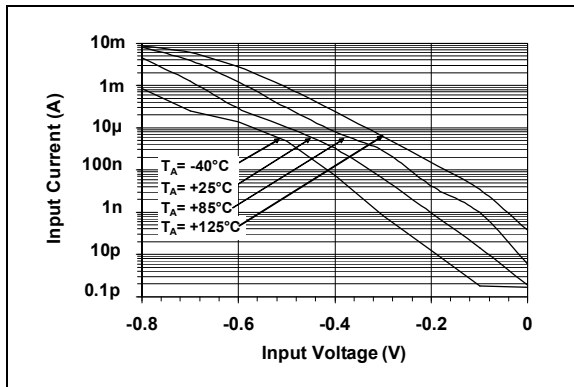


FIGURE 2-32: Input Bias Current vs. Input Voltage vs. Temperature.

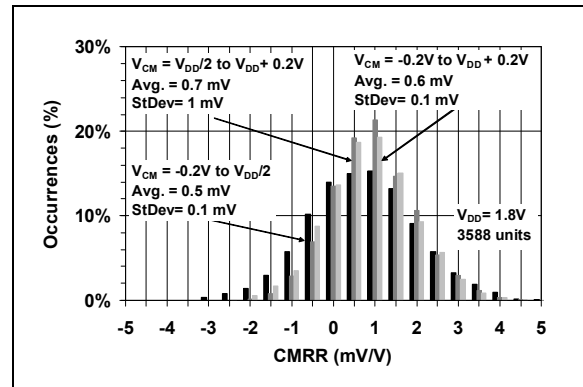


FIGURE 2-35: Common-Mode Rejection Ratio (CMRR).

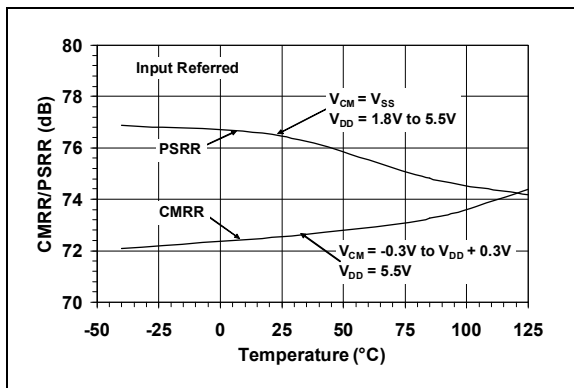


FIGURE 2-33: Common-Mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.

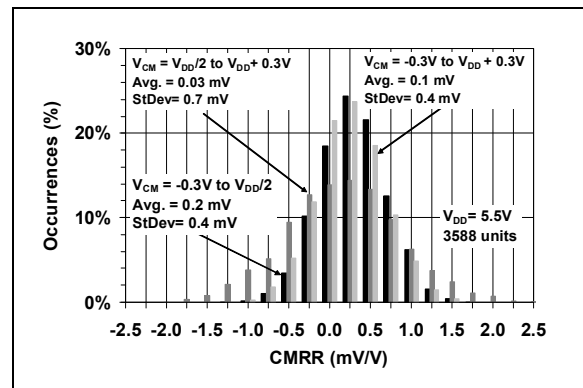


FIGURE 2-36: Common-Mode Rejection Ratio (CMRR).

Note: Unless otherwise indicated: $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 25\text{ pF}$.

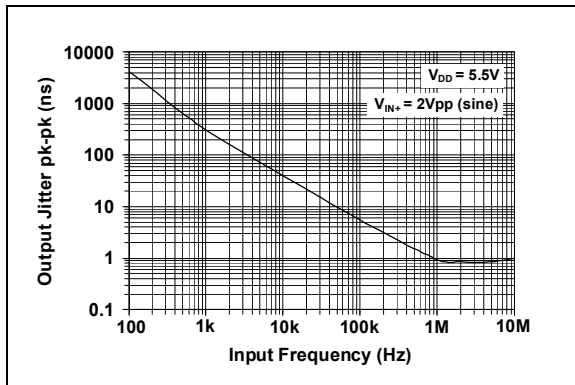


FIGURE 2-37: Output Jitter vs. Input Frequency.

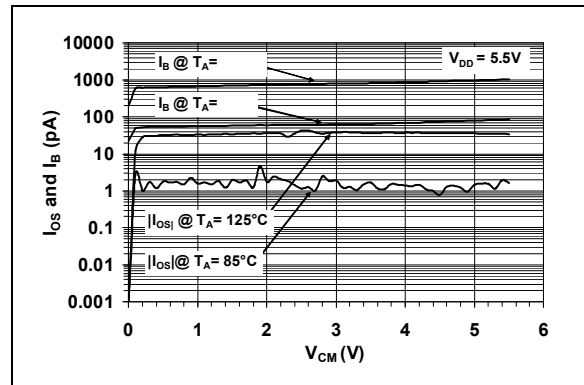


FIGURE 2-39: Input Offset Current and Input Bias Current vs. Common-Mode Input Voltage vs. Temperature.

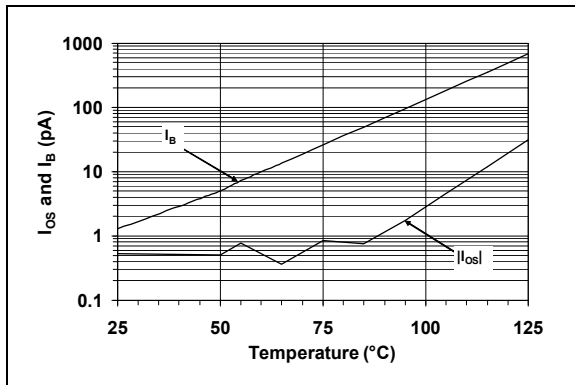


FIGURE 2-38: Input Offset Current and Input Bias Current vs. Temperature.

MCP6561/1R/1U/2/4

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

MCP6561	MCP6561R	MCP6561U	MCP6562	MCP6564	Symbol	Description
SC70, SOT-23	SOT-23	SOT-23	MSOP, SOIC	SOIC, TSSOP		
1	1	4	1	1	OUT, OUTA	Digital Output (Comparator A)
4	4	3	2	2	V_{IN-} , V_{INA-}	Inverting Input (Comparator A)
3	3	1	3	3	V_{IN+} , V_{INA+}	Noninverting Input (Comparator A)
5	2	5	8	4	V_{DD}	Positive Power Supply
—	—	—	5	5	V_{INB+}	Noninverting Input (Comparator B)
—	—	—	6	6	V_{INB-}	Inverting Input (Comparator B)
—	—	—	7	7	OUTB	Digital Output (Comparator B)
—	—	—	—	8	OUTC	Digital Output (Comparator C)
—	—	—	—	9	V_{INC-}	Inverting Input (Comparator C)
—	—	—	—	10	V_{INC+}	Noninverting Input (Comparator C)
2	5	2	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	V_{IND+}	Noninverting Input (Comparator D)
—	—	—	—	13	V_{IND-}	Inverting Input (Comparator D)
—	—	—	—	14	OUTD	Digital Output (Comparator D)

3.1 Analog Inputs

The comparator noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.2 Digital Outputs

The comparator outputs are CMOS push-pull, digital outputs. They are designed to be compatible with CMOS and TTL logic, and are capable of driving heavy DC or capacitive loads.

3.3 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 1.8V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD} .

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 μ F to 0.1 μ F) within 2 mm of the V_{DD} pin. These pins can share a bulk capacitor with nearby analog parts (within 100 mm), but it is not required.

MCP6561/1R/1U/2/4

NOTES:

4.0 APPLICATION INFORMATION

The MCP6561/1R/1U/2/4 families of push-pull output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of high-speed applications requiring low-power consumption.

4.1 Comparator Inputs

4.1.1 NORMAL OPERATION

The input stage of these families of devices uses three differential input stages in parallel: one operates at low input voltages, one at high input voltages and one at middle input voltages. With this topology, the input voltage range is 0.3V above V_{DD} and 0.3V below V_{SS} , while providing low offset voltage throughout the Common-mode range. The input offset voltage is measured at both $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

The MCP6561/1R/1U/2/4 families have internally set hysteresis V_{HYST} that is small enough to maintain input offset accuracy and large enough to eliminate output chattering caused by the comparator's own input noise voltage, E_{NI} . Figure 4-1 depicts this behavior. Input offset voltage (V_{OS}) is the center (average) of the (input referred) low-high and high-low trip points. Input hysteresis voltage (V_{HYST}) is the difference between the same trip points.

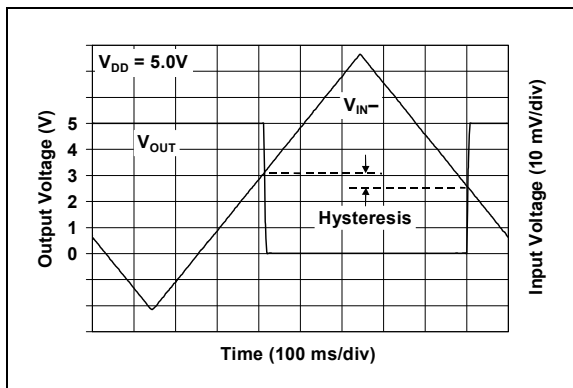


FIGURE 4-1: The MCP6561/1R/1U/2/4 Comparators' Internal Hysteresis Eliminates Output Chatter Caused by Input Noise Voltage.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-2. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS} . They also clamp any voltages that go too far above V_{DD} . Their breakdown voltage is high enough to allow normal operation and low enough to bypass ESD events within the specified limits.

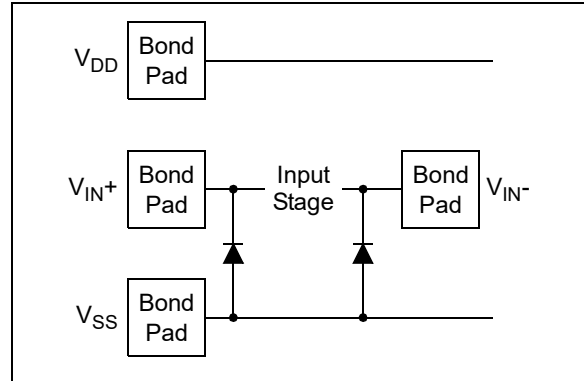


FIGURE 4-2: Simplified Analog Input ESD Structures.

In order to prevent damage and/or improper operation of these amplifiers, the circuits they are in must limit the currents (and voltages) at the V_{IN+} and V_{IN-} pins (see Section 1.1 "Absolute Maximum Ratings†" at the beginning of Section 1.0 "Electrical Characteristics"). Figure 4-3 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN+} and V_{IN-}) from going too far below ground, and the resistors, R_1 and R_2 , limit the possible current drawn out of the input pin. Diodes, D_1 and D_2 , prevent the input pin (V_{IN+} and V_{IN-}) from going too far above V_{DD} . When implemented as shown, resistors, R_1 and R_2 , also limit the current through D_1 and D_2 .

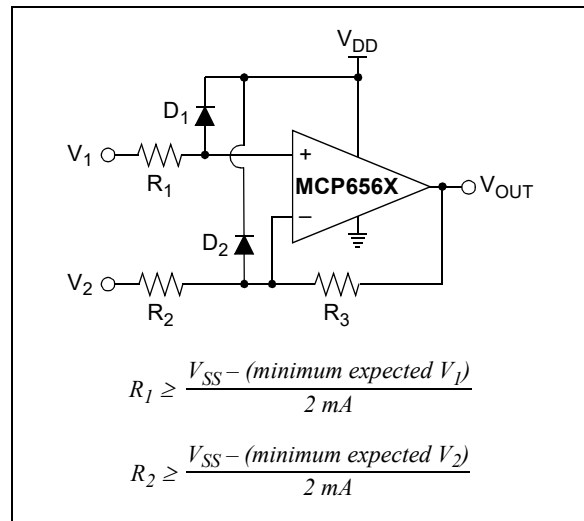


FIGURE 4-3: Protecting the Analog Inputs.

It is also possible to connect the diodes to the left of the resistors, R_1 and R_2 . In this case, the currents through the diodes, D_1 and D_2 , need to be limited by some other mechanism. The resistor then serves as an inrush current limiter; the DC current into the input pins (V_{IN+} and V_{IN-}) should be very small.

MCP6561/1R/1U/2/4

A significant amount of current can flow out of the inputs when the Common-mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-32. Applications that are high-impedance may need to limit the usable voltage range.

4.1.3 PHASE REVERSAL

The MCP6561/1R/1U/2/4 comparator families use CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.2 Push-Pull Output

The push-pull output is designed to be compatible with CMOS and TTL logic, while the output transistors are configured to give rail-to-rail output performance. They are driven with circuitry that minimizes any switching current (shoot-through current from supply-to-supply) when the output is transitioned from high-to-low or from low-to-high (see Figure 2-15 and Figure 2-18 for more information).

4.3 Externally Set Hysteresis

Greater flexibility in selecting hysteresis (or input trip points) is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is best not to cycle between high and low states too frequently (e.g., air conditioner thermostatic control). Output chatter also increases the dynamic supply current.

4.3.1 NONINVERTING CIRCUIT

Figure 4-4 shows a noninverting circuit for single-supply applications using just two resistors. The resulting hysteresis diagram is shown in Figure 4-5.

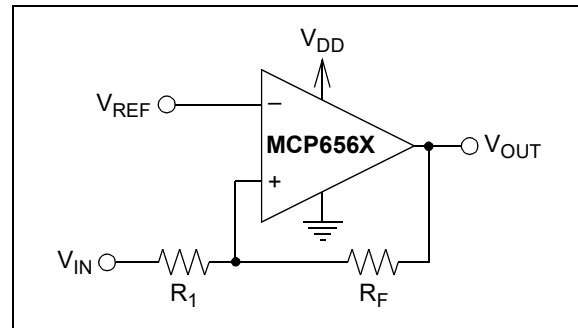


FIGURE 4-4: Noninverting Circuit with Hysteresis for Single Supply.

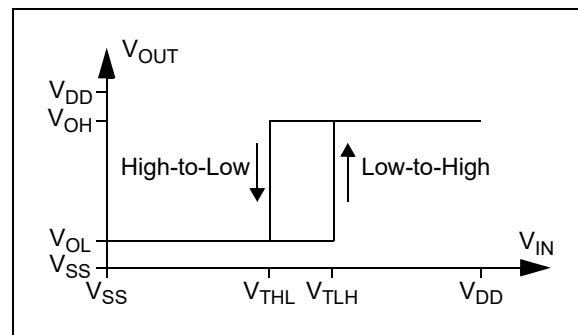


FIGURE 4-5: Hysteresis Diagram for the Noninverting Circuit.

The trip points for Figure 4-4 and Figure 4-5 are:

EQUATION 4-1:

$$V_{TLH} = V_{REF} \left(1 + \frac{R_1}{R_F} \right) - V_{OL} \left(\frac{R_1}{R_F} \right)$$

$$V_{THL} = V_{REF} \left(1 + \frac{R_1}{R_F} \right) - V_{OH} \left(\frac{R_1}{R_F} \right)$$

Where:

V_{TLH} = Trip Voltage from Low-to-High

V_{THL} = Trip Voltage from High-to-Low

4.3.2 INVERTING CIRCUIT

Figure 4-6 shows an inverting circuit for single supply using three resistors. The resulting hysteresis diagram is shown in Figure 4-7.

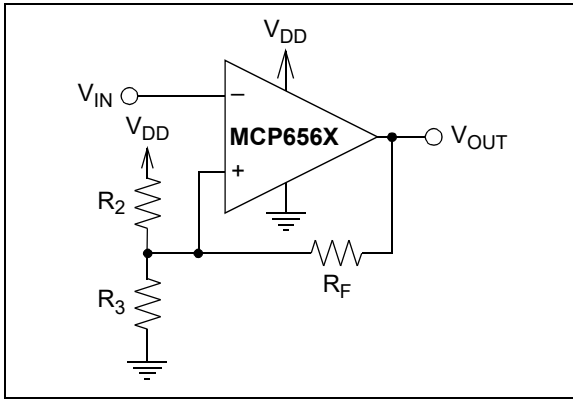


FIGURE 4-6: Inverting Circuit with Hysteresis.

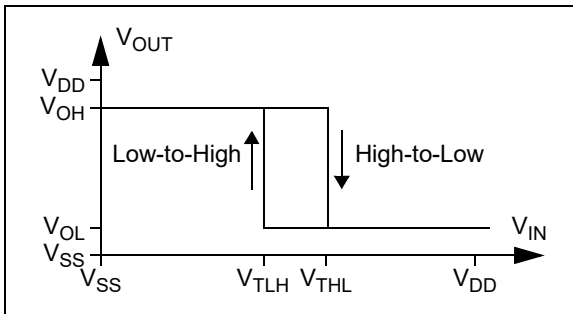


FIGURE 4-7: Hysteresis Diagram for the Inverting Circuit.

In order to determine the trip voltages (V_{THL} and V_{TLH}) for the circuit shown in Figure 4-6, R_2 and R_3 can be simplified to the Thevenin equivalent circuit with respect to V_{DD} , as shown in Figure 4-8.

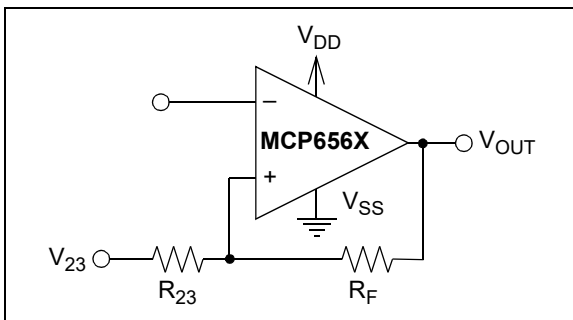


FIGURE 4-8: Thevenin Equivalent Circuit.

Where:

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{R_3}{R_2 + R_3} \times V_{DD}$$

Using this simplified circuit, the trip voltage can be calculated using the following equation:

EQUATION 4-2:

$$V_{THL} = V_{OH} \left(\frac{R_{23}}{R_{23} + R_F} \right) + V_{23} \left(\frac{R_F}{R_{23} + R_F} \right)$$

$$V_{TLH} = V_{OL} \left(\frac{R_{23}}{R_{23} + R_F} \right) + V_{23} \left(\frac{R_F}{R_{23} + R_F} \right)$$

Where:

V_{TLH} = Trip Voltage from Low-to-High

V_{THL} = Trip Voltage from High-to-Low

Figure 2-20, and Figure 2-23 can be used to determine typical values for V_{OH} and V_{OL} .

4.4 Bypass Capacitors

With this family of comparators, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 μ F to 0.1 μ F) within 2 mm for good edge rate performance.

4.5 Capacitive Loads

Reasonable capacitive loads (e.g., logic gates) have little impact on propagation delay (see Figure 2-31). The supply current increases with increasing toggle frequency (Figure 2-19), especially with higher capacitive loads. The output slew rate and propagation delay performance will be reduced with higher capacitive loads.

MCP6561/1R/1U/2/4

4.6 PCB Surface Leakage

In applications where low input bias current is critical, PCB (Printed Circuit Board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6561/1R/1U/2/4 families' bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-9.

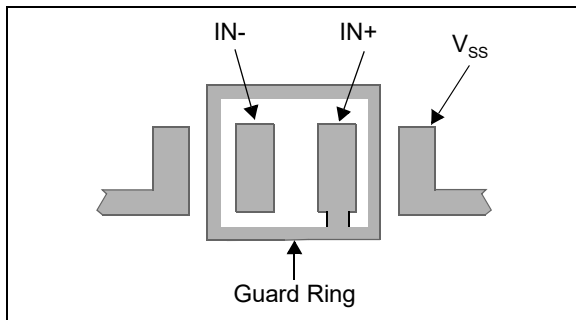


FIGURE 4-9: Example Guard Ring Layout for Inverting Circuit.

1. Inverting Configuration (Figures 4-6 and 4-9):
 - a) Connect the guard ring to the noninverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the comparator (e.g., $V_{DD}/2$ or ground).
 - b) Connect the inverting pin (V_{IN-}) to the input pad without touching the guard ring.
2. Noninverting Configuration (Figure 4-4):
 - a) Connect the noninverting pin (V_{IN+}) to the input pad without touching the guard ring.
 - b) Connect the guard ring to the inverting input pin (V_{IN-}).

4.7 PCB Layout Technique

When designing the PCB layout, it is critical to note that analog and digital signal traces are adequately separated to prevent signal coupling. If the comparator output trace is at close proximity to the input traces, then large output voltage changes from V_{SS} to V_{DD} , or visa versa, may couple to the inputs and cause the device output to oscillate. To prevent such oscillation, the output traces must be routed away from the input pins. The SC70 and SOT-23 are relatively immune because the output pin OUT (Pin 1) is separated by the power pin V_{DD}/V_{SS} (Pin 2) from the input pin +IN (as long as the analog and digital traces remain separated throughout the PCB). However, the pinouts for the dual and quad packages (SOIC, MSOP, TSSOP) have OUT and -IN pins (Pins 1 and 2) close to each other. The recommended layout for these packages is shown in Figure 4-10.

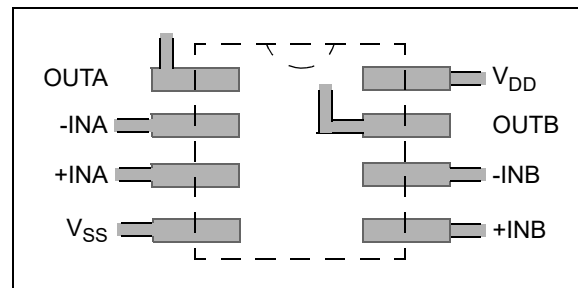


FIGURE 4-10: Recommended Layout.

4.8 Unused Comparators

An unused amplifier in a quad package (MCP6564) should be configured as shown in Figure 4-11. This circuit prevents the output from toggling and causing crosstalk. It uses the minimum number of components and draws minimal current (see Figure 2-15 and Figure 2-18).

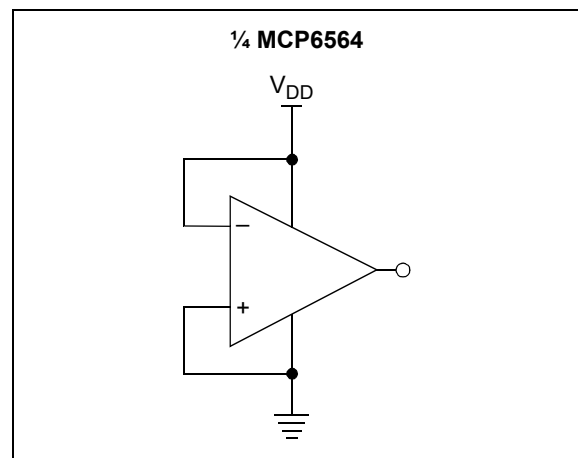


FIGURE 4-11: Unused Comparators.

4.9 Typical Applications

4.9.1 PRECISE COMPARATOR

Some applications require higher DC precision. An easy way to solve this problem is to use an amplifier (such as the MCP6291) to gain-up the input signal before it reaches the comparator. Figure 4-12 shows an example of this approach.

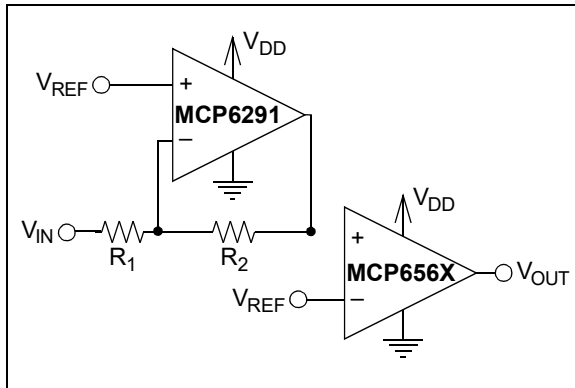


FIGURE 4-12: *Precise Inverting Comparator.*

4.9.2 WINDOWED COMPARATOR

Figure 4-13 shows one approach to designing a windowed comparator. The AND gate produces a logic '1' when the input voltage is between V_{RB} and V_{RT} (where $V_{RT} > V_{RB}$).

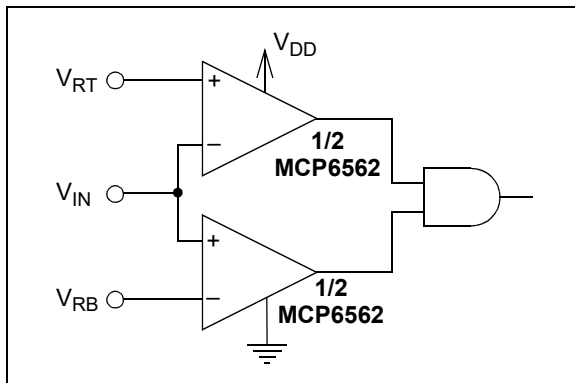


FIGURE 4-13: *Windowed Comparator.*

4.9.3 BISTABLE MULTIVIBRATOR

A simple bistable multivibrator design is shown in Figure 4-14. V_{REF} needs to be between the power supplies ($V_{SS} = GND$ and V_{DD}) to achieve oscillation. The output duty cycle changes with V_{REF} .

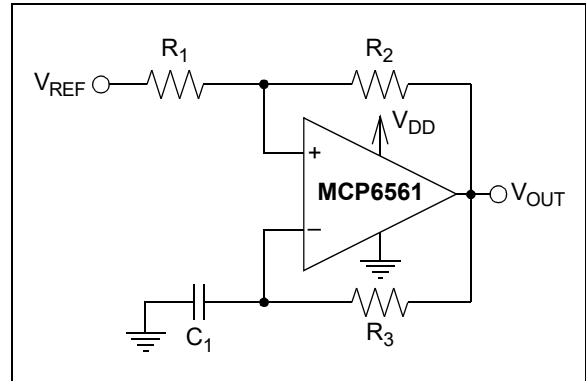


FIGURE 4-14: *Bistable Multivibrator.*

MCP6561/1R/1U/2/4

NOTES:

5.0 DESIGN AIDS

5.1 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

5.2 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip website at www.microchip.com/analogtools. Three of our boards that are especially useful are:

- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV
- 5/6-Pin SOT23 Evaluation Board, P/N VSUPEV2

5.3 Application Notes

The following Microchip Application Note is available on the Microchip website at www.microchip.com and is recommended as a supplemental reference resource:

- **AN895**, "Oscillator Circuits For RTD Temperature Sensors", DS00895

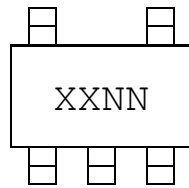
MCP6561/1R/1U/2/4

NOTES:

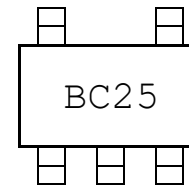
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

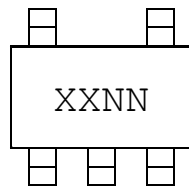
5-Lead SC-70 (MCP6561)



Example:



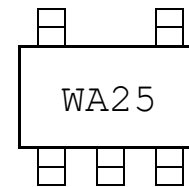
5-Lead SOT-23 (MCP6561, MCP6561R, MCP6561U)



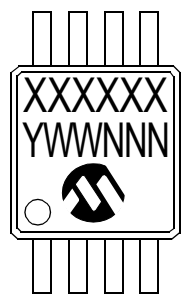
Device	Code
MCP6561T	WBNN
MCP6561RT	WANN
MCP6561UT	WKNN

Note: Applies to 5-Lead SOT-23.

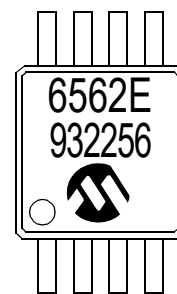
Example:



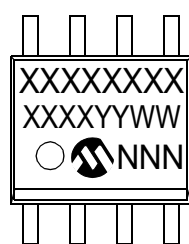
8-Lead MSOP (MCP6562)



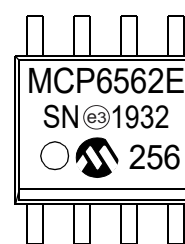
Example:



8-Lead SOIC (150 mil) (MCP6562)



Example:



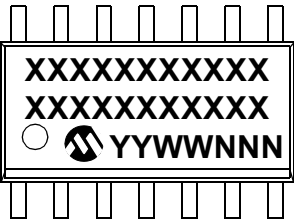
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

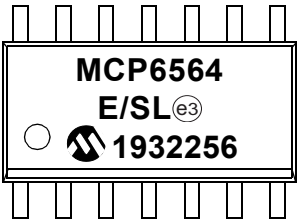
MCP6561/1R/1U/2/4

Package Marking Information (Continued)

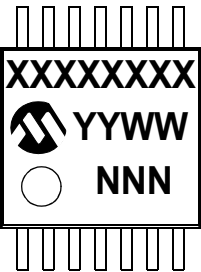
14-Lead SOIC (150 mil) (MCP6564)



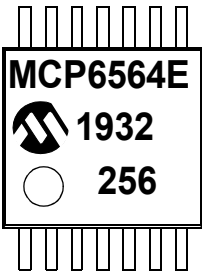
Example:



14-Lead TSSOP (MCP6564)

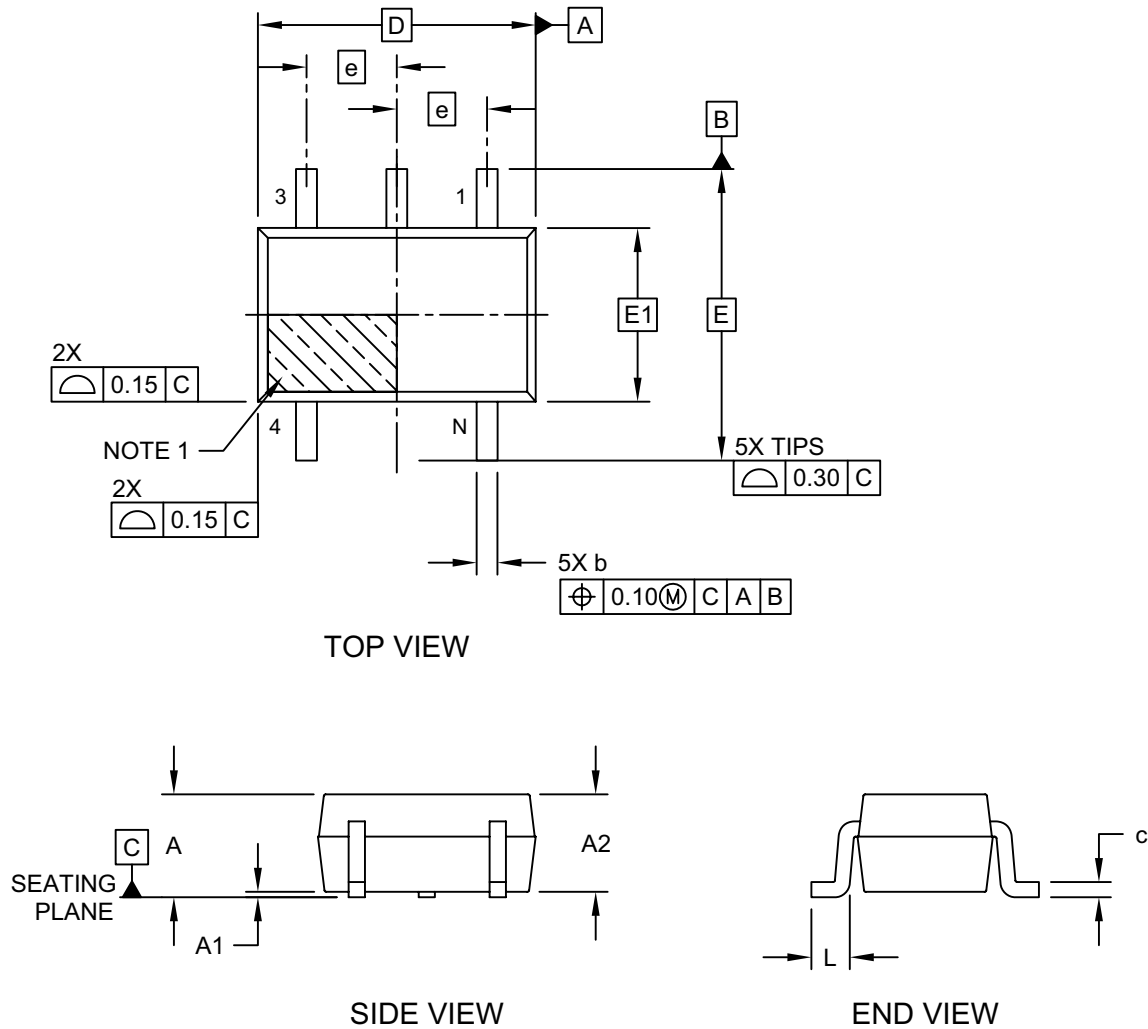


Example:



5-Lead Plastic Small Outline Transistor (LT) [SC70]

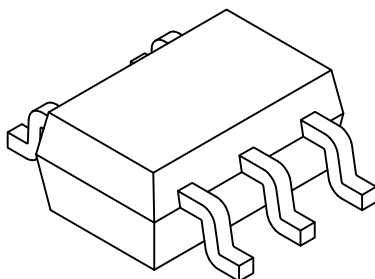
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



MCP6561/1R/1U/2/4

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D	2.00 BSC		
Overall Width	E	2.10 BSC		
Molded Package Width	E1	1.25 BSC		
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

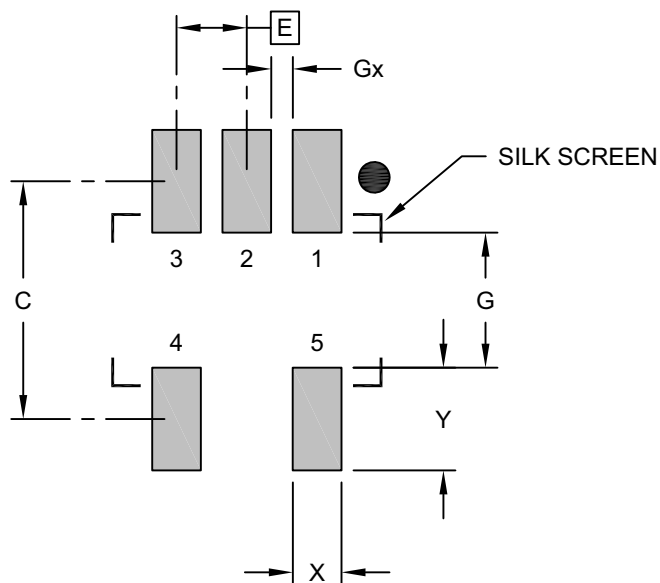
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061-LT Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

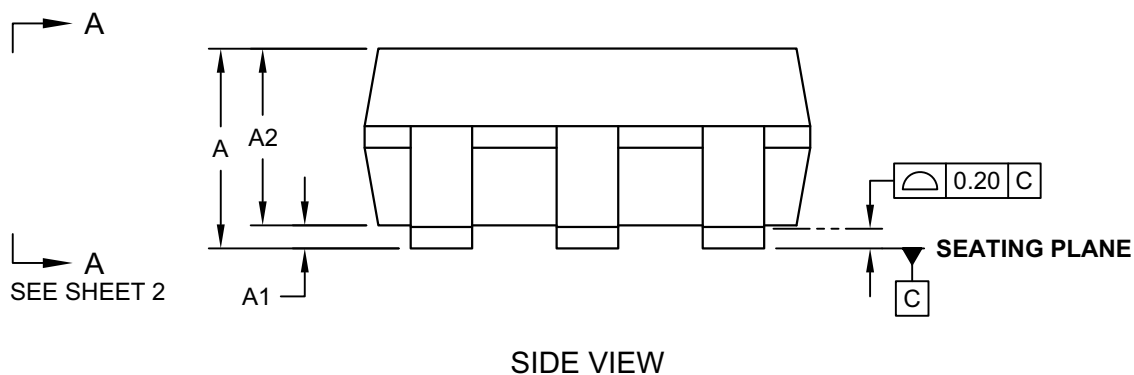
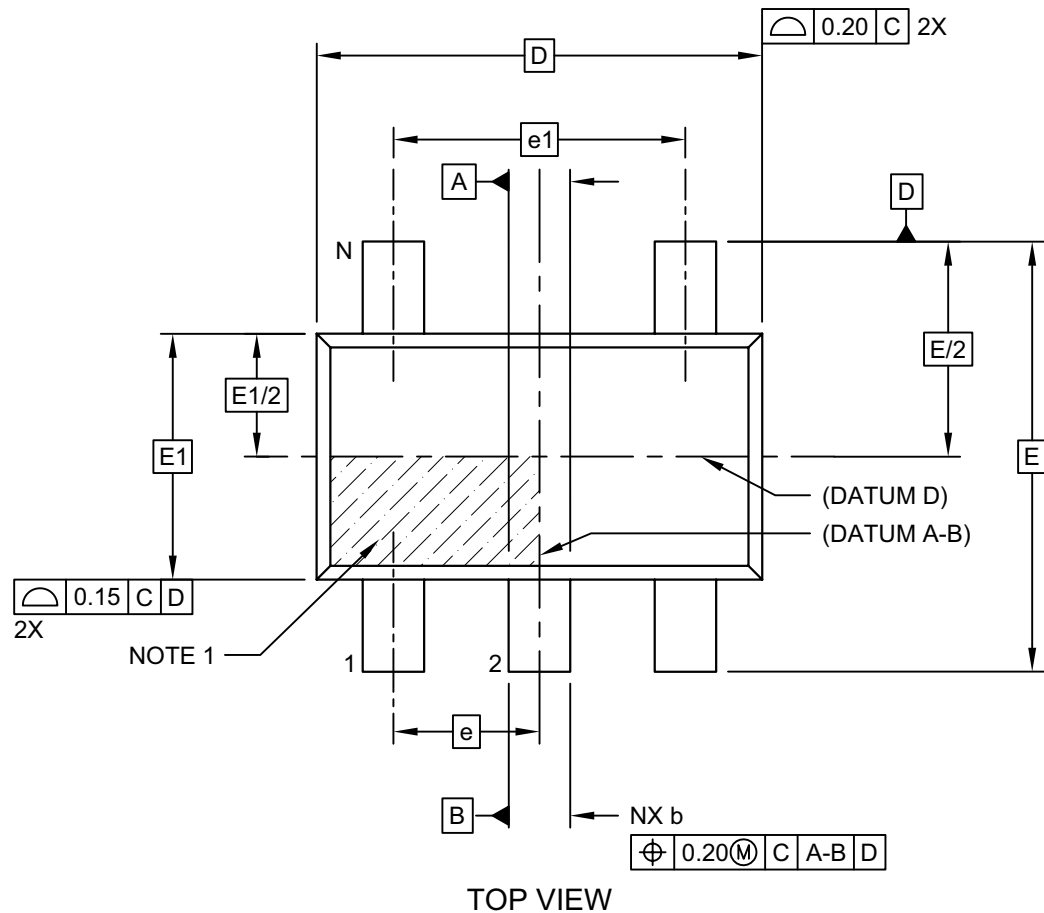
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061-LT Rev E

MCP6561/1R/1U/2/4

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

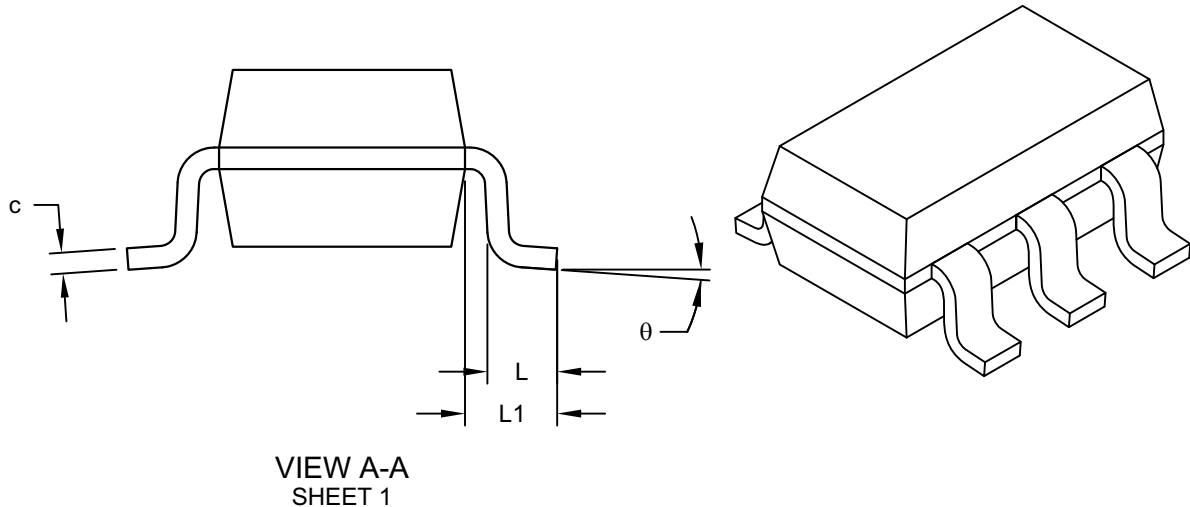
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-091-OT Rev F Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	-	0.60
Footprint	L1	0.60 REF		
Foot Angle	φ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

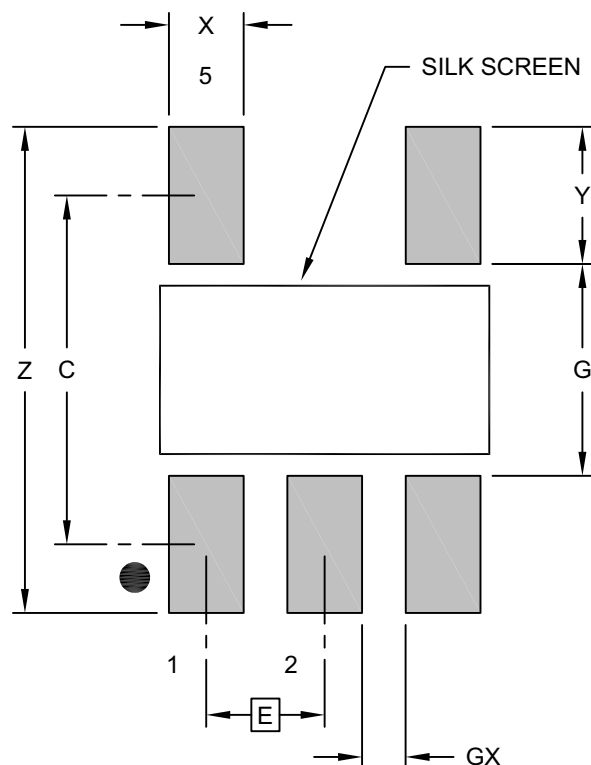
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev F Sheet 2 of 2

MCP6561/1R/1U/2/4

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

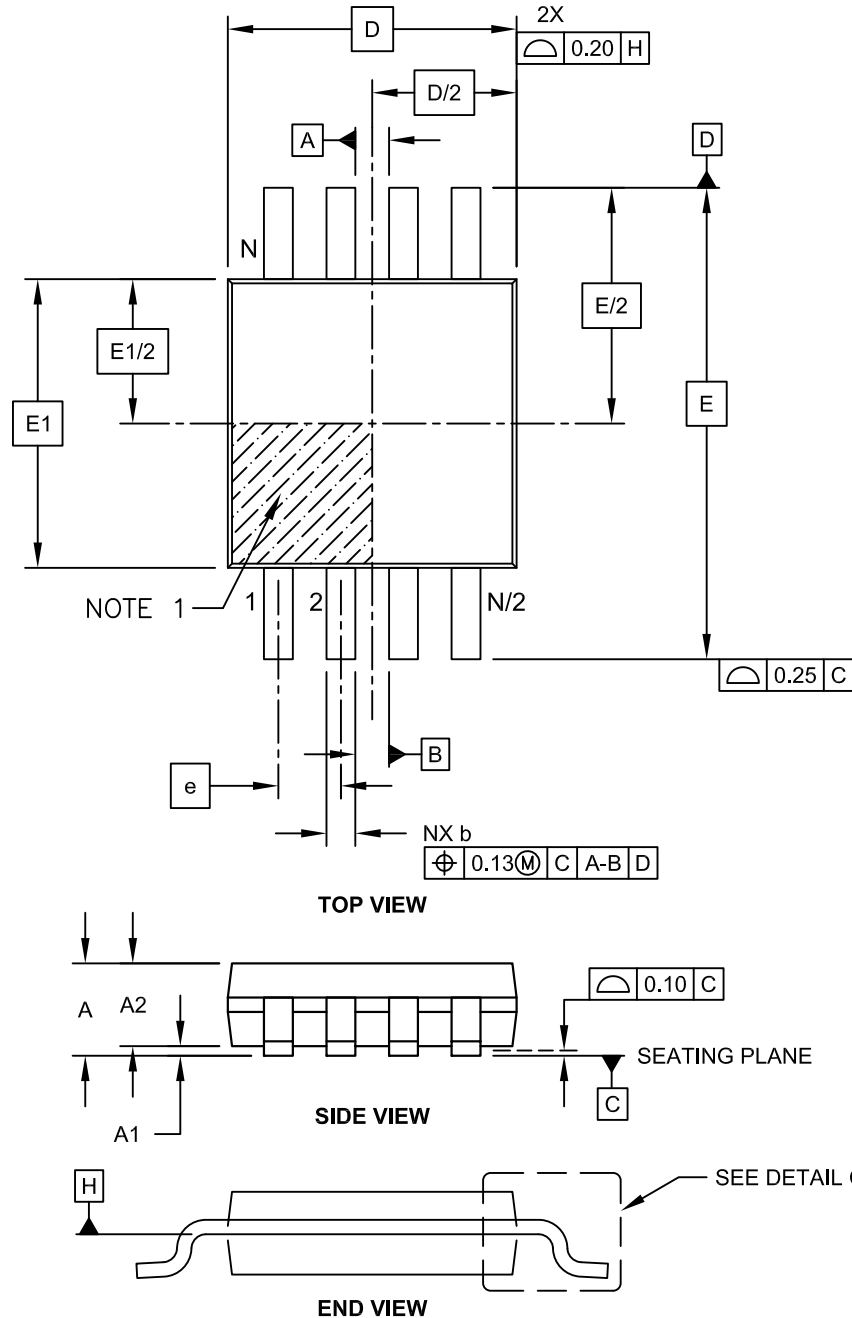
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev F

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

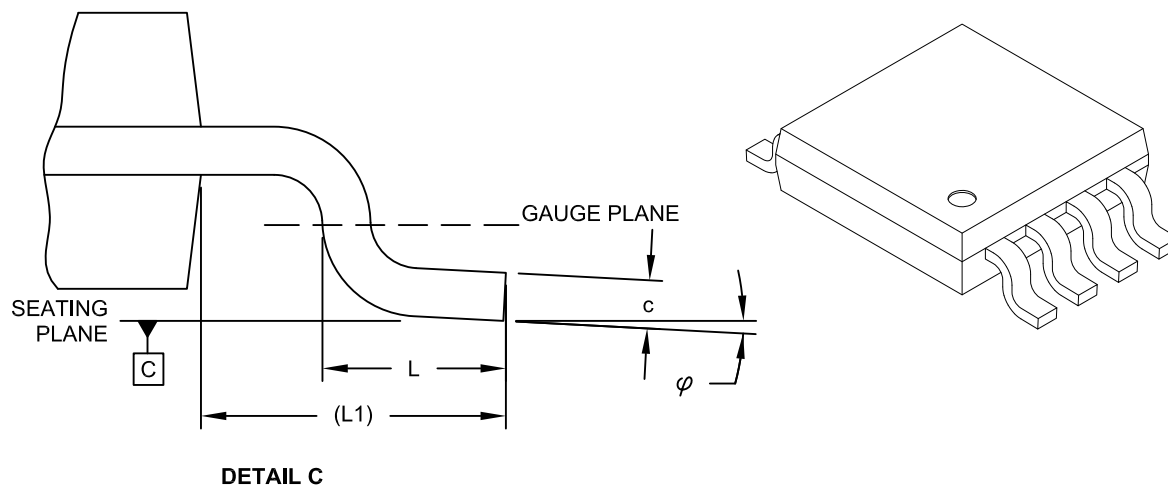


Microchip Technology Drawing C04-111C Sheet 1 of 2

MCP6561/1R/1U/2/4

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

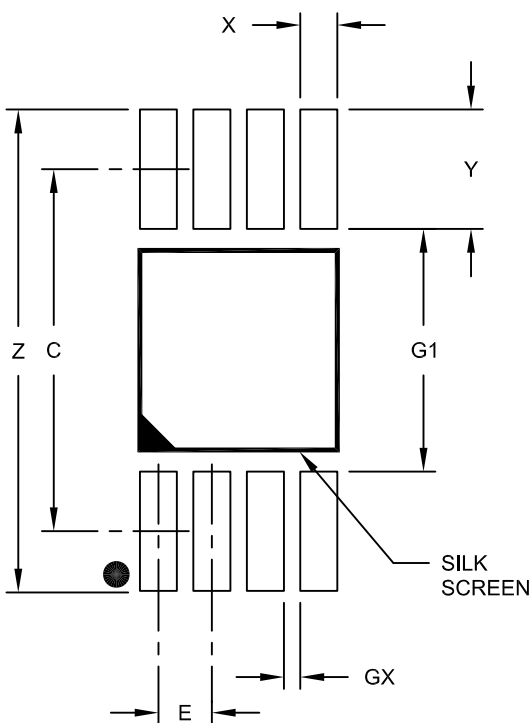
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

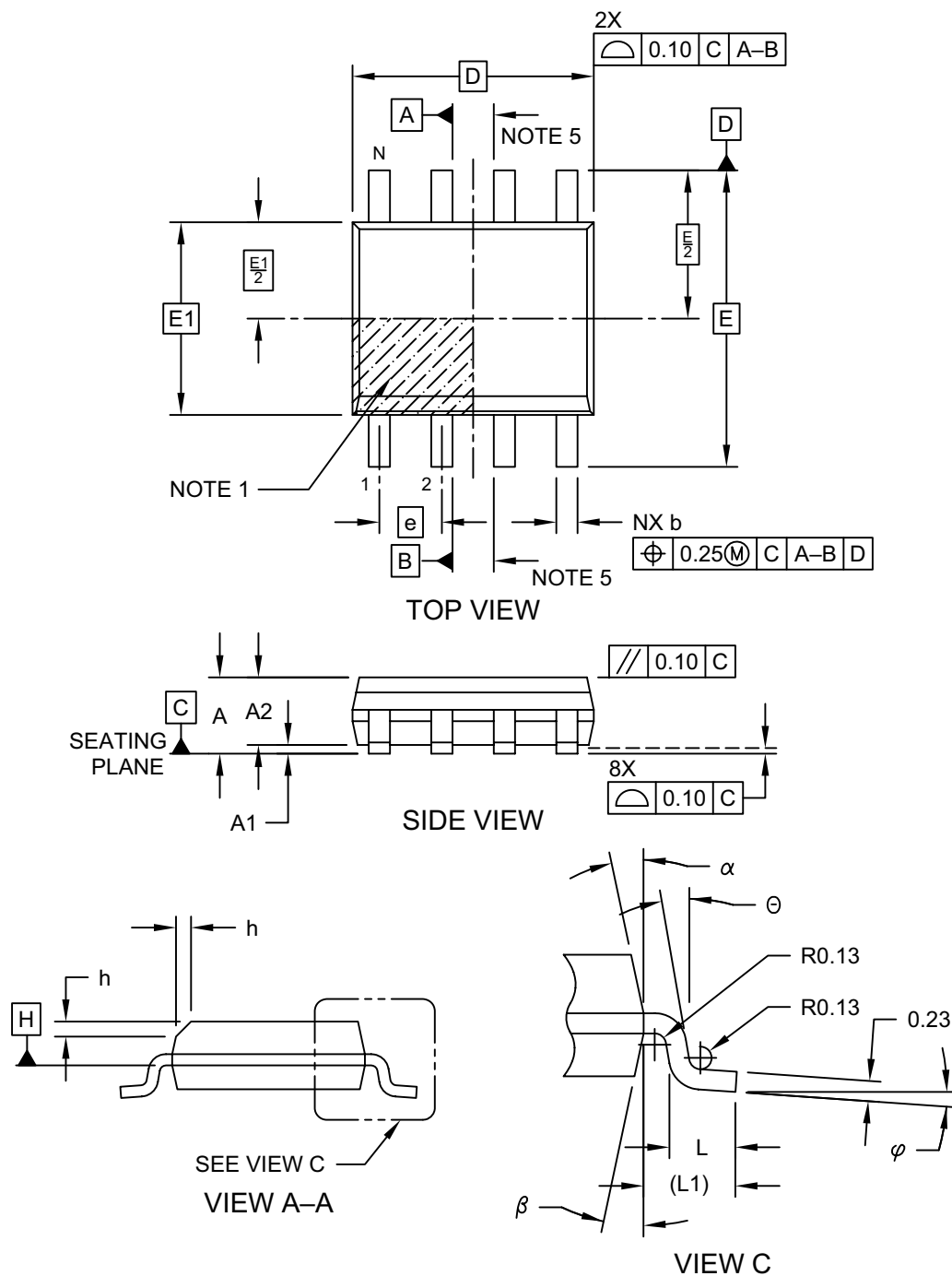
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

MCP6561/1R/1U/2/4

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

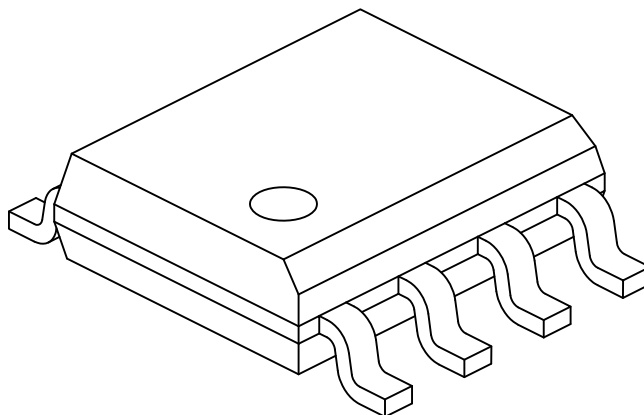
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-057-SN Rev E Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

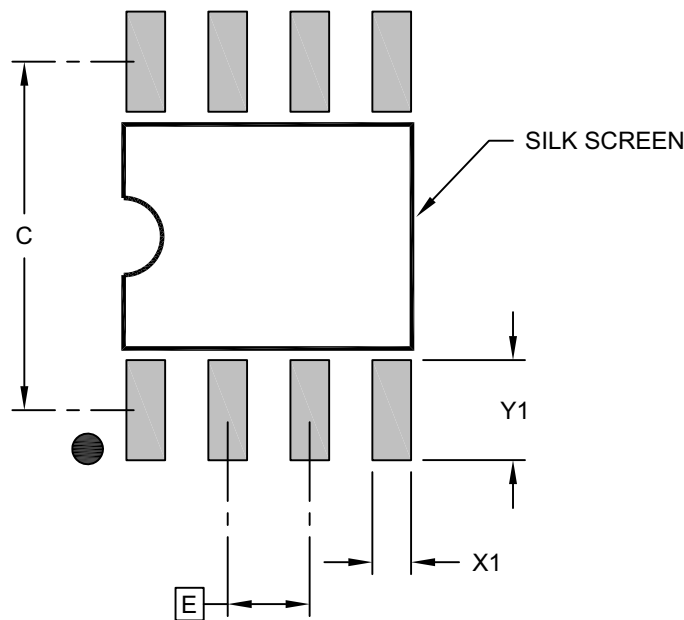
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev E Sheet 2 of 2

MCP6561/1R/1U/2/4

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

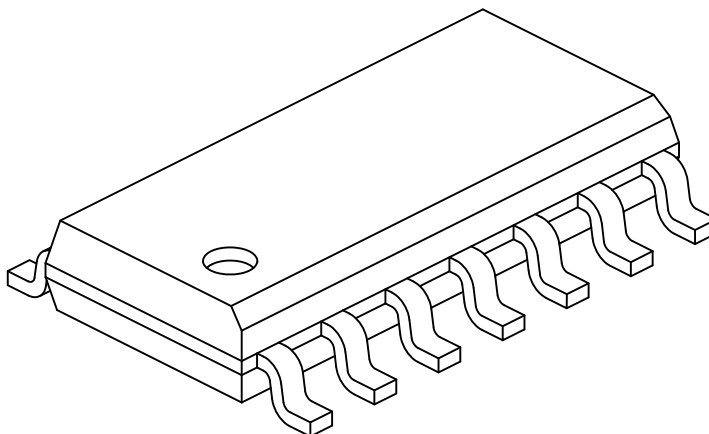
- 1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev E

MCP6561/1R/1U/2/4

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		14		
Pitch	e		1.27 BSC		
Overall Height	A		-	-	1.75
Molded Package Thickness	A2		1.25	-	-
Standoff §	A1		0.10	-	0.25
Overall Width	E		6.00 BSC		
Molded Package Width	E1		3.90 BSC		
Overall Length	D		8.65 BSC		
Chamfer (Optional)	h		0.25	-	0.50
Foot Length	L		0.40	-	1.27
Footprint	L1		1.04 REF		
Lead Angle	Θ		0°	-	-
Foot Angle	φ		0°	-	8°
Lead Thickness	c		0.10	-	0.25
Lead Width	b		0.31	-	0.51
Mold Draft Angle Top	α		5°	-	15°
Mold Draft Angle Bottom	β		5°	-	15°

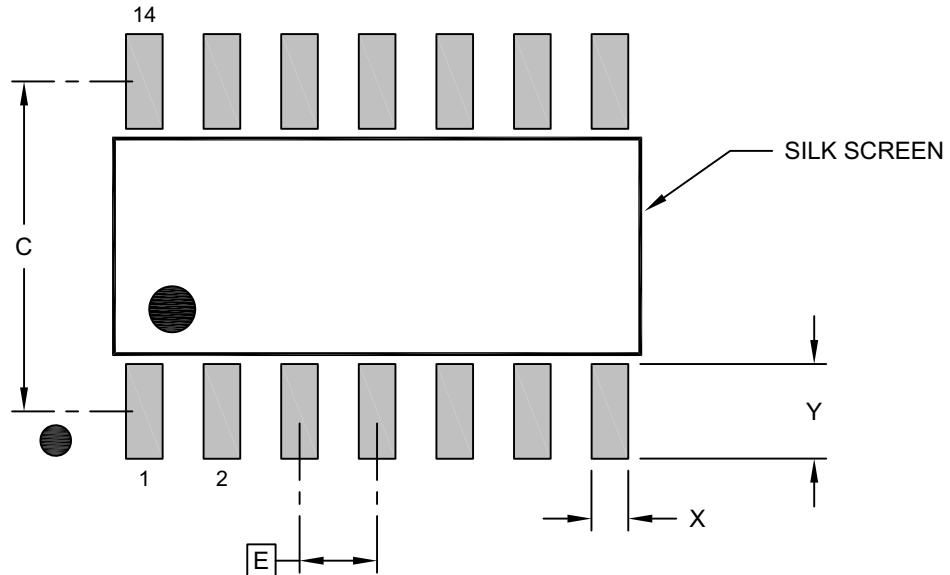
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

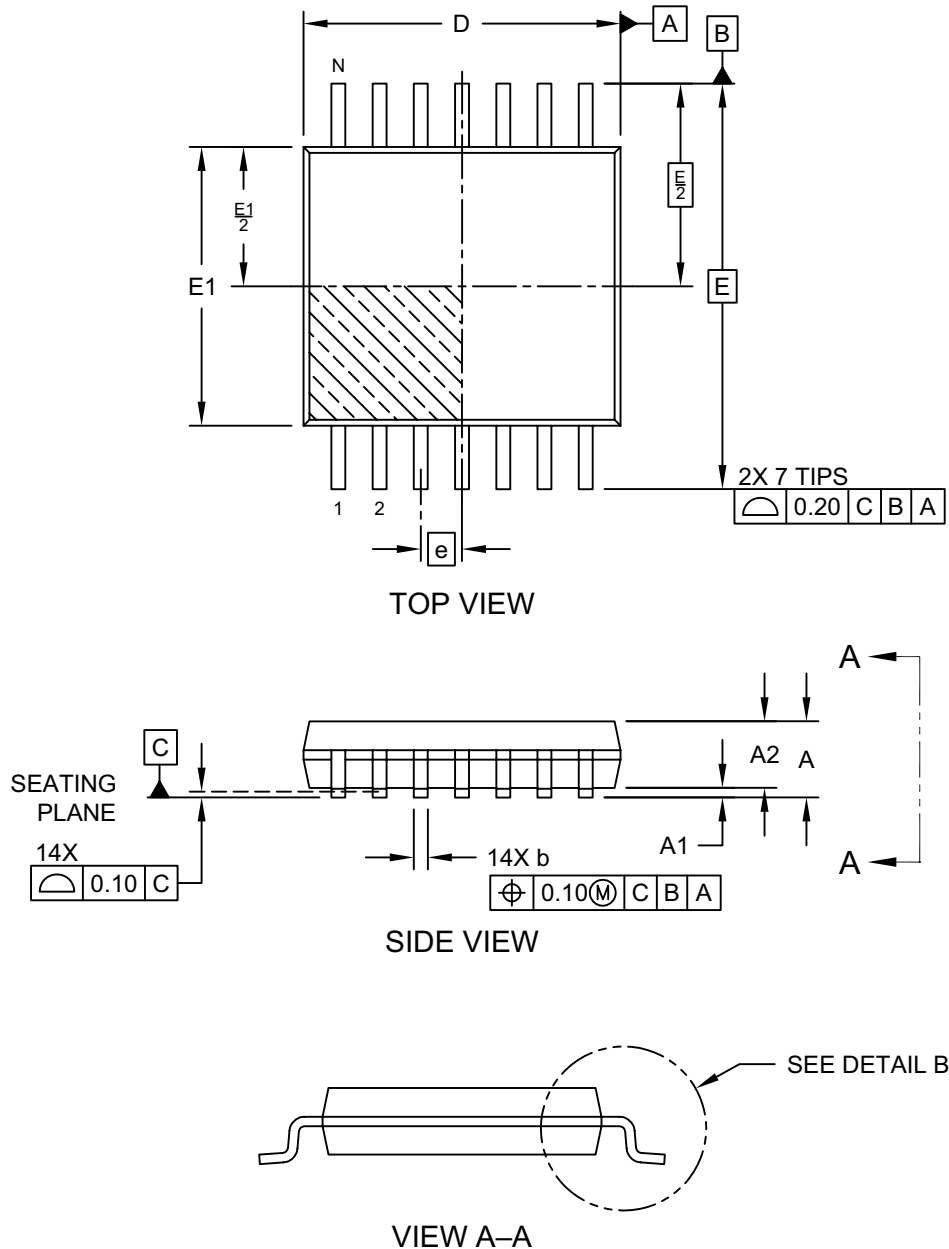
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

MCP6561/1R/1U/2/4

14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

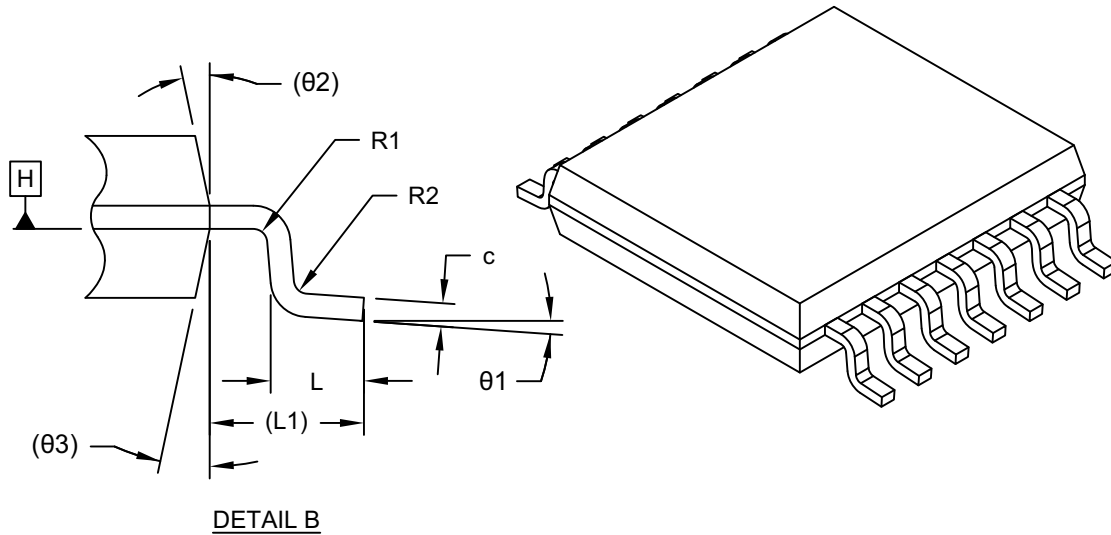
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-087 Rev D Sheet 1 of 2

14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

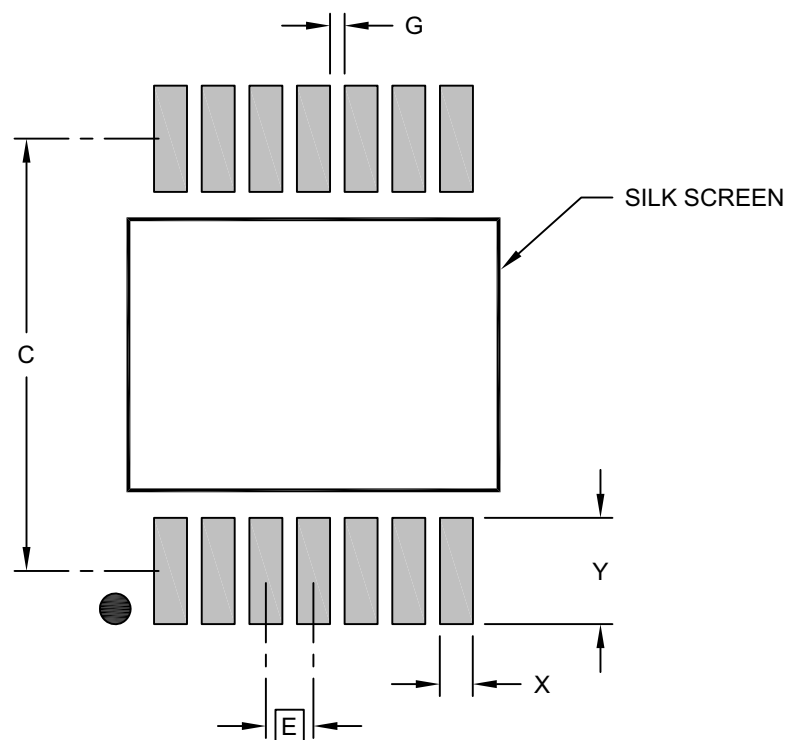
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

MCP6561/1R/1U/2/4

14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (Xnn)	X			0.45
Contact Pad Length (Xnn)	Y			1.45
Contact Pad to Contact Pad (Xnn)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087 Rev D

APPENDIX A: REVISION HISTORY

Revision E (March 2020)

The following is the list of modifications:

1. Updated package drawings for the 5-lead SC-70 and 14-lead TSSOP packages in [Section 6.0 “Packaging Information”](#).

Revision D (October 2019)

The following is the list of modifications:

1. Updated [Section 6.0 “Packaging Information”](#).

Revision C (February 2013)

The following is the list of modifications:

1. Added the Analog Input (V_{IN}) parameter in [Section 1.0 “Electrical Characteristics”](#).
2. Updated the package drawing section.

Revision B (August 2009)

The following is the list of modifications:

1. Added MCP6561U throughout the document.
2. Updated package drawing section.

Revision A (March 2009)

- Original Release of this Document.

MCP6561/1R/1U/2/4

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	-	<u>X</u>	<u>/XX</u>
Device		Temperature Range	Package
Device: - MCP6561T: Single Comparator (Tape and Reel) (SC70, SOT-23) - MCP6561RT: Single Comparator (Tape and Reel) (SOT-23 only) - MCP6561UT: Single Comparator (Tape and Reel) (SOT-23 only) - MCP6562: Dual Comparator - MCP6562T: Dual Comparator (Tape and Reel) - MCP6564: Quad Comparator - MCP6564T: Quad Comparator (Tape and Reel)			
Temperature Range: E = -40°C to +125°C			
Package: - LT = Plastic Small Outline Transistor (SC70), 5-Lead - OT = Plastic Small Outline Transistor (SOT-23), 5-Lead - MS = Plastic Micro Small Outline Transistor (MSOP), 8-Lead - SN = Plastic Small Outline Transistor (SOIC), 8-Lead - ST = Plastic Thin Shrink Small Outline Transistor (TSSOP), 14-Lead - SL = Plastic Small Outline Transistor (SOIC), 14-Lead			
Examples: a) MCP6561T-E/LT: Tape and Reel, Extended Temperature, 5-Lead SC70 Package. b) MCP6561T-E/OT: Tape and Reel, Extended Temperature, 5-Lead SOT-23 Package. a) MCP6561RT-E/OT: Tape and Reel, Extended Temperature, 5-Lead SOT-23 Package. a) MCP6561UT-E/OT: Tape and Reel, Extended Temperature, 5-Lead SOT-23 Package. a) MCP6562-E/MS: Extended Temperature, 8-Lead MSOP Package. b) MCP6562-E/SN: Extended Temperature, 8-Lead SOIC Package. a) MCP6564T-E/SL: Tape and Reel, Extended Temperature, 14-Lead SOIC Package. b) MCP6564T-E/ST: Tape and Reel, Extended Temperature, 14-Lead TSSOP Package.			

MCP6561/1R/1U/2/4

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TempTrackr, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, Vite, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2009-2020, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-5713-8

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820