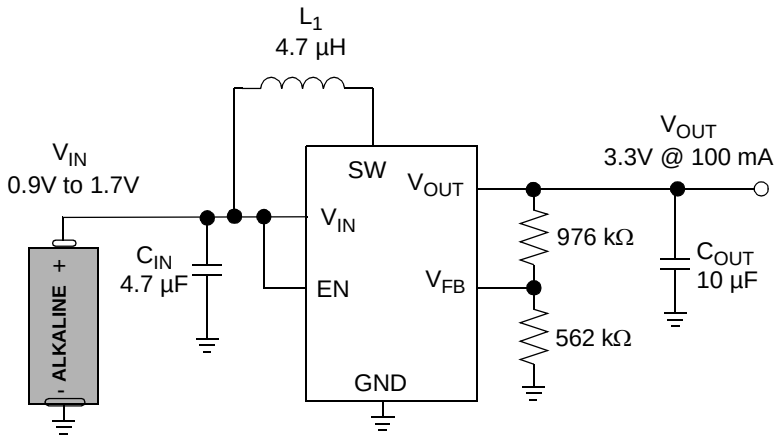
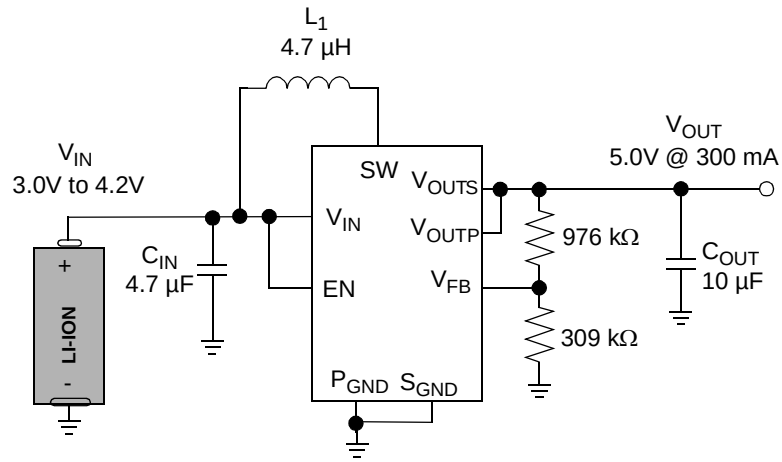
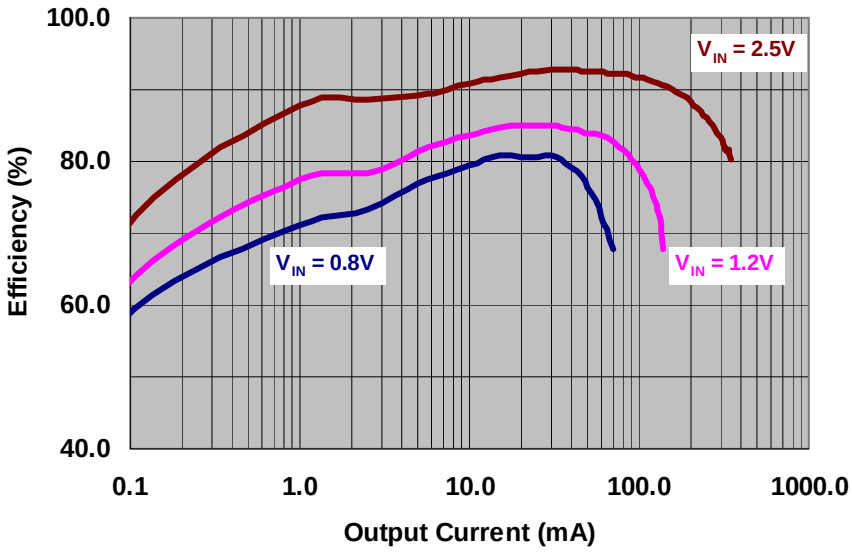
Typical Application





Efficiency vs. I_{OUT} for $3.3V_{OUT}$



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

EN, V_{FB}, V_{IN}, V_{SW}, V_{OUT} - GND .....+6.5V
EN, V_{FB} ....<maximum of V_{OUT} or V_{IN} > (GND – 0.3V)
Output Short-Circuit Current ..... Continuous
Output Current Bypass Mode.....400 mA
Power Dissipation ..... Internally Limited
Storage Temperature .....-65°C to +150°C
Ambient Temp. with Power Applied.....-40°C to +85°C
Operating Junction Temperature.....-40°C to +125°C
ESD Protection On All Pins:
HBM..... 3 kV
MM.....300V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{IN} = 1.2V, C_{OUT} = C_{IN} = 10 µF, L = 4.7 µH, V_{OUT} = 3.3V, I_{OUT} = 15 mA, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +85°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Minimum Start-Up Voltage	V_{IN}	—	0.65	**0.8**	V	Note 1
Minimum Input Voltage After Start-Up	V_{IN}	—	0.35	—	V	Note 1
Output Voltage Adjust Range	V_{OUT}	**2.0**		**5.5**	V	$V_{OUT} \geq V_{IN}$; Note 2
Maximum Output Current	I_{OUT}	—	150	—	mA	1.2V V_{IN}, 2.0V V_{OUT}
		—	150	—	mA	1.5V V_{IN}, 3.3V V_{OUT}
		—	350	—	mA	3.3V V_{IN}, 5.0V V_{OUT}
Feedback Voltage	V_{FB}	**1.175**	1.21	**1.245**	V	
Feedback Input Bias Current	I_{VFB}	—	10	—	pA	
Quiescent Current – PFM Mode	I_{QPFM}	—	19	30	µA	Measured at V_{OUT} = 4.0V; EN = V_{IN}, I_{OUT} = 0 mA; Note 3
Quiescent Current – PWM Mode	I_{QPWM}	—	220	—	µA	Measured at V_{OUT} = 4.0V; EN = V_{IN}, I_{OUT} = 0 mA; Note 3
Quiescent Current – Shutdown	$I_{Q\overline{SHDN}}$	—	0.7	2.3	µA	V_{OUT} = EN = GND; Includes N-Channel and P-Channel Switch Leakage
NMOS Switch Leakage	I_{NLK}	—	0.3	—	µA	V_{IN} = V_{SW} = 5V; V_{OUT} = 5.5V V_{EN} = V_{FB} = GND
PMOS Switch Leakage	I_{PLK}	—	0.05	—	µA	V_{IN} = VS_W = GND; V_{OUT} = 5.5V

Note 1: 3.3 kΩ resistive load, 3.3V_{OUT} (1 mA).
2: For V_{IN} > V_{OUT}, V_{OUT} will not remain in regulation.
3: I_{QOUT} is measured at V_{OUT}; V_{OUT} is externally supplied with a voltage higher than the nominal 3.3V output (device is not switching); no load; V_{IN} quiescent current will vary with boost ratio. V_{IN} quiescent current can be estimated by: (I_{QPFM} * (V_{OUT}/V_{IN})), (I_{QPWM} * (V_{OUT}/V_{IN})).
4: Peak current limit determined by characterization, not production tested.
5: 220Ω resistive load, 3.3V_{OUT} (15 mA).

DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{IN} = 1.2V, C_{OUT} = C_{IN} = 10 µF, L = 4.7 µH, V_{OUT} = 3.3V, I_{OUT} = 15 mA, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +85°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
NMOS Switch On Resistance	$R_{DS(ON)N}$	—	0.6	—	Ω	V_{IN} = 3.3V, I_{SW} = 100 mA
PMOS Switch On Resistance	$R_{DS(ON)P}$	—	0.9	—	Ω	V_{IN} = 3.3V, I_{SW} = 100 mA
NMOS Peak Switch Current Limit	$I_{N(MAX)}$	600	850	—	mA	Note 4
V_{OUT} Accuracy	V_{OUT}%	**-3**	—	**+3**	%	Includes Line and Load Regulation; V_{IN} = 1.5V
Line Regulation	$\lvert(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}\rvert$	**-1**	0.01	**1**	%/V	V_{IN} = 1.5V to 3V I_{OUT} = 25 mA
Load Regulation	$\lvert\Delta V_{OUT}/V_{OUT}\rvert$	**-1**	0.01	**1**	%	I_{OUT} = 25 mA to 100 mA; V_{IN} = 1.5V
Maximum Duty Cycle	DC_{MAX}	88	90	—	%	
Switching Frequency	f_{SW}	**425**	500	**575**	kHz	
EN Input Logic High	V_{IH}	**90**	—	—	%of V_{IN}	I_{OUT} = 1 mA
EN Input Logic Low	V_{IL}	—	—	**20**	%of V_{IN}	I_{OUT} = 1 mA
EN Input Leakage Current	I_{ENLK}	—	0.005	—	µA	V_{EN} = 5V
Soft-Start Time	t_{SS}	—	750	—	µS	EN Low-to-High, 90% of V_{OUT}; Note 5
Thermal Shutdown Die Temperature	T_{SD}	—	150	—	°C	
Die Temperature Hysteresis	T_{SDHYS}	—	10	—	°C	

Note 1: 3.3 kΩ resistive load, 3.3V_{OUT} (1 mA).

2: For V_{IN} > V_{OUT}, V_{OUT} will not remain in regulation.

3: I_{QOUT} is measured at V_{OUT}; V_{OUT} is externally supplied with a voltage higher than the nominal 3.3V output (device is not switching); no load; V_{IN} quiescent current will vary with boost ratio. V_{IN} quiescent current can be estimated by: (I_{QPFM} * (V_{OUT}/V_{IN})), (I_{QPWM} * (V_{OUT}/V_{IN})).

4: Peak current limit determined by characterization, not production tested.

5: 220Ω resistive load, 3.3V_{OUT} (15 mA).

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{IN} = 1.2V, C_{OUT} = C_{IN} = 10 µF, L = 4.7 µH, V_{OUT} = 3.3V, I_{OUT} = 15 mA.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	Steady State
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Package Thermal Resistances						
Thermal Resistance, 6LD-SOT-23	θ_{JA}	—	190.5	—	°C/W	
Thermal Resistance, 8LD-2x3 DFN	θ_{JA}	—	75	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = EN = 1.2V, C_{OUT} = C_{IN} = 10 µF, L = 4.7 µH, V_{OUT} = 3.3V, I_{LOAD} = 15 mA, T_A = +25°C.

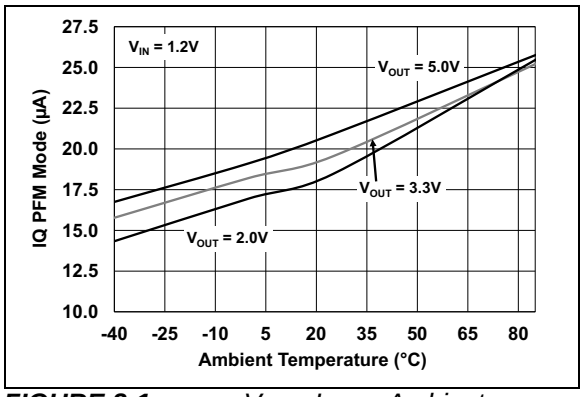


FIGURE 2-1: *V_{OUT} I_Q vs. Ambient Temperature in PFM Mode.*

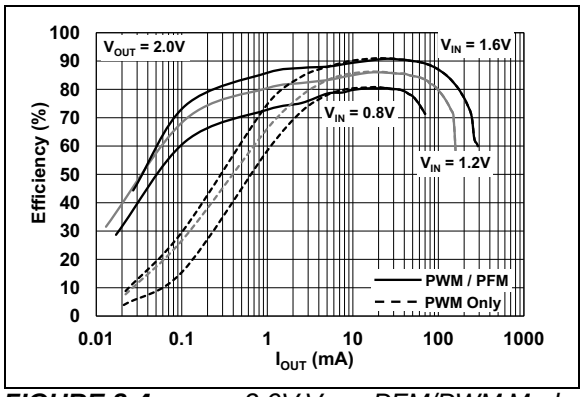


FIGURE 2-4: *2.0V V_{OUT} PFM/PWM Mode Efficiency vs. I_{OUT}.*

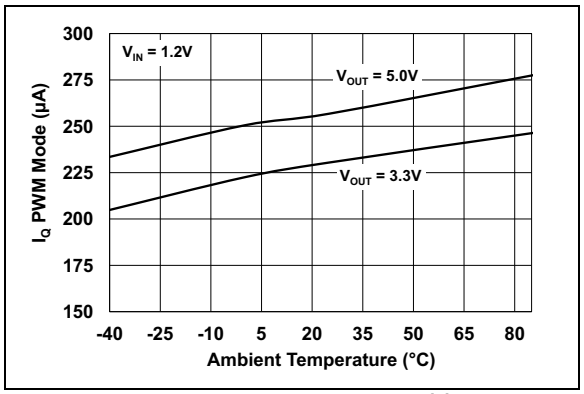


FIGURE 2-2: *V_{OUT} I_Q vs. Ambient Temperature in PWM Mode.*

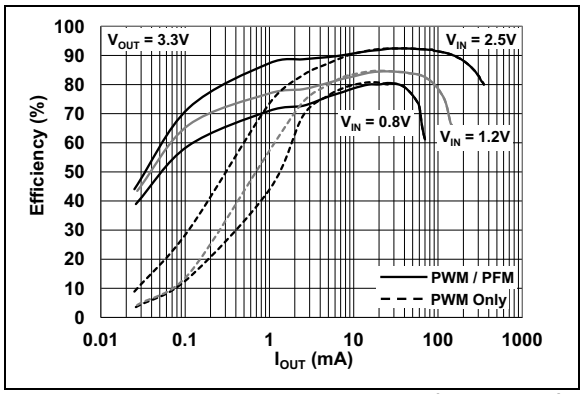


FIGURE 2-5: *3.3V V_{OUT} PFM/PWM Mode Efficiency vs. I_{OUT}.*

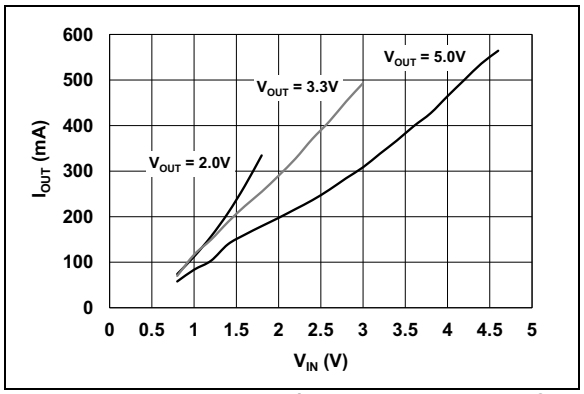


FIGURE 2-3: *Maximum I_{OUT} vs. V_{IN} After Start-Up, V_{OUT} 10% Below Regulation Point.*

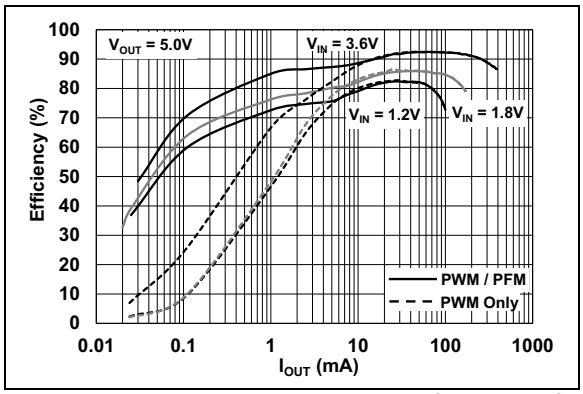


FIGURE 2-6: *5.0V V_{OUT} PFM/PWM Mode Efficiency vs. I_{OUT}.*

Note: Unless otherwise indicated, V_{IN} = EN = 1.2V, C_{OUT} = C_{IN} = 10 µF, L = 4.7 µH, V_{OUT} = 3.3V, I_{LOAD} = 15 mA, T_A = +25°C.

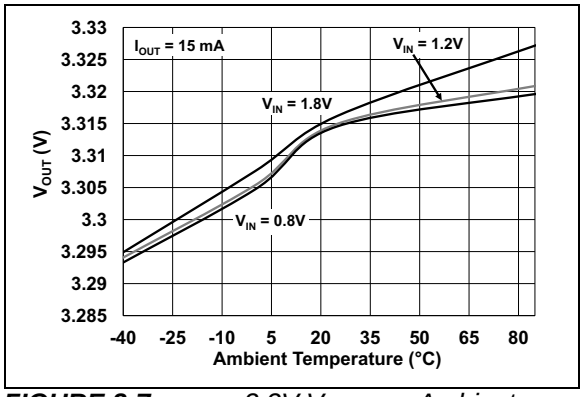


FIGURE 2-7: *3.3V V_{OUT} vs. Ambient Temperature.*

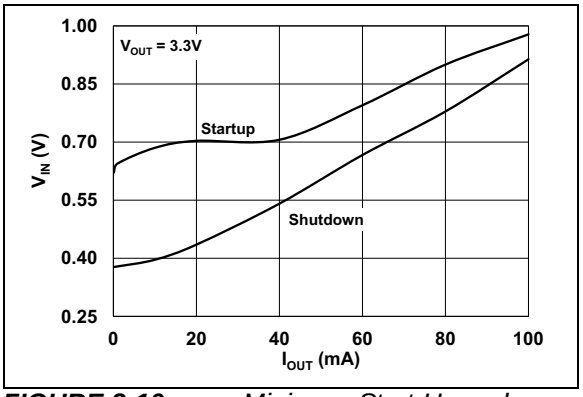


FIGURE 2-10: *Minimum Start-Up and Shutdown V_{IN} into Resistive Load vs. I_{OUT}.*

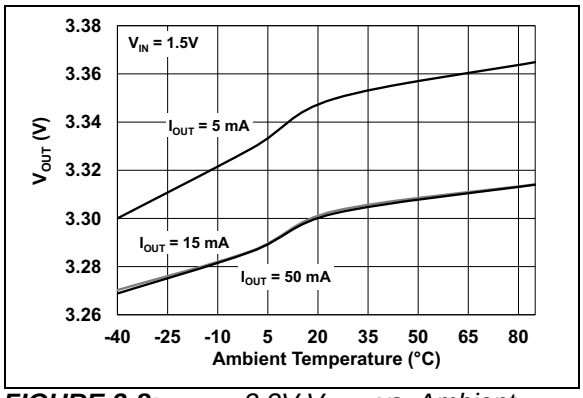


FIGURE 2-8: *3.3V V_{OUT} vs. Ambient Temperature.*

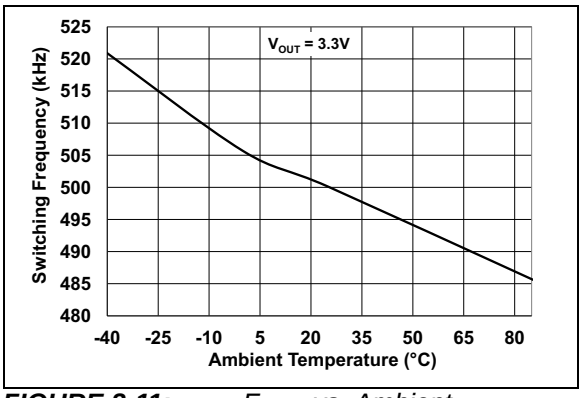


FIGURE 2-11: *F_{OSC} vs. Ambient Temperature.*

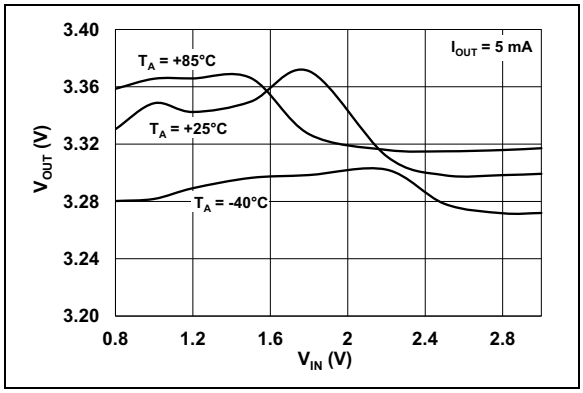


FIGURE 2-9: *3.3V V_{OUT} vs. V_{IN}.*

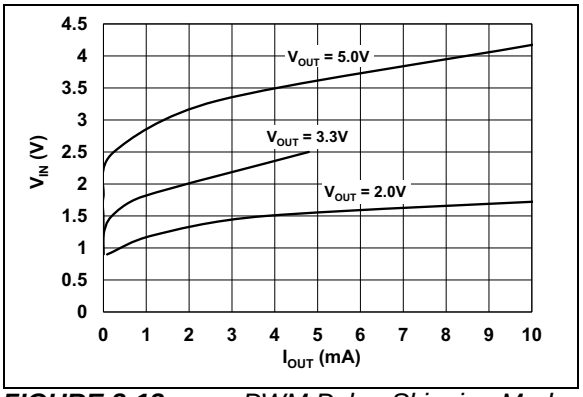


FIGURE 2-12: *PWM Pulse-Skipping Mode Threshold vs. I_{OUT}.*

Note: Unless otherwise indicated, V_{IN} = EN = 1.2V, C_{OUT} = C_{IN} = 10 µF, L = 4.7 µH, V_{OUT} = 3.3V, I_{LOAD} = 15 mA, T_A = +25°C.

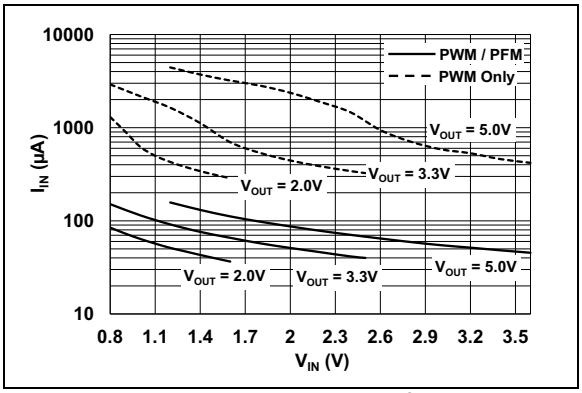


FIGURE 2-13: *Input No Load Current vs. V_{IN}.*

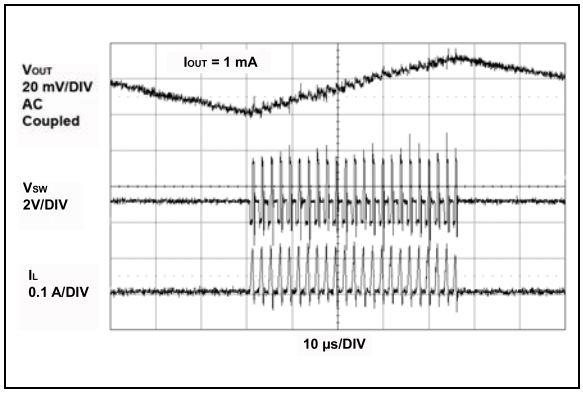


FIGURE 2-16: *MCP1640 3.3V V_{OUT} PFM Mode Waveforms.*

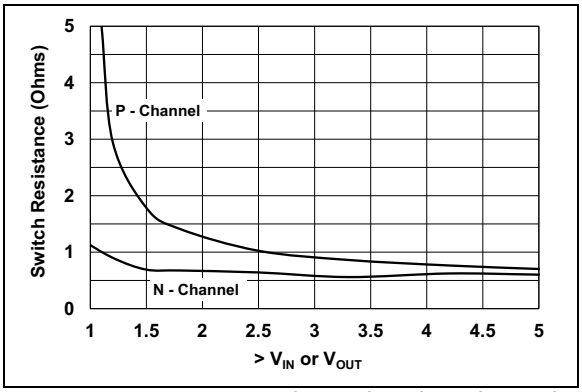


FIGURE 2-14: *N-Channel and P-Channel R_{DSON} vs. > of V_{IN} or V_{OUT}.*

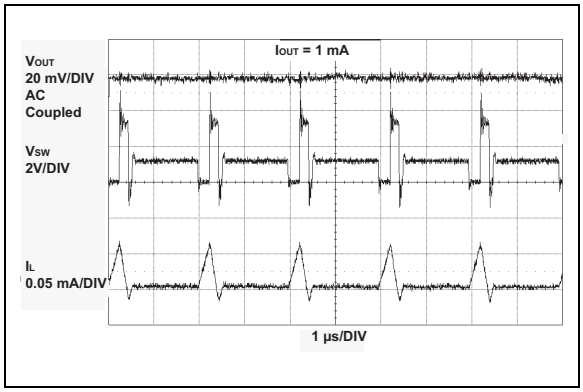


FIGURE 2-17: *MCP1640B 3.3V V_{OUT} PWM Mode Waveforms.*

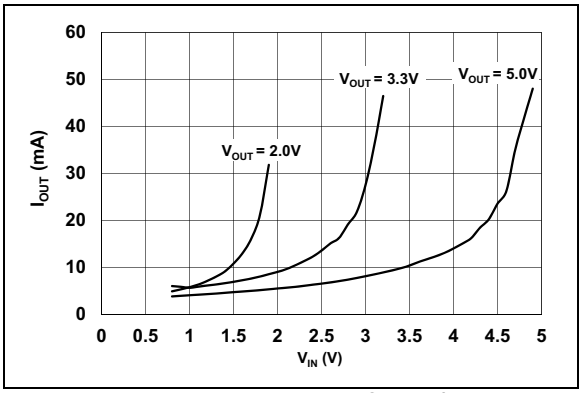


FIGURE 2-15: *Average of PFM/PWM Threshold Current vs. V_{IN}.*

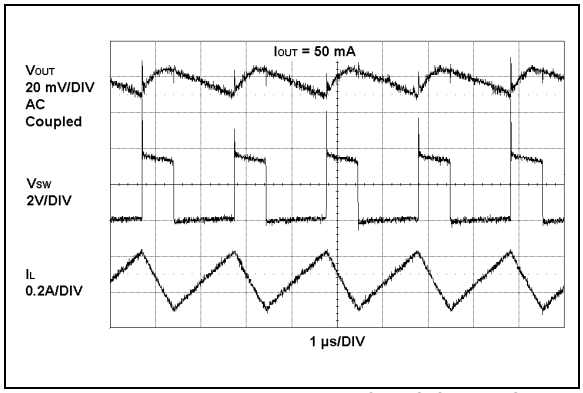


FIGURE 2-18: *MCP1640/B High Load Waveforms.*

Note: Unless otherwise indicated, V_{IN} = EN = 1.2V, C_{OUT} = C_{IN} = 10 µF, L = 4.7 µH, V_{OUT} = 3.3V, I_{LOAD} = 15 mA, T_A = +25°C.

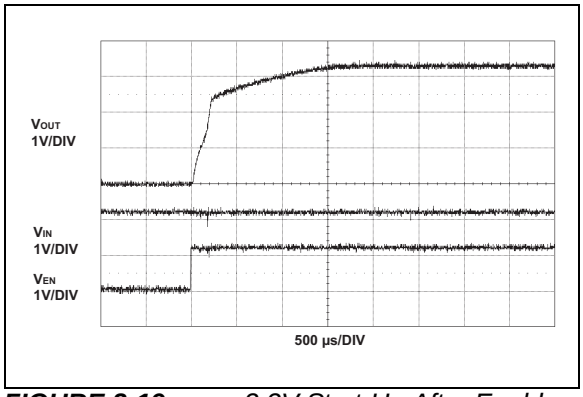


FIGURE 2-19: *3.3V Start-Up After Enable.*

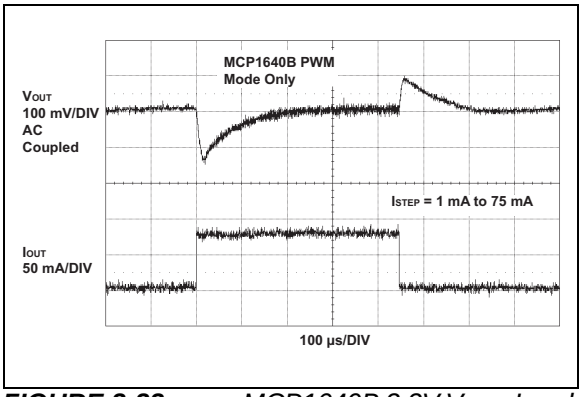


FIGURE 2-22: *MCP1640B 3.3V V_{OUT} Load Transient Waveforms.*

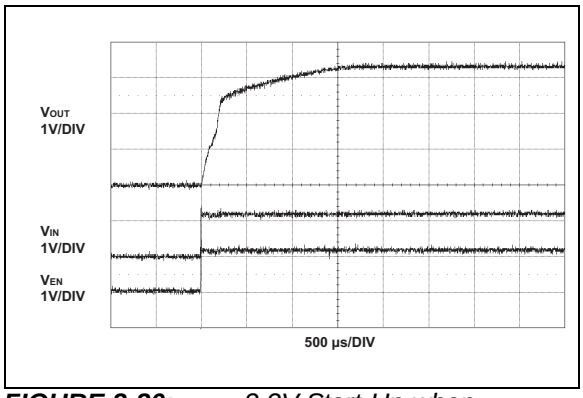


FIGURE 2-20: *3.3V Start-Up when $V_{IN} = V_{ENABLE}$.*

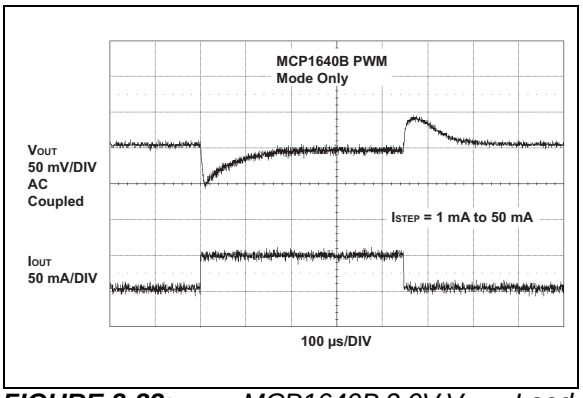


FIGURE 2-23: *MCP1640B 2.0V V_{OUT} Load Transient Waveforms.*

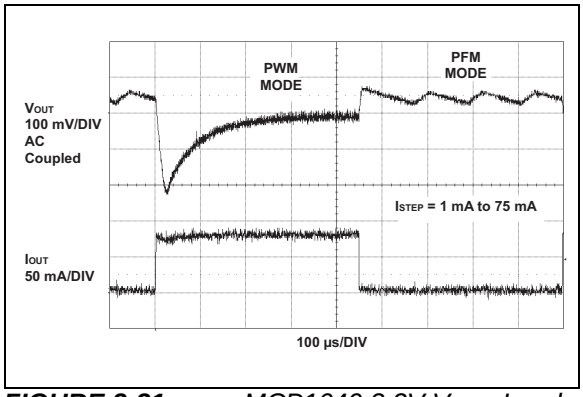


FIGURE 2-21: *MCP1640 3.3V V_{OUT} Load Transient Waveforms.*

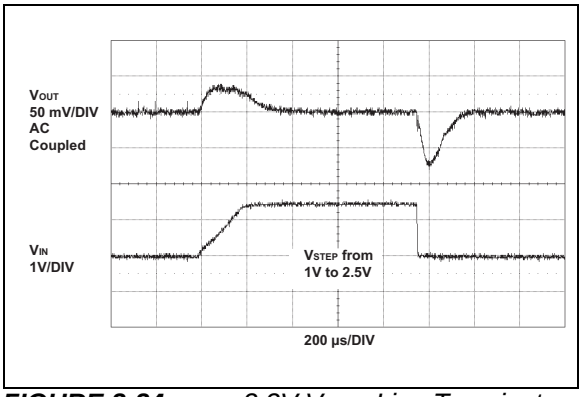


FIGURE 2-24: *3.3V V_{OUT} Line Transient Waveforms.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP1640/B/C/D 2x3 DFN	MCP1640/B/C/D SOT-23	Symbol	Description
1	4	V_{FB}	Feedback Voltage Pin
2	—	S_{GND}	Signal Ground Pin
3	—	P_{GND}	Power Ground Pin
4	3	EN	Enable Control Input Pin
5	1	SW	Switch Node, Boost Inductor Input Pin
6	—	V_{OUTP}	Output Voltage Power Pin
7	—	V_{OUTS}	Output Voltage Sense Pin
8	6	V_{IN}	Input Voltage Pin
9	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}
—	2	GND	Ground Pin
—	5	V_{OUT}	Output Voltage Pin

3.1 Feedback Voltage Pin (V_{FB})

The V_{FB} pin is used to provide output voltage regulation by using a resistor divider. Feedback voltage will be 1.21V typical with the output voltage in regulation.

3.2 Signal Ground Pin (S_{GND})

The signal ground pin is used as a return for the integrated V_{REF} and error amplifier. In the 2x3 DFN package, the S_{GND} and power ground (P_{GND}) pins are connected externally.

3.3 Power Ground Pin (P_{GND})

The power ground pin is used as a return for the high-current N-Channel switch. In the 2x3 DFN package, the P_{GND} and S_{GND} pins are connected externally.

3.4 Enable Pin (EN)

The EN pin is a logic-level input used to enable or disable device switching and lower quiescent current while disabled. A logic high (>90% of V_{IN}) will enable the regulator output. A logic low (<20% of V_{IN}) will ensure that the regulator is disabled.

3.5 Switch Node Pin (SW)

Connect the inductor from the input voltage to the SW pin. The SW pin carries inductor current and can be as high as 800 mA peak. The integrated N-Channel switch drain and integrated P-Channel switch source are internally connected at the SW node.

3.6 Output Voltage Power Pin (V_{OUTP})

The output voltage power pin connects the output voltage to the switch node. High current flows through the integrated P-Channel and out of this pin to the output capacitor and the output. In the 2x3 DFN package, V_{OUTP} and V_{OUTS} are connected externally.

3.7 Output Voltage Sense Pin (V_{OUTS})

The output voltage sense pin connects the regulated output voltage to the internal bias circuits. In the 2x3 DFN package, the V_{OUTS} and output voltage power (V_{OUTP}) pins are connected externally.

3.8 Power Supply Input Voltage Pin (V_{IN})

Connect the input voltage source to V_{IN}. The input source should be decoupled to GND with a 4.7 µF minimum capacitor.

3.9 Exposed Thermal Pad (EP)

There is no internal electrical connection between the Exposed Thermal Pad (EP) and the S_{GND} and P_{GND} pins. They must be connected to the same potential on the Printed Circuit Board (PCB).

3.10 Ground Pin (GND)

The ground or return pin is used for circuit ground connection. Length of trace from input cap return, output cap return, and GND pin should be made as short as possible to minimize noise on the GND pin. In the SOT-23-6 package, a single ground pin is used.

3.11 Output Voltage Pin (V_{OUT})

The output voltage pin connects the integrated P-Channel MOSFET to the output capacitor. The FB voltage divider is also connected to the V_{OUT} pin for voltage regulation.

NOTES:

4.0 DETAILED DESCRIPTION

4.1 Device Option Overview

The MCP1640/B/C/D family of devices is capable of low start-up voltage and delivers high efficiency over a wide load range for single-cell, two-cell, or three-cell alkaline, NiCd, NiMH and single-cell Li-Ion battery inputs. A high level of integration lowers total system cost, eases implementation and reduces board area.

The devices feature low start-up voltage, adjustable output voltage, PWM/PFM mode operation, low I_Q, integrated synchronous switch, internal compensation, low noise anti-ring control, inrush current limit, and soft start.

There are two options for the MCP1640/B/C/D family:

- PWM/PFM mode or PWM-Only mode
- "True Output Disconnect" mode or Input-to-Output Bypass mode

4.1.1 PWM/PFM MODE OPTION

The MCP1640/C devices use an automatic switchover from PWM to PFM mode for light load conditions to maximize efficiency over a wide range of output current. During PFM mode, higher peak current is used to pump the output up to the threshold limit. While operating in PFM or PWM mode, the P-Channel switch is used as a synchronous rectifier, turning off when the inductor current reaches 0 mA to maximize efficiency.

In PFM mode, a comparator is used to terminate switching when the output voltage reaches the upper threshold limit. Once switching has terminated, the output voltage will decay or coast down. During this period, very low I_Q is consumed from the device and input source, which keeps power efficiency high at light load.

The disadvantages of PWM/PFM mode are higher output ripple voltage and variable PFM mode frequency. The PFM mode frequency is a function of input voltage, output voltage and load. While in PFM mode, the boost converter pumps the output up at a switching frequency of 500 kHz.

4.1.2 PWM-ONLY MODE OPTION

The MCP1640B/D devices disable PFM mode switching, and operate only in PWM mode over the entire load range. During periods of light load operation, the MCP1640B/D continues to operate at a constant 500 kHz switching frequency, keeping the output ripple voltage lower than PFM mode.

During PWM-Only mode, the MCP1640B/D P-Channel switch acts as a synchronous rectifier by turning off (to prevent reverse current flow from the output cap back to the input) in order to keep efficiency high.

For noise immunity, the N-Channel MOSFET current sense is blanked for approximately 100 ns. With a typical minimum duty cycle of 100 ns, the MCP1640B/D continues to switch at a constant frequency under light load conditions. Figure 2-12 represents the input voltage versus load current for the pulse skipping threshold in PWM-Only mode. At lighter loads, the MCP1640B/D devices begin to skip pulses.

4.1.3 TRUE OUTPUT DISCONNECT MODE OPTION

The MCP1640/B devices incorporate a true output disconnect feature. With the EN pin pulled low, the output of the MCP1640/B is isolated or disconnected from the input by turning off the integrated P-Channel switch and removing the switch bulk diode connection. This removes the DC path that is typical in boost converters, which allows the output to be disconnected from the input. During this mode, less than 1 µA of current is consumed from the input (battery). True output disconnect does not discharge the output; the output voltage is held up by the external C_{OUT} capacitance.

4.1.4 INPUT BYPASS MODE OPTION

The MCP1640C/D devices incorporate the Input Bypass shutdown option. With the EN input pulled low, the output is connected to the input using the internal P-Channel MOSFET. In this mode, the current draw from the input (battery) is less than 1 µA with no load. Input Bypass mode is used when the input voltage range is high enough for the load to operate in Sleep or Low I_Q mode. When a higher regulated output voltage is necessary to operate the application, the EN input is pulled high, enabling the boost converter.

TABLE 4-1: PART NUMBER SELECTION

Part Number	PWM/ PFM	PWM -Only	True Disconnect	Input -to- Output Bypass
MCP1640	X		X	
MCP1640B		X	X	
MCP1640C	X			X
MCP1640D		X		X

4.2 Functional Description

The MCP1640/B/C/D is a compact, high-efficiency, fixed frequency, step-up DC-DC converter that provides an easy-to-use power supply solution for applications powered by either single-cell, two-cell, or three-cell alkaline, NiCd, NiMH, and single-cell Li-Ion or Li-Polymer batteries.

Figure 4-1 depicts the functional block diagram of the MCP1640/B/C/D.

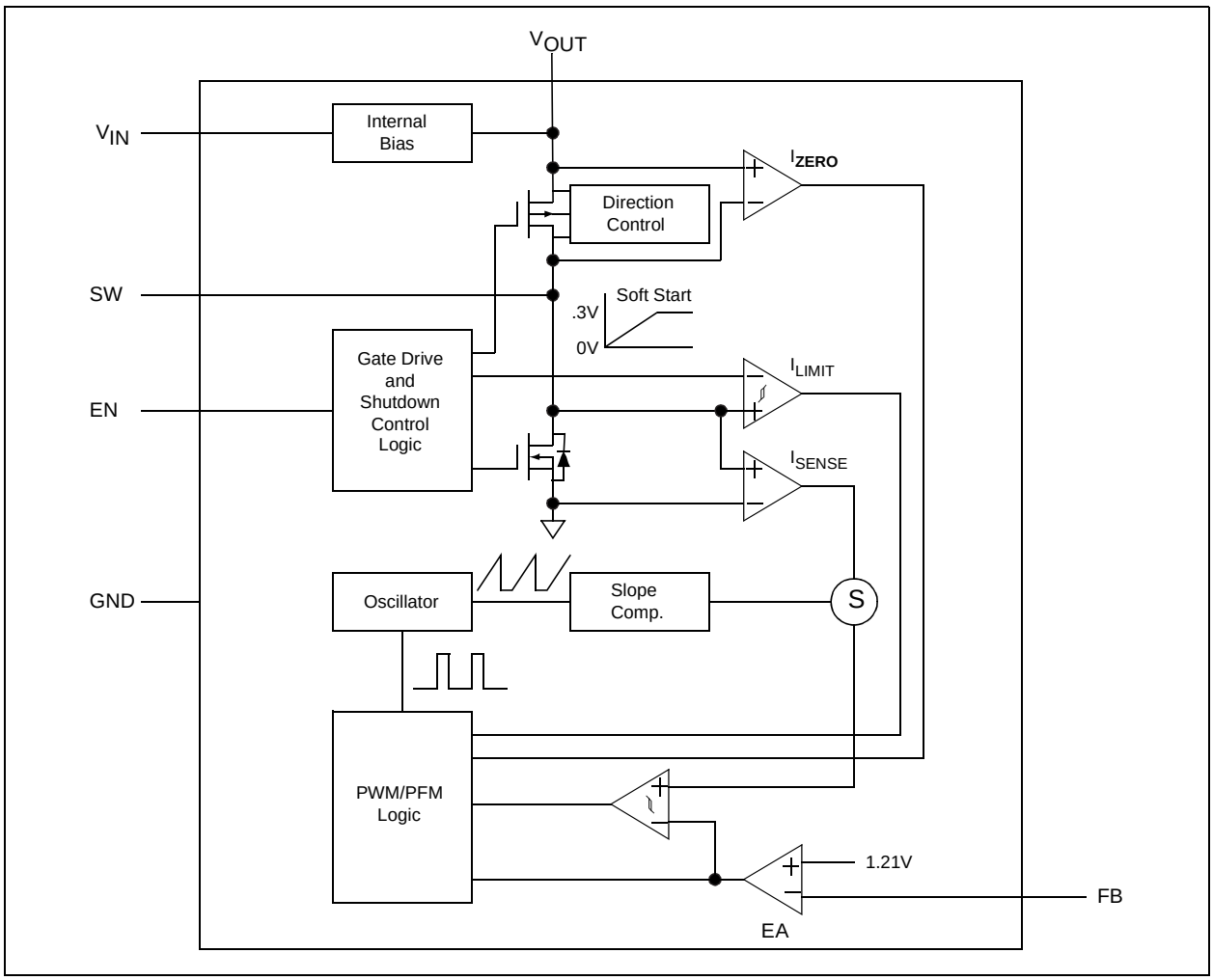


FIGURE 4-1: *MCP1640/B/C/D Block Diagram.*

4.2.1 LOW-VOLTAGE START-UP

The MCP1640/B/C/D is capable of starting from a low input voltage. Start-up voltage is typically 0.65V for a 3.3V output and 1 mA resistive load.

When enabled, the internal start-up logic turns the rectifying P-Channel switch on until the output capacitor is charged to a value close to the input voltage. The rectifying switch is current-limited to approximately 100 mA during this time. This will affect the start-up under higher load currents, and the device may not start to the nominal value. After charging the output capacitor to the input voltage, the device starts switching. If the input voltage is below 1.6V, the device runs open-loop with a fixed duty cycle of 70% until the output reaches 1.6V. During this time, the boost switch current is limited to 50% of its nominal value. Once the output voltage reaches 1.6V, normal closed-loop PWM operation is initiated.

The MCP1640/B/C/D charges an internal capacitor with a very weak current source. The voltage on this capacitor, in turn, slowly ramps the current limit of the boost switch to its nominal value. The soft-start capacitor is completely discharged in the event of a commanded shutdown or a thermal shutdown.

There is no undervoltage lockout feature for the MCP1640/B/C/D. The device will start-up at the lowest possible voltage and run down to the lowest possible voltage. For typical battery applications, this may result in “motor-boating” (emitting a low-frequency tone) for deeply discharged batteries.

4.2.2 PWM-ONLY MODE OPERATION

In normal PWM operation, the MCP1640/B/C/D operates as a fixed frequency, synchronous boost converter. The switching frequency is internally maintained with a precision oscillator typically set to 500 kHz. The MCP1640B/D devices will operate in PWM-Only mode even during periods of light load operation. By operating in PWM-Only mode, the output ripple remains low and the frequency is constant. Operating in fixed PWM mode results in lower efficiency during light load operation (when compared to PFM mode (MCP1640/C)).

Lossless current sensing converts the peak current signal to a voltage to sum with the internal slope compensation. This summed signal is compared to the voltage error amplifier output to provide a peak current control command for the PWM signal. The slope compensation is adaptive to the input and output voltage. Therefore, the converter provides the proper amount of slope compensation to ensure stability, but is not excessive, which causes a loss of phase margin. The peak current limit is set to 800 mA typical.

4.2.3 PFM MODE OPERATION

The MCP1640/C devices are capable of operating in normal PWM mode and PFM mode to maintain high efficiency at all loads. In PFM mode, the output ripple has a variable frequency component that changes with the input voltage and output current. The value of the output capacitor changes the low-frequency component ripple. Output ripple peak-to-peak values are not affected by the output capacitor. With no load, the quiescent current draw from the output is typically 19 µA. This is not a switching current and is not dependent on the input and output parameters. The no-load input current drawn from the battery depends on the above parameters. Its variation is shown in Figure 2-13. The PFM mode can be disabled in selected device options.

PFM operation is initiated if the output load current falls below an internally programmed threshold. The output voltage is continuously monitored. When the output voltage drops below its nominal value, PFM operation pulses one or several times to bring the output back into regulation. If the output load current rises above the upper threshold, the MCP1640/C transitions smoothly into PWM mode.

4.2.4 ADJUSTABLE OUTPUT VOLTAGE

The MCP1640/B/C/D output voltage is adjustable with a resistor divider over a 2.0V minimum to 5.5V maximum range. High-value resistors can be used to minimize quiescent current to keep efficiency high at light loads.

4.2.5 ENABLE PIN

The enable pin is used to turn the boost converter on and off. The enable threshold voltage varies with input voltage. To enable the boost converter, the EN voltage level must be greater than 90% of the V_{IN} voltage. To disable the boost converter, the EN voltage must be less than 20% of the V_{IN} voltage.

4.2.6 INTERNAL BIAS

The MCP1640/B/C/D gets its start-up bias from V_{IN}. Once the output exceeds the input, bias comes from the output. Therefore, once started, operation is completely independent of V_{IN}. Operation is only limited by the output power level and the input source series resistance. When started, the output will remain in regulation down to 0.35V typical with 1 mA output current for low source impedance inputs.

4.2.7 INTERNAL COMPENSATION

The error amplifier, with its associated compensation network, completes the closed-loop system by comparing the output voltage to a reference at the input of the error amplifier, and feeding the amplified and inverted signal to the control input of the inner current loop. The compensation network provides phase leads and lags at appropriate frequencies to cancel excessive phase lags and leads of the power circuit. All necessary compensation components and slope compensation are integrated.

4.2.8 SHORT CIRCUIT PROTECTION

Unlike most boost converters, the MCP1640/B/C/D allows its output to be shorted during normal operation. The internal current limit and overtemperature protection limit excessive stress and protect the device during periods of short circuit, overcurrent and overtemperature. While operating in Bypass mode, the P-Channel current limit is inhibited to minimize quiescent current.

4.2.9 LOW NOISE OPERATION

The MCP1640/B/C/D integrates a low noise anti-ring switch that damps the oscillations typically observed at the switch node of a boost converter when operating in the Discontinuous Inductor Current mode. This removes the high-frequency radiated noise.

4.2.10 OVERTEMPERATURE PROTECTION

Overtemperature protection circuitry is integrated into the MCP1640/B/C/D. This circuitry monitors the device junction temperature and shuts the device off if the junction temperature exceeds the typical +150°C threshold. If this threshold is exceeded, the device will automatically restart when the junction temperature drops by 10°C. The soft start is reset during an overtemperature condition.

NOTES:

5.0 APPLICATION INFORMATION

5.1 Typical Applications

The MCP1640/B/C/D synchronous boost regulator operates over a wide input and output voltage range. The power efficiency is high for several decades of load range. Output current capability increases with input voltage and decreases with increasing output voltage. The maximum output current is based on the N-Channel peak current limit. Typical characterization curves in this data sheet are presented to display the typical output current capability.

5.2 Adjustable Output Voltage Calculations and Maximum Output Current

To calculate the resistor divider values for the MCP1640/B/C/D, the following equation can be used, where R_{TOP} is connected to V_{OUT}, R_{BOT} is connected to GND and both are connected to the FB input pin.

EQUATION 5-1:

$$R_{TOP} = R_{BOT} \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

EXAMPLE 1:

V_{OUT} = 3.3V
V_{FB} = 1.21V
R_{BOT} = 309 kΩ
R_{TOP} = 533.7 kΩ (Standard Value = 536 kΩ)

EXAMPLE 2:

V_{OUT} = 5.0V
V_{FB} = 1.21V
R_{BOT} = 309 kΩ
R_{TOP} = 967.9 kΩ (Standard Value = 976 kΩ)

The internal error amplifier is of transconductance type; its gain is not related to the resistors' value. There are some potential issues with higher-value resistors. For small surface-mount resistors, environment contamination can create leakage paths that significantly change the resistor divider ratio and modify the output voltage tolerance.

Smaller feedback resistor values will increase the current drained from the battery by a few µA, but will result in good regulation over the entire temperature range and environment conditions. The feedback input leakage current can also impact the divider and change the output voltage tolerance.

For boost converters, the removal of the feedback resistors during operation must be avoided. In this case, the output voltage will increase above the absolute maximum output limits of the MCP1640/B/C/D and damage the device.

The maximum device output current is dependent upon the input and output voltage. For example, to ensure a 100 mA load current for V_{OUT} = 3.3V, a minimum of 1.0-1.1V input voltage is necessary. If an application is powered by one Li-Ion battery (V_{IN} from 3.0V to 4.2V), the minimum load current the MCP1640/B/C/D can deliver is close to 300 mA at 5.0V output and a maximum of 500 mA (Figure 2-3).

5.2.1 $V_{IN} > V_{OUT}$ SITUATION

For $V_{IN} > V_{OUT}$, the output voltage will not remain in regulation. $V_{IN} > V_{OUT}$ is an unusual situation for a boost converter, and there is a common issue when two Alkaline cells (2 x 1.6V typical) are used to boost to 3.0V output. The Input-to-Output Bypass option is recommended to be used in this situation until the batteries' voltages go down to a safe headroom. A minimum headroom of approximately 150 to 200 mV between V_{OUT} and V_{IN} must be ensured, unless a low-frequency, high-amplitude output ripple on V_{OUT} is expected. The ripple and its frequency is V_{IN} and load dependent. The higher the V_{IN}, the higher the ripple and the lower its frequency.

5.3 Input Capacitor Selection

The boost input current is smoothed by the boost inductor reducing the amount of filtering necessary at the input. Some capacitance is recommended to provide decoupling from the source. Low ESR X5R or X7R are well suited since they have a low temperature coefficient and small size. For most applications, 4.7 µF of capacitance is sufficient at the input. For high-power applications that have high source impedance or long leads, connecting the battery to the input 10 µF of capacitance is recommended. Additional input capacitance can be added to provide a stable input voltage.

Table 5-1 contains the recommended range for the input capacitor value.

5.4 Output Capacitor Selection

The output capacitor helps provide a stable output voltage during sudden load transients and reduces the output voltage ripple. As with the input capacitor, X5R and X7R ceramic capacitors are well suited for this application. Using other capacitor types (aluminum or tantalum) with large ESR has an impact on the converter's efficiency and maximum output power (see AN1337).

The MCP1640/B/C/D is internally compensated, so output capacitance range is limited (see Table 5-1 for the recommended output capacitor range). An output capacitance higher than 10 µF adds a better load-step response and high-frequency noise attenuation, especially while stepping from light current loads (PFM mode) to heavy current loads (PWM mode). Overshoots and undershoots during pulse load application are reduced by adding a zero in the compensation loop. A small capacitance (for example 100 pF) in parallel with an upper feedback resistor will reduce output spikes, especially in PFM mode.

While the N-Channel switch is on, the output current is supplied by the output capacitor C_{OUT}. The amount of output capacitance and equivalent series resistance will have a significant effect on the output ripple voltage. While C_{OUT} provides load current, a voltage drop also appears across its internal ESR that results in ripple voltage.

EQUATION 5-2:

$$I_{OUT} = C_{OUT} \times \left(\frac{dV}{dt}\right)$$

Where:

dV = ripple voltage

dt = On time of the N-Channel switch ($D \times 1/F_{SW}$)

Table 5-1 contains the recommended range for the input and output capacitor value.

TABLE 5-1: CAPACITOR VALUE RANGE

	C_{IN}	C_{OUT}
Min.	4.7 µF	10 µF
Max.	—	100 µF

5.5 Inductor Selection

The MCP1640/B/C/D is designed to be used with small surface-mount inductors; the inductance value can range from 2.2 µH to 10 µH. An inductance value of 4.7 µH is recommended to achieve a good balance between inductor size, converter load transient response and minimized noise.

TABLE 5-2: MCP1640/B/C/D RECOMMENDED INDUCTORS

Part Number	Value (µH)	DCR Ω (typ.)	I_{SAT} (A)	Size WxLxH (mm)
Coilcraft				
EPL2014-472	4.7	0.23	1.06	2.0x2.0x1.4
EPL3012-472	4.7	0.165	1.1	3.0x3.0x1.3
MSS4020-472	4.7	0.115	1.5	4.0x4.0x2.0
LPS6225-472	4.7	0.065	3.2	6.0x6.0x2.4
Coiltronics®				
SD3110	4.7	0.285	0.68	3.1x3.1x1.0
SD3112	4.7	0.246	0.80	3.1x3.1x1.2
SD3114	4.7	0.251	1.14	3.1x3.1x1.4
SD3118	4.7	0.162	1.31	3.8x3.8x1.2
SD3812	4.7	0.256	1.13	3.8x3.8x1.2
SD25	4.7	0.0467	1.83	5.0x5.0x2.5
Würth Elektronik®				
WE-TPC Type TH	4.7	0.200	0.8	2.8x2.8x1.35
WE-TPC Type S	4.7	0.105	0.90	3.8x3.8x1.65
WE-TPC Type M	4.7	0.082	1.65	4.8x4.8x1.8
WE-TPC Type X	4.7	0.046	2.00	6.8x6.8x2.3
Sumida Corporation				
CMH23	4.7	0.537	0.70	2.3x2.3x1.0
CMD4D06	4.7	0.216	0.75	3.5x4.3x0.8
CDRH4D	4.7	0.09	0.800	4.6x4.6x1.5
TDK-EPCOS				
B82462A2472M000	4.7	0.084	2.00	6.0x6.0x2.5
B82462G4472M	4.7	0.04	1.8	6.3x6.3x3.0

Several parameters are used to select the correct inductor: maximum rated current, saturation current and copper resistance (ESR). For boost converters, the inductor current is much higher than the output current; the average of the inductor current is equal to the input current drawn from the input. The lower the inductor ESR, the higher the efficiency of the converter. This is a common trade-off in size versus efficiency.

Peak current is the maximum or the limit, and saturation current typically specifies a point at which the inductance has rolled off a percentage of the rated value. This can range from a 20% to 40% reduction in inductance. As inductance rolls off, the inductor ripple current increases; as does the peak switch current. It is important to keep the inductance from rolling off too much, causing switch current to reach the peak limit.

5.6 Thermal Calculations

The MCP1640/B/C/D is available in two different packages: 6-Lead SOT-23 and 8-Lead 2 x 3 DFN. The junction temperature is estimated by calculating the power dissipation and applying the package thermal resistance (θ_{JA}). The maximum continuous junction temperature rating for the MCP1640/B/C/D is +125°C.

To quickly estimate the internal power dissipation for the switching boost regulator, an empirical calculation using measured efficiency can be used. Given the measured efficiency, the internal power dissipation is estimated by Equation 5-3.

EQUATION 5-3:

$$\left(\frac{V_{OUT} \times I_{OUT}}{Efficiency}\right) - (V_{OUT} \times I_{OUT}) = P_{Dis}$$

The difference between the first term – input power, and the second term – power delivered, is the internal MCP1640/B/C/D power dissipation. This is an estimate, assuming that most of the power lost is internal to the MCP1640/B/C/D and not C_{IN}, C_{OUT} and the inductor. There is some percentage of power lost in the boost inductor, with very little loss in the input and output capacitors. For a more accurate estimation of internal power dissipation, subtract the $I_{INRMS}^2 \times L_{ESR}$ power dissipation.

5.7 PCB Layout Information

Good printed circuit board layout techniques are important to any switching circuitry, and switching power supplies are no different. When wiring the switching high-current paths, short and wide traces should be used. Therefore, it is important that the input and output capacitors be placed as close as possible to the MCP1640/B/C/D to minimize the loop area.

The feedback resistors and feedback signal should be routed away from the switching node and the switching current loop. When possible, ground planes and traces should be used to help shield the feedback signal and minimize noise and magnetic interference.

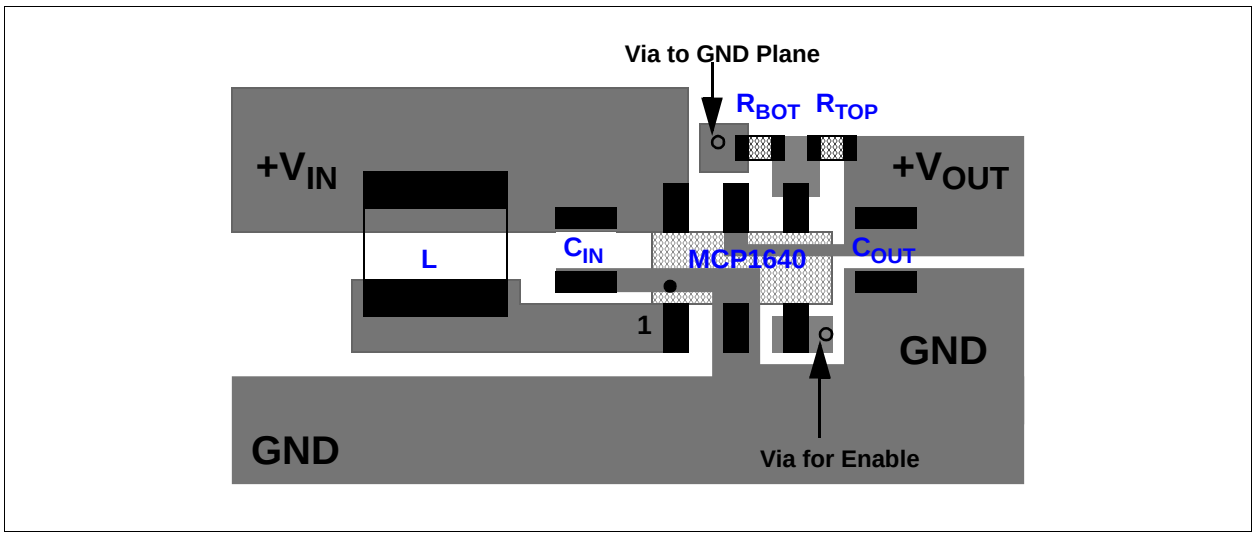


FIGURE 5-1: *MCP1640/B/C/D SOT-23-6 Recommended Layout.*

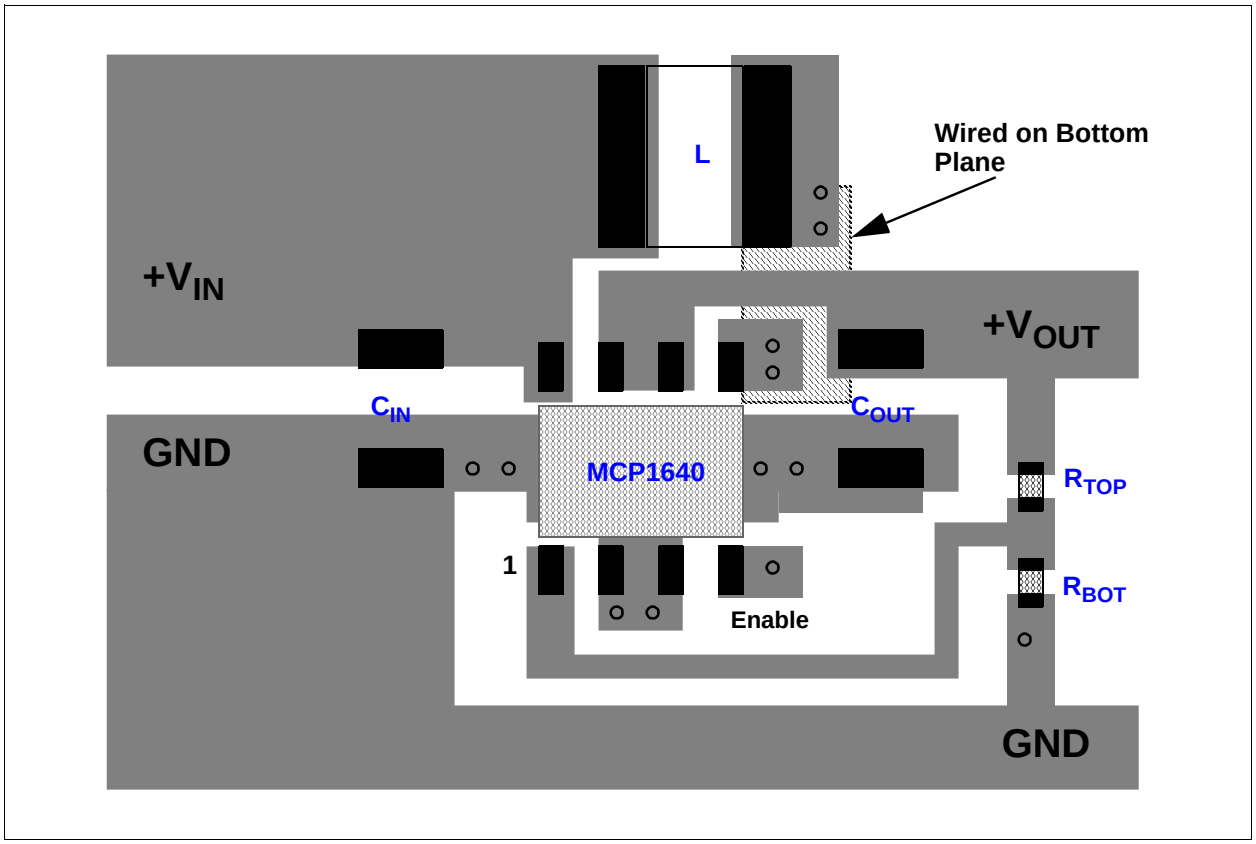
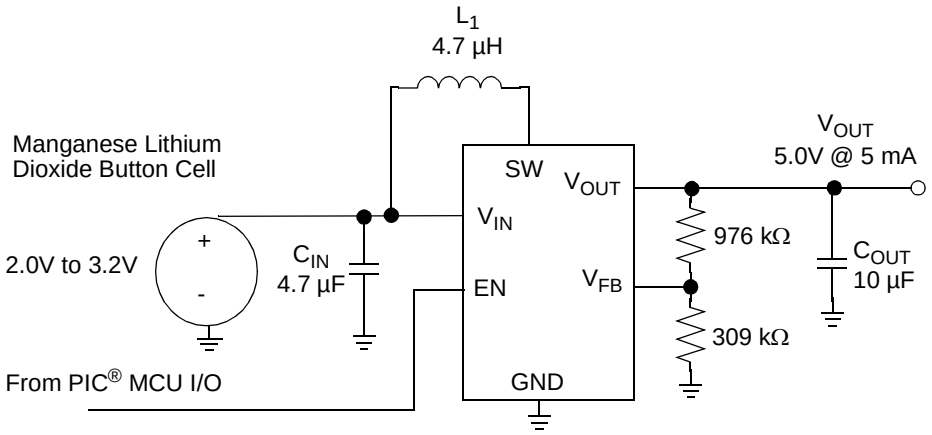


FIGURE 5-2: *MCP1640/B/C/D DFN-8 Recommended Layout.*

6.0 TYPICAL APPLICATION CIRCUITS



Note: For applications that can operate directly from the battery input voltage during Sleep mode and require a higher voltage during Normal Run mode, the MCP1640C device provides Input to Output Bypass when disabled. The PIC® microcontroller is powered by the output of the MCP1640C. One of its I/O pins is used to enable and disable the MCP1640C. While operating in Sleep mode, the MCP1640C input quiescent current is typically less than 1 µA.

FIGURE 6-1: *Manganese Lithium Coin Cell Application Using Bypass Mode.*

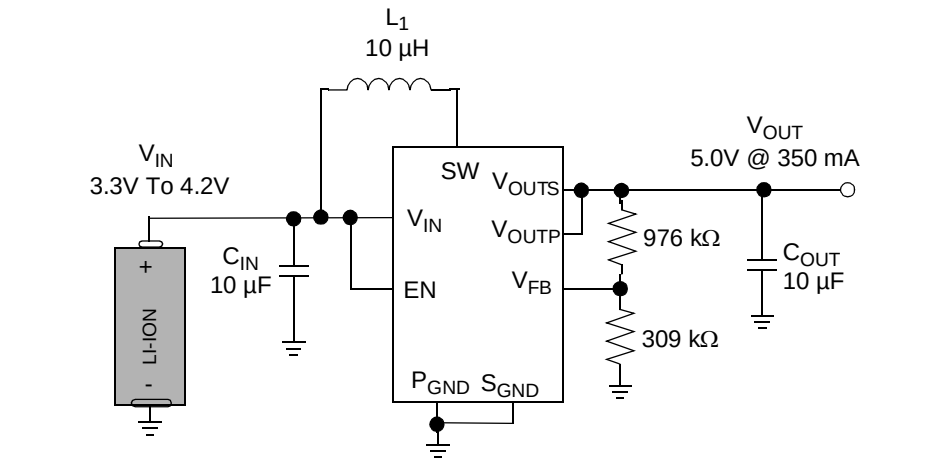


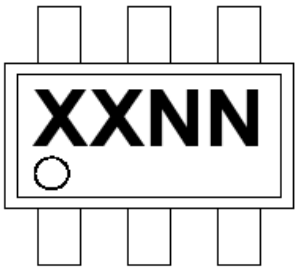
FIGURE 6-2: *USB On-The-Go Powered by Li-Ion.*

NOTES:

7.0 PACKAGING INFORMATION

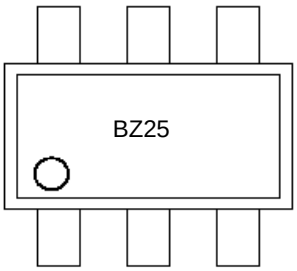
7.1 Package Marking Information

6-Lead SOT-23



Part Number	Code
MCP1640T-I/CHY	BZNN
MCP1640BT-I/CHY	BWNN
MCP1640CT-I/CHY	BXNN
MCP1640DT-I/CHY	BYNN

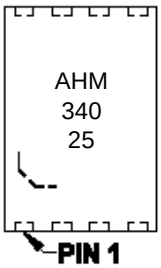
Example



8-Lead DFN

Part Number	Code
MCP1640-I/MC	AHM
MCP1640T-I/MC	AHM
MCP1640B-I/MC	AHP
MCP1640BT-I/MC	AHP
MCP1640C-I/MC	AHQ
MCP1640CT-I/MC	AHQ
MCP1640D-I/MC	AHR
MCP1640DT-I/MC	AHR

Example

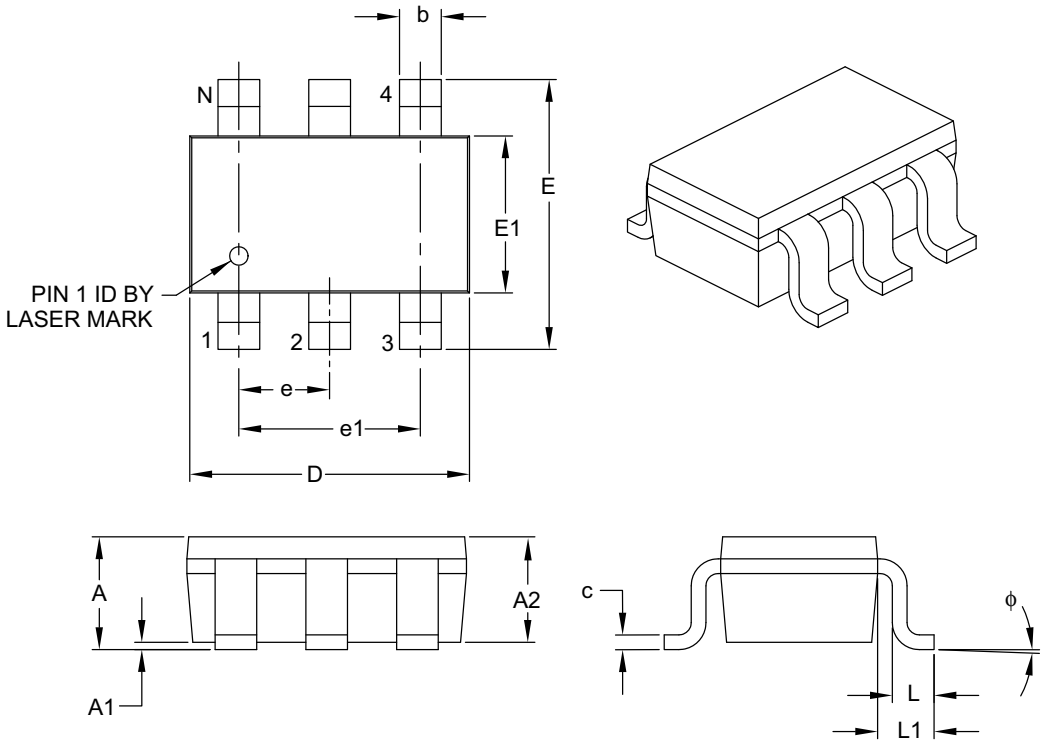


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

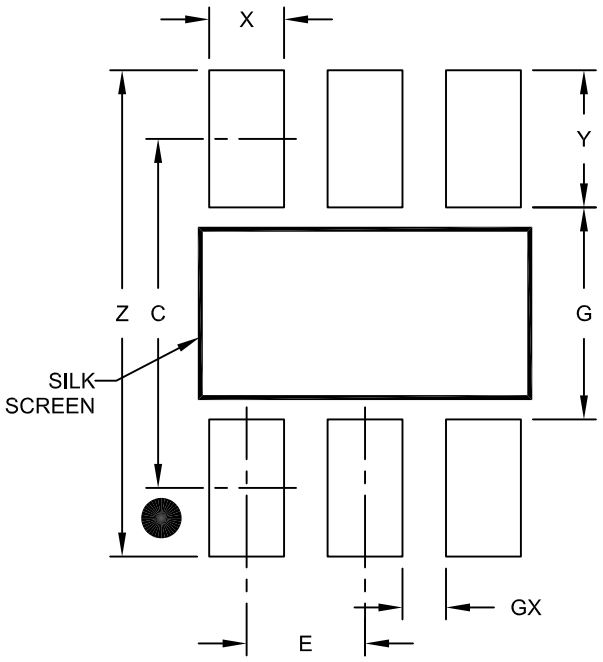
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

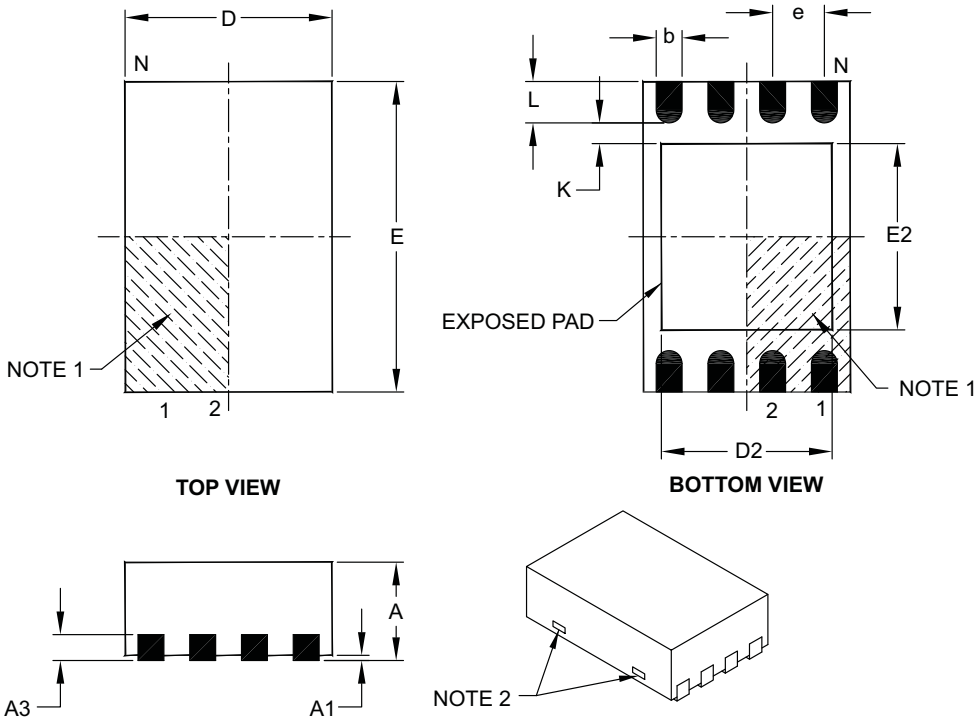
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

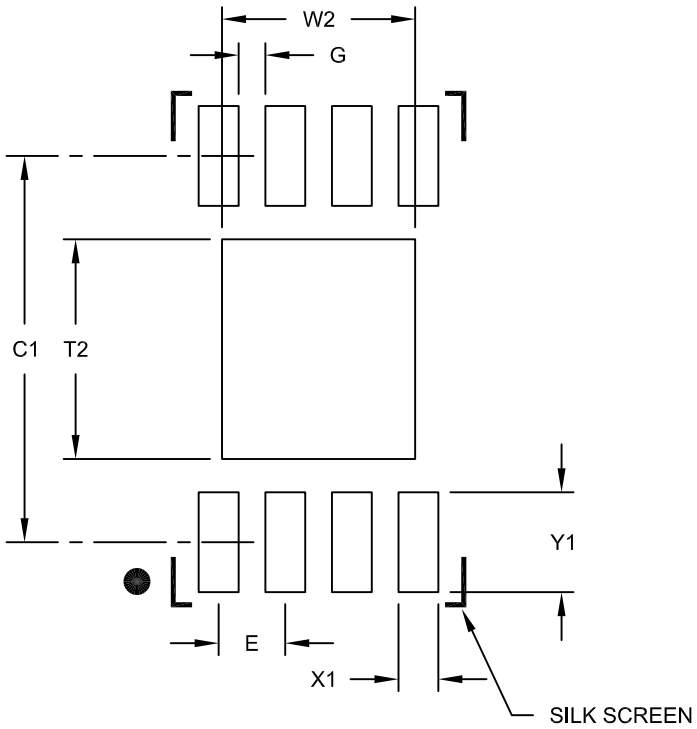
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B

NOTES:

APPENDIX A: REVISION HISTORY

Revision D (September 2015)

The following is the list of modifications:

1. Deleted maximum values for NMOS Switch Leakage and PMOS Switch Leakage parameters in DC Characteristics table.
2. Updated Figure 2-15 in **Section 2.0 "Typical Performance Curves"**.
3. Minor typographical corrections.

Revision C (November 2014)

The following is the list of modifications:

1. Updated Features list.
2. Updated values in the DC Characteristics and Temperature Specifications tables.
3. Updated Figures 2-6 and 2-15.
4. Updated **Section 4.2.1 "Low-Voltage Start-Up"**.
5. Updated **Section 5.2 "Adjustable Output Voltage Calculations and Maximum Output Current"**.
6. Updated **Section 5.4 "Output Capacitor Selection"**.
7. Updated markings and SOT-23 package specification drawings for CHY designator in **Section 7.0 "Packaging Information"**.
8. Minor editorial corrections.

Revision B (March 2011)

The following is the list of modifications:

1. Updated Table 5-2.
2. Added the package markings tables in **Section 7.0 "Packaging Information"**.

Revision A (February 2010)

Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel	Temperature Range	Package

Device	MCP1640:	0.65V, PWM/PFM True Disconnect, Sync Boost Regulator
	MCP1640B:	0.65V, PWM Only True Disconnect, Sync Boost Regulator
	MCP1640C:	0.65V, PWM/PFM Input to Output Bypass, Sync Boost Regulator
	MCP1640D:	0.65V, PWM Only Input to Output Bypass, Sync Boost Regulator
Tape and Reel Option	T	= Tape and Reel (1)
	blank	= DFN only
Temperature Range	I	= -40°C to +85°C (Industrial)
Package	CHY*	=Plastic Small Outline Transistor (SOT-23), 6-lead
	MC	=Plastic Dual Flat, No Lead (2x3 DFN), 8-lead
	*Y = Nickel palladium gold manufacturing designator.	

Examples:

a) MCP1640-I/MC: 0.65V, PWM/PFM True Disconnect Sync Reg., 8LD-DFN pkg.

b) MCP1640T-I/MC: 0.65V, PWM/PFM True Disconnect Sync Reg., 8LD-DFN pkg. Tape and Reel

c) MCP1640B-I/MC: 0.65V, PWM-Only True Disconnect Sync Reg., 8LD-DFN pkg.

d) MCP1640BT-I/MC: 0.65V, PWM-Only True Disconnect Sync Reg., 8LD-DFN pkg. Tape and Reel

e) MCP1640C-I/MC: 0.65V, PWM/PFM Input-to-Output Bypass Sync Reg., 8LD-DFN pkg.

f) MCP1640CT-I/MC: 0.65V, PWM/PFM Input-to-Output Bypass Sync Reg., 8LD-DFN pkg. Tape and Reel

g) MCP1640D-I/MC: 0.65V, PWM-Only Input-to-Output Bypass Sync Reg., 8LD-DFN pkg.

h) MCP1640DT-I/MC: 0.65V, PWM-Only Input-to-Output Bypass Sync Reg., 8LD-DFN pkg. Tape and Reel

i) MCP1640T-I/CHY: 0.65V, PWM/PFM True Disconnect Sync Reg., 6LD SOT-23 pkg. Tape and Reel

j) MCP1640BT-I/CHY: 0.65V, PWM-Only True Disconnect Sync Reg., 6LD SOT-23 pkg. Tape and Reel

k) MCP1640CT-I/CHY: 0.65V, PWM/PFM Input-to-Output Bypass Sync Reg., 6LD SOT-23 pkg. Tape and Reel

l) MCP1640DT-I/CHY: 0.65V, PWM-Only Input-to-Output Bypass Sync Reg., 6LD SOT-23 pkg. Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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