3 Features and benefits

- Three switching regulators: 2 synchronous and 1 nonsynchronous
- One low dropout linear regulator
- Output current capability:
  - 1.5 A continuous on channel 1
  - 1.25 A continuous on channels 2 and 3
  - 400 mA continuous on channel 4
  - Internal power MOSFETs on all channels
- Voltage feed-forward on channel 1
- ±1.5 % output voltage accuracy on all channels
- Cycle-by-cycle current limit and short-circuit protection
- Fixed 800 kHz switching frequency
- Internal soft-start
- Overvoltage, undervoltage and overtemperature protection
- Open-drain power-good output signal
- Separate active-high enable input for each channel
- Pb-free packaging designated by suffix code EP

4 Applications

- Set-top boxes and receivers
- Cable modems
- Networking cards
- Telecom line cards

5 Orderable parts

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package
MC34700EP/R2	–40 °C to 85 °C	32 QFN

6 Pinning information

6.1 Pinning

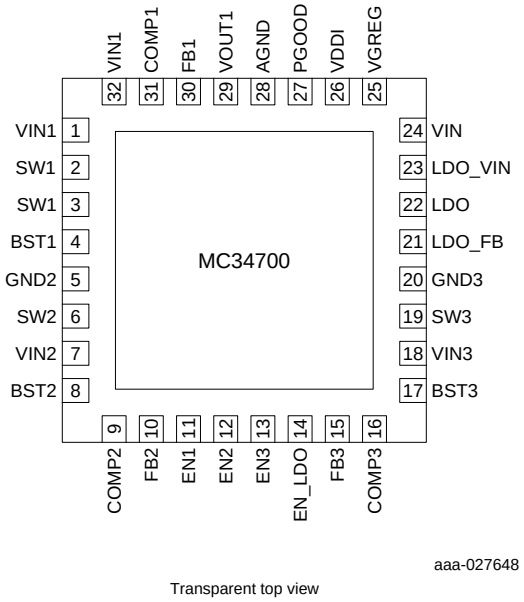

Figure 2. MC34700 pin connections

6.2 Pin definitions

Pin	Symbol	Description
1,32	VIN1	Buck regulator #1's power input voltage. VIN1 is connected to the drain of the DC/DC #1's high-side MOSFET. Local bypass capacitors are recommended.
2,3	SW1	Buck regulator #1's switching node. SW1 is connected to the source of the high-side MOSFET. Connect this pin to the cathode of the catch diode and the output inductor.
4	BST1	Buck regulator #1's bootstrap capacitor input. Connect a capacitor between the BST1 and SW1 pin of DC/DC #1 to enhance the gate of the high-side MOSFET during switching.
5	GND2	Buck regulator #2's power ground. GND2 is connected to the source of DC/DC #2's low-side MOSFET. Connect this pin to the DC/DC #2's power return path.
6	SW2	Buck regulator #2's switching node. SW2 is connected to source of the high-side and the drain of the low-side MOSFET. Connect this pin to the output inductor.
7	VIN2	Buck regulator #2's power input voltage. VIN2 is connected to the drain of the DC/DC #2's high-side MOSFET. Local bypass capacitors are recommended.
8	BST2	Buck regulator #2's bootstrap capacitor input. Connect a capacitor between the BST2 and SW2 pin of DC/DC #2 to enhance the gate of the high-side MOSFET during switching.

Pin	Symbol	Description
9	COMP2	Buck regulator #2's compensation output. COMP2 is connected to DC/DC #2's error amplifier's output. Connect the required external compensation network between the COMP2 pin and the FB2 pin.
10	FB2	DC/DC#2's error amplifier inverting input. Connect the required compensation network and feedback network to this terminal as appropriate.
11	EN1	This input enables buck regulator #1. Asserting EN1 high turns on DC/DC #1. The internal control logic remains active as long as VIN is present.
12	EN2	This input enables buck regulator #2. Asserting EN2 high turns on DC/DC #2. The internal control logic remains active as long as VIN is present.
13	EN3	This input enables buck regulator #3. Asserting EN3 high turns on DC/DC #3. The internal control logic remains active as long as VIN is present.
14	EN_LDO	This input enables the LDO. Asserting EN_LDO high turns on the LDO. The internal control logic remains active as long as VIN is present.
15	FB3	DC/DC#3's error amplifier inverting input. Connect the required compensation network and feedback network to this terminal as appropriate.
16	COMP3	Buck regulator #3's compensation output. COMP3 is connected to DC/DC #3's error amplifier's output. Connect the required external compensation network between the COMP3 pin and the FB3 pin.
17	BST3	Buck regulator #3's bootstrap capacitor input. Connect a capacitor between the BST3 and SW3 pin of DC/DC #3 to enhance the gate of the high-side MOSFET during switching.
18	VIN3	Buck regulator #3's power input voltage. VIN3 is connected to the drain of the DC/DC #3's high-side MOSFET. Local bypass capacitors are recommended.
19	SW3	Buck regulator #3's switching node. SW3 is connected to source of the high side and the drain of the low-side MOSFET. Connect this pin to the output inductor.
20	GND3	Buck regulator #3's power ground. GND3 is connected to the source of DC/DC #3's low side MOSFET. Connect this pin to the DC/DC #3's power return path.
21	LDO_FB	LDO error amplifier inverting input. Connect the appropriate output voltage feedback resistor divider to this pin.
22	LDO	LDO regulator output. Connect this pin to the feedback resistor divider and output capacitor.
23	LDO_VIN	LDO's power input voltage. LDO_VIN is connected to the drain of the linear regulator's pass device. Local bypass capacitors are recommended.
24	VIN	IC supply voltage input. This pin should be decoupled from the buck regulator's power input voltages (VIN1, VIN2, VIN3). Filtering is required for proper device operation.

Pin	Symbol	Description
25	VGREG	This is the output of an internal linear regulator which is used to supply the gate drivers. The VGREG linear regulator is driven from the input supply voltage VIN, and it's output is also used to drive the gates of the low side MOSFETs of regulators DC/DC #2 and DC/DC #3, as well as the LDO. Connect this pin to a low ESR, 1.0 µF bypass capacitor.
26	VDDI	Internal regulator output used to supply the internal logic and analog blocks. VDDI is driven from the gate drive supply voltage, VGREG. Connect this pin to a 1.0 µF, low ESR decoupling filter capacitor.
27	PGOOD	Status signal used to indicate that all the regulators' output voltages are good. Upon a fault occurrence, this output signal goes low. PGOOD is an open drain output, and must be pulled up by an external resistor to a supply voltage suitable for I/O.
28	AGND	Analog ground of the IC. Internal analog and logic signals are referenced to this pin.
29	VOUT1	DC/DC#1's shunt input. VOUT1 is connected to a discharge MOSFET. This MOSFET is used to discharge the output of DC/DC1 when there is a fault condition, such as thermal shutdown or a short circuit. It is also used to provide a preload to maintain a minimum duty. Connect this pin to the output of DC/DC #1.
30	FB1	DC/DC#1's error amplifier inverting input. Connect the required compensation network and feedback network to this terminal as appropriate.
31	COMP1	Buck regulator #1's compensation output. COMP1 is connected to DC/DC #1's error amplifier's output. Connect the required external compensation network between the COMP1 pin and the FB1 pin.
33	AGND	Thermal pad for heat transfer. Connect the thermal pad to the analog ground.

7 Simplified internal block diagram

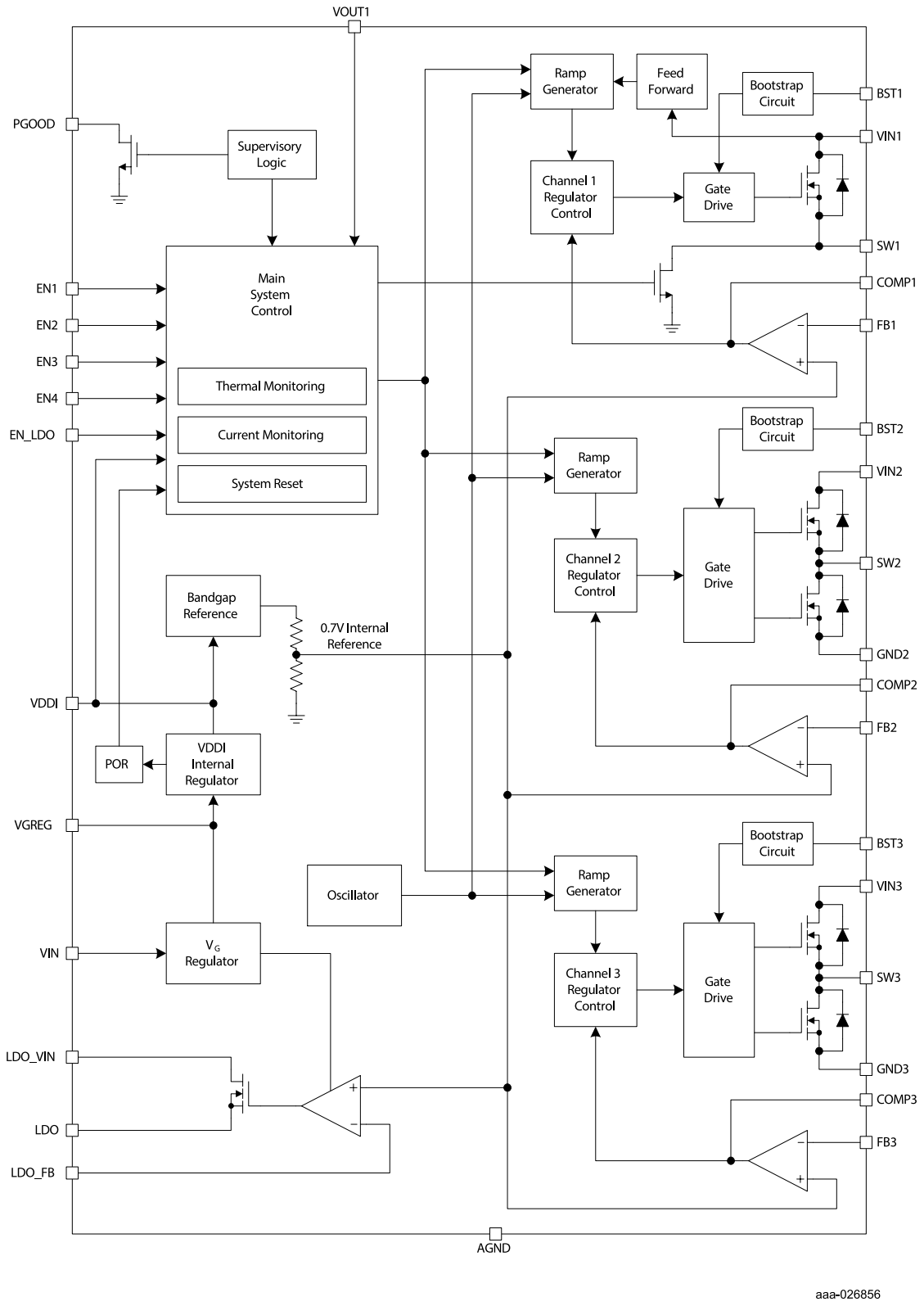

Figure 3. Internal block diagram

8 General product characteristics

8.1 Absolute maximum ratings

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device. This is a stress only rating and operation at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Ratings	Symbol	Value	Unit
Electrical ratings			
Input voltages • Input voltage • Input DC/DC1 voltage, I_{VIN} = 0 • Input DC/DC2, 3, and LDO voltage	 V_{IN} V_{IN1} V_{IN2}, V_{IN3}, V_{INLDO}	 –0.3 to 20 –0.3 to 20 –0.3 to 7	V
Switch node voltages • Switch node DC/DC1 • Switch node DC/DC2, DC/DC3	 V_{SW1} V_{SW2}, V_{SW3}	 –0.3 to 20 –0.3 to 7	V
Bootstrap voltages • Bootstrap DC/DC1 • Bootstrap DC/DC2, DC/DC3 • Bootstrap voltage referenced to switch node voltage	 V_{BST1} V_{BST2}, V_{BST3} $V_{BST} – V_{SW}$	 –0.3 to 25 –0.3 to 14 –0.3 to 7	V
Compensation (COMP1, 2, and 3), feedback (FB1, FB2, FB3, LDO_FB), V_{DDI}	—	–0.3 to 3	V
All other pins (EN1, 2, 3, EN_LDO, PGOOD, VGREG, LDO, VOUT1)	—	–0.3 to 7	V
ESD voltage [1] • Human body model (HBM) all pins	V_{ESD}	 ±2000	V
Thermal ratings			
Operating temperature • Ambient • Junction	 T_A T_J	 –40 to +85 –40 to +125	°C
Peak package temperature during reflow [2], [3]	T_{PPRT}	300	°C
Storage temperature	T_{STRG}	–40 to +150	°C
Thermal resistance			
Thermal resistance [2] • Junction-to-case • Junction-to-ambient	 $T_{ΘJC}$ $T_{ΘJA}$	 6.7 37	°C/W
Power dissipation • T_A = 25 °C • T_A = 70 °C • T_A = 85 °C	P_D	 2.5 1.3 1.0	W

Ratings	Symbol	Value	Unit

Notes:

1. *ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).*
2. *Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.*
3. *NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to nxp.com, search by part number. Remove prefixes/ suffixes and enter the core ID to view all orderable parts (for MC33xxxD enter 33xxx), and review parametrics.*

8.2 Static and dynamic electrical characteristics

Table 3. Electrical characteristics

Characteristics noted under conditions 9.0 V ≤ V_{IN} ≤ 18 V, –40 °C ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply						
V_{IN}	VIN voltage	Maximum Minimum	— —	18 9.0	— —	V
I_{SDB}	Standby current	V_{EN1} = V_{EN2} = V_{EN3} = V_{EN_LDO} = 0 V	—	8.95	15	mA
I_{IN}	Operating current	V_{EN1} = V_{EN2} = V_{EN3} = V_{EN_LDO} = 5.0 V V_{VIN} = 9.0 V, Load = 0 A	—	15.4	—	mA
V_{DDI}	Internal supply voltage	—	2.3	2.5	2.7	V
Power-on reset						
V_{VGREG_RISING}	VGREG rising threshold voltage	—	3.5	4.0	4.5	V
$V_{VGREG\_FALLING}$	VGREG falling threshold voltage	—	3.0	3.4	4.0	V
V_{VGREG_HYS}	VGREG hysteresis voltage	—	0.2	0.55	1.0	V
VGREG linear regulator						
$R_{VGREGIN}$	On resistance	I_{VGREG} = 80 mA	—	30	—	Ω
V_{VGREG}	Output voltage	—	4.75	5.25	5.5	V
$V_{IN\_dV/dT}$	Maximum input dV/dT	VIN1= VIN	—	10	—	V/µs
Bias voltages						
C_{VGREG}	VGREG decoupling	VGREG= 5.0 V	—	1.0	—	µF
C_{VDDI}	VDDI decoupling	VDDI= 2.5 V	—	1.0	—	µF
Enable						
$V_{EN1,2,3}$ V_{EN_LDO}	Output enable logic high threshold voltage	—	0.78	—	—	V
$V_{EN1,2,3}$ V_{EN_LDO}	Output enable logic low threshold voltage	—	—	—	0.61	V
R_{EN_IN}	EN input resistance to ground	—	—	1.5	—	MΩ
t_{DELAY1}	Delay from enable to soft start DC1	—	—	1.0	—	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DELAY2,3}$	Delay from enable to soft start DC2, DC3	—	—	160	—	ms
Reference						
$V_{REF1,2,3}$	DC/DC1, 2, 3 reference voltage	—	0.690	0.700	0.710	V
V_{REF_LDO}	LDO reference voltage	—	0.690	0.700	0.710	V
Oscillator						
f_{SW}	Switching frequency	—	760	800	840	kHz
Soft-start						
$t_{SS\_BUCKREG}$	Soft-start duration DC1, 2, 3	—	2.5	3.5	4.5	ms
t_{SS_LDO}	Soft-start duration LDO	—	0.3	0.5	0.7	ms
Ramp generators						
V_{RAMP_AMP1}	Ramp amplitude (DC/DC1)	V_{FF_GAIN1} x P_{VIN1},P_{VIN1} = 18 V	—	1.0	—	V_{P-P}
V_{FF_GAIN1}	VFF gain (DC/DC1)	—	—	0.055	—	V/V
$V_{RAMP\_AMP2,3}$	Ramp amplitude (DC/DC2,3)	V_{FF_GAIN2} x P_{VIN2},P_{VIN2} = 6.0 V	—	1.25	—	V_{P-P}
$V_{FF\_GAIN2,3}$	VFF gain (DC/DC2,3)	—	—	0.208	—	V/V
V_{RAMP_OFFSET}	Ramp bottom (DC/DC1,2,3)	—	—	0.2	—	V
D_1	Min duty cycle (DC/DC1)	I_{LOAD1} = 0 A	—	—	16	%
D_1	Max duty cycle (DC/DC1)	I_{LOAD1} = 0 A	68.4	—	—	%
$D_{2,3}$	Min duty cycle (DC/DC2,3)	I_{LOAD1} = 0 A	—	0	0	%
$D_{2,3}$	Max duty cycle (DC/DC2,3)	I_{LOAD1} = 0 A	83.6	—	—	%
Power-good						
Δ_{OV_TH}	OV threshold, all regulators	Percentage of set point	—	—	108	%
Δ_{UV_TH}	UV threshold,all regulators	Percentage of set point	92	—	—	%
V_{OL_PGOOD}	PGOOD output low level	I_{SINK} = 6.0 mA	—	0.4	—	V
$t_{PG-RESET}$	PGOOD reset delay	—	—	100	—	µs
$t_{PG-FILTER}$	PGOOD glitch rejection	—	—	10	—	µs
Buck converter 1						
V_{IN1_MAX}	Maximum VIN1 input voltage	—	—	18	—	V
V_{IN1_MIN}	Minimum VIN1 input voltage	—	—	9.0	—	V
$V_{DC1VOUTMAX}$	Maximum output voltage	V_{IN} = 9.0 V	—	5.25	—	V
$V_{DC1VOUTMIN}$	Minimum output voltage	V_{IN} = 9.0 V	—	2.0	—	V
$I_{OUTDC1MAX}$	Maximum output current	—	—	1.5	—	A
Δ_{VOUT1}	Total system accuracy	—	–1.5	—	1.5	%
I_{SHORT1}	Peak short-circuit current limit	—	2.5	—	4.5	A
$R_{DS(ON)\_HS}$	High side on resistance	—	—	150	—	mΩ
R_{DO}	Equivalent dropout resistance	V_{IN1} = 5.5 V, V_{OUT} = 3.3 V, I_{LOAD} = 2.0 A	—	183	—	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
A_{EA}	Error amplifier DC gain	—	—	110	—	dB
GBW	Error amplifier unity-gain bandwidth	—	—	4.0	—	MHz
SR	Error amplifier slew rate @ 15 pF	—	—	1.8	—	V/µs
t_{LIM1}	Current limit timer	—	—	10	—	ms
$t_{TIMEOUT1}$	Current limit retry timeout period	—	—	100	—	ms
Buck converter 2						
V_{IN2_MAX}	Maximum VIN2 input voltage	—	—	6.0	—	V
V_{IN2_MIN}	Minimum VIN2 input voltage	—	—	1.5	—	V
$V_{DC2VOUTMAX}$	Maximum output voltage	V_{IN} =9.0 V	—	3.6	—	V
$V_{DC2VOUTMIN}$	Minimum output voltage	V_{IN} = 9.0 V	—	0.7	—	V
$IOUT_{DC2MAX}$	Maximum output current	—	—	1.25	—	A
ΔV_{OUT2}	Total system accuracy	—	–1.5	—	1.5	%
I_{SHORT2}	Peak short-circuit current limit	—	2.0	—	4.5	A
$R_{DS(ON)\_HS}$	High-side on resistance	—	—	175	—	mΩ
$R_{DS(ON)\_LS}$	Low-side on resistance	—	—	150	—	mΩ
R_{DO}	Equivalent dropout resistance	V_{IN2} = 1.7 V, V_{OUT} = 1.25 V, I_{LOAD} = 1.25 A	—	150	—	mΩ
I_{SW2}	SW2 leakage current	V_{IN} = 12 V, V_{IN2} = 0 V,EN2 = 0 V	—	400	—	µA
A_{EA}	Error amplifier DC gain	—	—	110	—	dB
GBW	Error amplifier unity gain bandwidth	—	—	4.0	—	MHz
SR	Error amplifier slew rate	—	—	1.8	—	V/µs
t_{LIM2}	Current limit timer	—	—	10	—	ms
$t_{TIMEOUT2}$	Current limit retry timeout period	—	—	100	—	ms
Buck converter 3						
V_{IN3_MAX}	Maximum VIN3 input voltage	—	—	6.0	—	V
V_{IN3_MIN}	Minimum VIN3 input voltage	—	—	1.5	—	V
$V_{DC3VOUTMAX}$	Maximum output voltage	—	—	3.6	—	V
$V_{DC2VOUTMIN}$	Minimum output voltage	—	—	0.7	—	V
$IOUT_{DC3MAX}$	Maximum output current	—	—	1.25	—	A
ΔV_{OUT3}	Total system accuracy	—	–1.5	—	1.5	%
I_{SHORT3}	Peak short-circuit current limit	—	2.0	—	4.5	A
$R_{DS(ON)\_HS}$	High-side on resistance	—	—	160	—	mΩ
$R_{DS(ON)\_LS}$	Low-side on resistance	—	—	140	—	mΩ
R_{DO}	Equivalent dropout resistance	V_{IN2} = 1.7 V, V_{OUT} = 1.25 V, I_{LOAD} = 1.25 A	—	150	—	mΩ
I_{SW3}	SW3 leakage current	V_{IN} = 12 V, V_{IN3}= 0 V,E_{N3} = 0 V	—	400	—	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
A_{EA}	Error amplifier DC gain	—	—	110	—	dB
GBW	Error amplifier unity gain bandwidth	—	—	4.0	—	MHz
SR	Error amplifier slew rate	—	—	1.8	—	V/µs
t_{LIM3}	Current limit timer	—	—	10	—	ms
$t_{TIMEOUT3}$	Current limit retry timeout period	—	—	100	—	ms
Linear regulator						
V_{INLDO}	Maximum LDO input voltage	—	—	6.0	—	V
V_{INLDO}	Minimum LDO input voltage	—	—	1.5	—	V
V_{LDO}	Maximum LDO output voltage	—	—	3.6	—	V
V_{LDO}	Minimum LDO output voltage	—	—	0.7	—	V
I_{LDO}	Maximum LDO output current	—	—	400	—	mA
ΔV_{LDO}	Total system accuracy	—	–1.5	—	1.5	%
V_{DROP}	Maximum dropout voltage	I_{LDO} = 400 mA	—	250	—	mV
P_{DISS_LDO}	LDO power dissipation	—	—	375	—	mW
I_{SHORT_LDO}	Maximum output current	—	—	1100	—	mA
I_{SHORT_LDO}	Minimum output current	—	—	500	—	mA
C_{LDO} C_{ESR}	Required output decoupling	—	— —	10 20	— —	µF mΩ
$t_{TIMEOUT\_LDO}$	Current limit retry timeout period	—	—	100	—	ms
Thermal shutdown						
T_{SD_MAX}	Maximum thermal shutdown threshold	—	—	160	—	°C
T_{SD}	Typical thermal shutdown threshold	—	—	140	—	°C
T_{SD_MIN}	Minimum thermal shutdown threshold	—	—	120	—	°C
T_{SD_HYS}	Thermal shutdown hysteresis	—	—	25	—	°C

9 Electrical performance curves

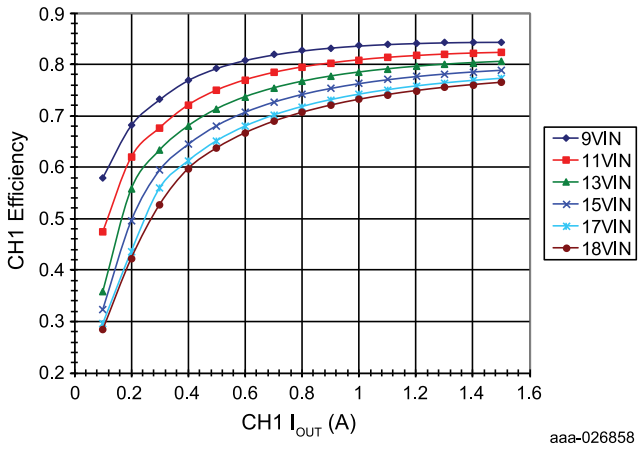

Figure 4. Typical CH1 efficiency (3.36 VOUT)

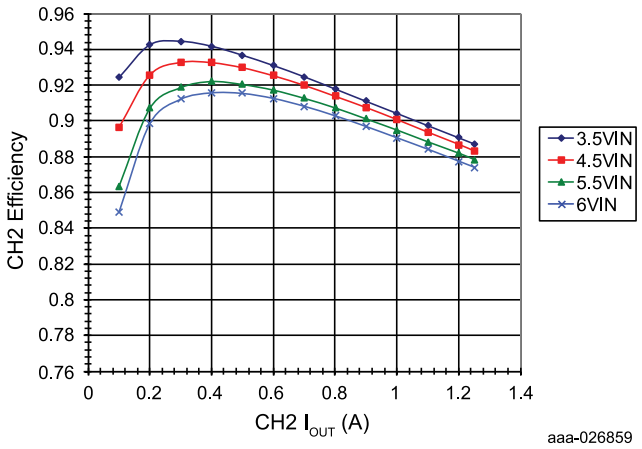

Figure 5. Typical CH2 efficiency (2.49 VOUT)

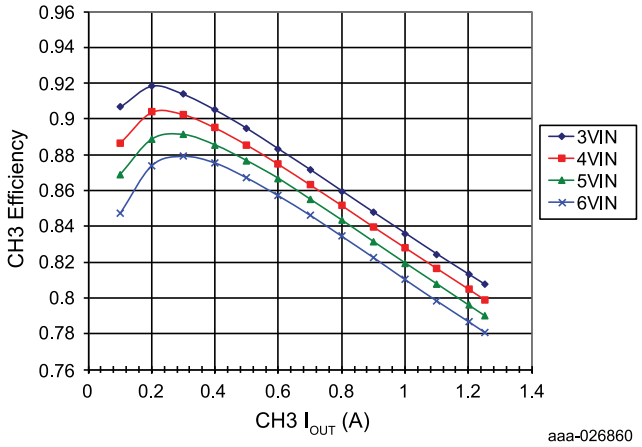

Figure 6. Typical CH3 efficiency (1.28 VOUT)

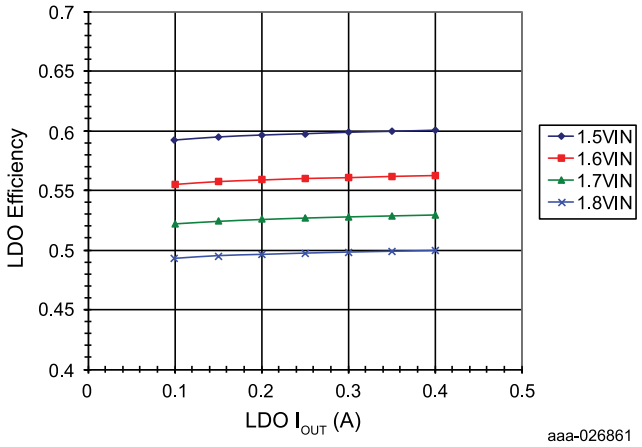

Figure 7. LDO Efficiency (0.89 VOUT)

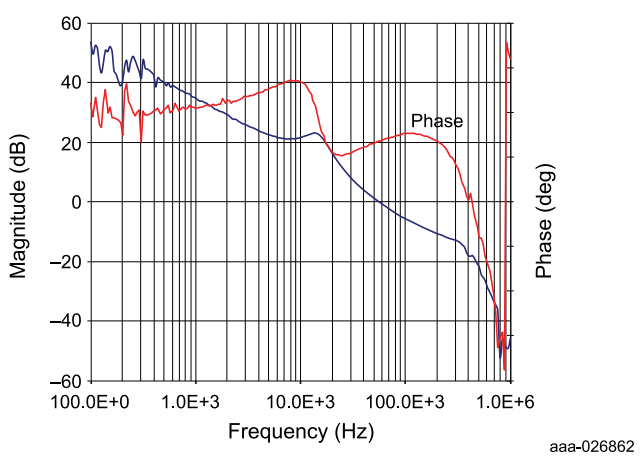

Figure 8. CH1 Loop Response - Application Example

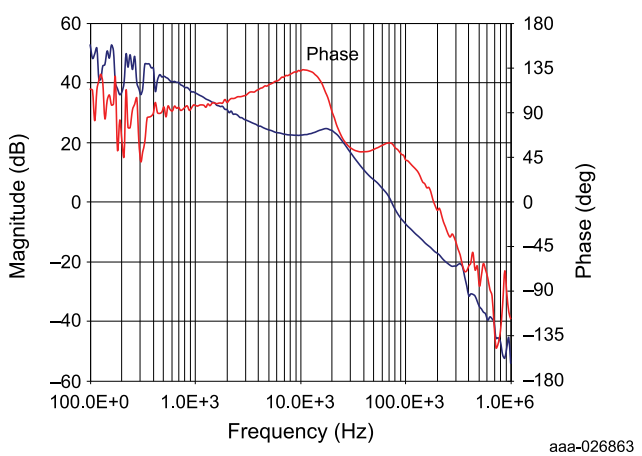

Figure 9. CH2 Loop Response - Application Example

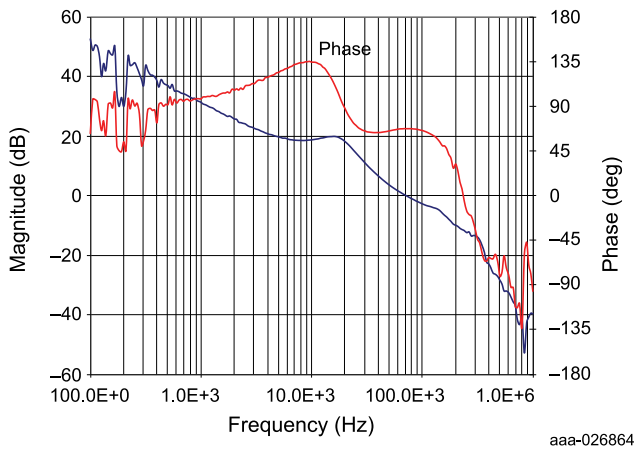

Figure 10. CH3 Loop Response - Application Example

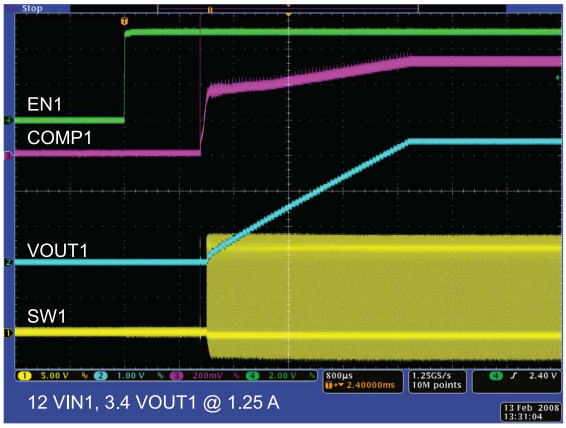

Figure 11. EN CH1 Start-up

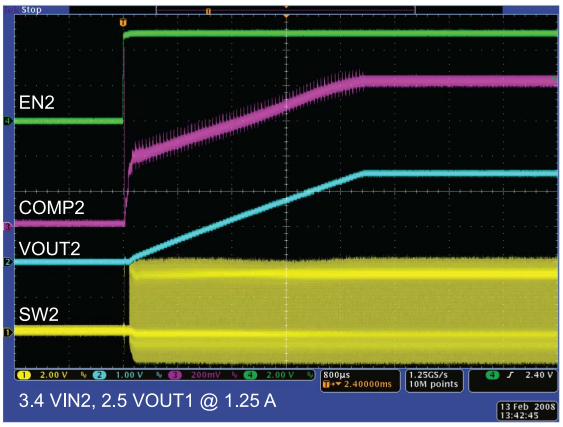

Figure 12. EN CH2 Start-up

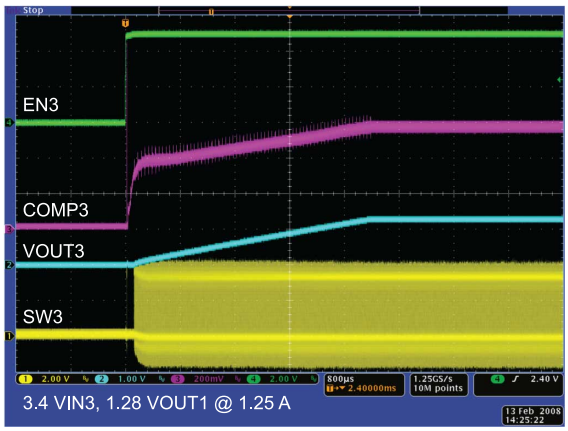

Figure 13. EN CH3 Start-up

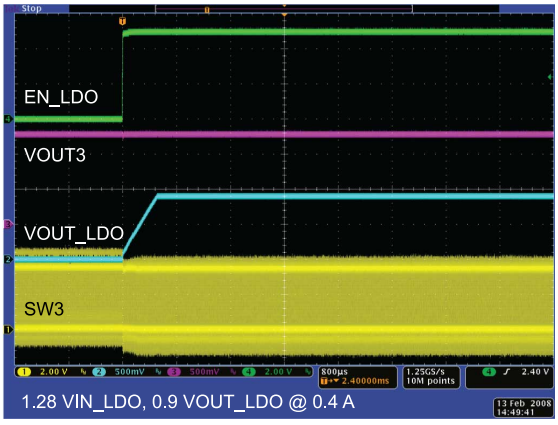

Figure 14. EN LDO Start-up

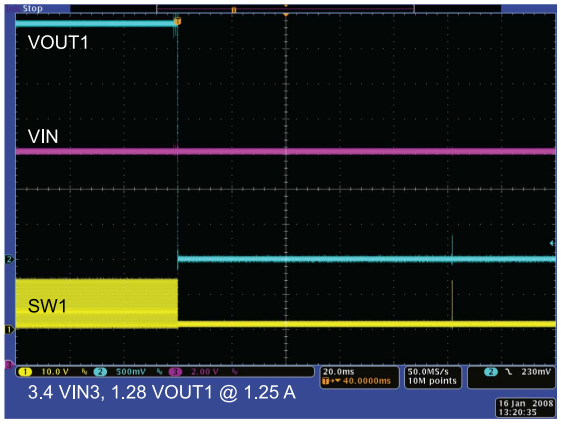

Figure 15. CH1 Short-circuit Response

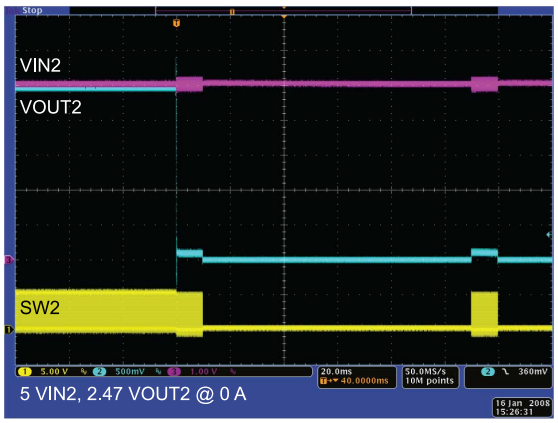

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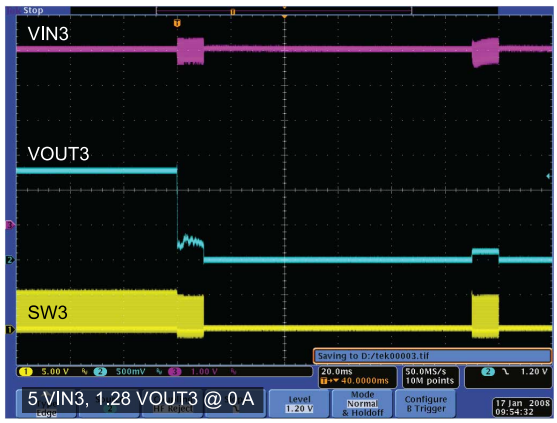
Figure 16. CH2 Short-circuit Response



aaa-026871

Figure 17. CH3 Short-circuit Response

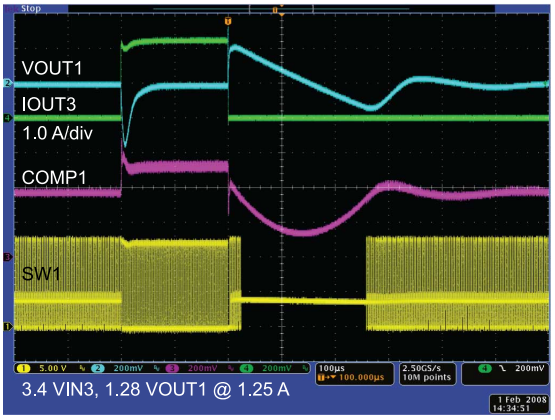


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Figure 18. CH1 Transient Response

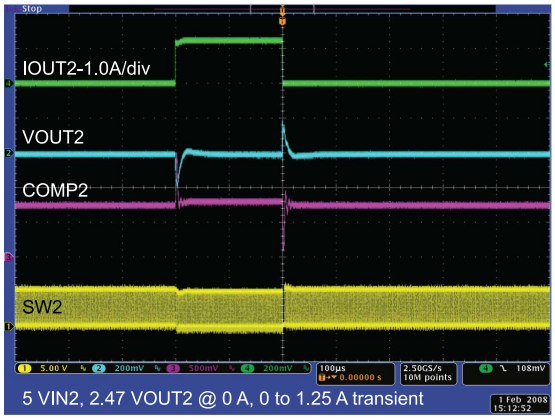

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Figure 19. CH2 Transient Response

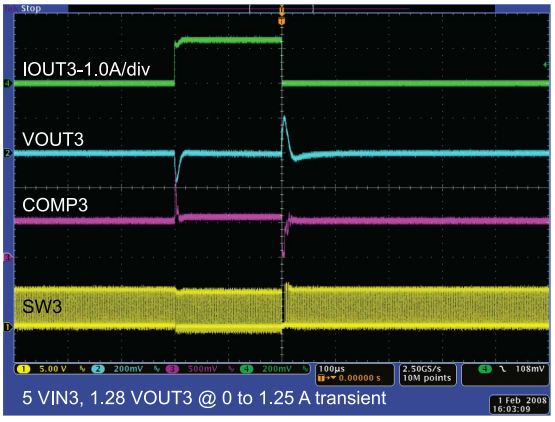

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Figure 20. CH3 Transient Response

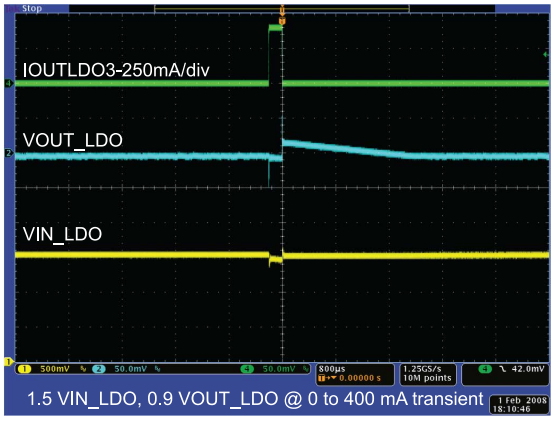

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Figure 21. LDO Transient Response

10 Functional device operation

10.1 Initialization

When power is first applied to the 34700, the internal regulators and bias circuits need to be up and stable before the power on reset (POR) signal is released. The POR waits until the gate drive regulator's voltage, V_{GREG}, has reached about 4.0 V before it allows the rest of the internal blocks to be enabled.

Each regulator has an independent enable pin. This allows the user to program the power up sequence to suit the application. As each regulator is turned on, it will execute a soft start ramp of the output voltage. This is done to prevent the output voltage from overshooting the regulation point. Without a soft start ramp, the output voltage will ramp up faster than the control loop can typically respond, resulting in overshoot. As a result, the soft start periods for the switching regulators are longer (3.5 ms) than for the linear regulator (0.5 ms). The soft start is active each time the regulator is enabled, after a fault retry, or when the IC power is recycled.

After a successful start-up sequence, where all the regulators are enabled, no faults have occurred, and the output voltage is in regulation, the power good signal goes open drain after a 100 µs reset delay. A power good true indicates that all the regulators are functioning in normal operation mode.

10.2 Operational modes

Each regulator of the 34700 has three basic modes of operation.

10.2.1 Normal mode

In normal mode, the regulator is fully operational. To be in this mode, the 34700 input supply, VIN, needs to be present and within its operating range. The regulator's power input voltage also needs to be present and in range. The ENABLE pin for the regulator needs to be asserted, and the output voltage needs to be in regulation. No overcurrent or thermal faults are present in normal mode.

10.2.2 Standby mode

In standby mode, the ENABLE pin for the regulator is held low and the regulator is disabled. VIN needs to be present and within its operating range. The regulator's power input is not needed in this mode, but needs to be present and stable before transitioning to normal mode. No faults are present in standby mode. Note that the standby mode consumes the least amount of power.

10.2.3 Fault mode

In fault mode, the output is no longer in regulation, or an overcurrent or a thermal fault is present. To be in this mode the 34700 input supply, VIN needs to be present and within its operating range. The regulator's power input voltage also needs to be present and in range. However, if the power input is outside the operating range, a regulation fault may occur. The ENABLE pin for the regulator needs to be asserted.

10.2.4 Protection functions

The 34700 monitors the regulators for several fault conditions to protect both the system load and the IC from overstress. The response of the 34700 to a fault condition is described as follows.

10.2.5 Output overvoltage

An overvoltage (OV) condition occurs when the output voltage exceeds the overvoltage threshold, Δ_{OV_TH}. This can occur if the regulator's output is shorted to a supply with a higher output voltage. In this case, the power good signal is pulled low, alerting the host that a fault is present, but the regulator remains active. The regulator will continue to try to regulate the output: DC/DC1 will pulse skip; DC/DC2, 3 will go to minimum duty; and the LDO pass device will go high impedance.

To avoid false trips of the OV monitor, the power good circuit has a 10 µs glitch filter. Once the output voltage falls below the OV threshold and back into regulation, the fault is cleared and the power good signal goes high.

10.2.6 Output undervoltage

An undervoltage (UV) condition occurs when the output voltage falls below the undervoltage threshold, Δ_{UV_TH}. This can occur if the regulator's output is shorted to ground, overloaded, or the power input voltage has decreased. In this case, the power good signal is pulled low, alerting the host that a fault is present, but the regulator remains active. The regulator will continue to try to regulate the output: DC/DC1, 2, 3 will go to maximum duty or current limit; and the LDO pass device will go to a low resistance.

To avoid false trips of the UV monitor, the power good circuit has a 10 µs glitch filter. Once the output voltage rises above the UV threshold and back into regulation, the fault is cleared and the power good signal goes high.

10.2.7 Current limit

A current limit condition for the switching regulators' occurs when the peak current in the high side power MOSFET exceeds the current limit threshold. The switch current is monitored using a sense FET and a comparator. The sense FET acts as a current detecting device by sampling a fraction of the current in the power MOSFET. This sampled current is compared to an internal reference to determine if the regulator is exceeding the current limit or not.

If the peak switch current reaches the peak current limit threshold (I_{SHORT}), the regulator will start the cycle by cycle current limit operation, the power good signal is pulled low after the 10 µs glitch filter, and a 10 ms current limit timer (t_{LIM}) begins. The regulator will stay in this mode of operation until one of the following occur:

- The current is reduced back to normal levels before the current limit timer expires and normal operation is resumed.
- The current limit timer expires without regaining normal operation, at which time the regulator turns off. The regulator remains off for a 100 ms retry timeout period ($t_{TIMEOUT}$), after which the regulator will attempt a soft start cycle.
- The switch current continues to increase until it exceeds the cycle by cycle current limit by approximately 1.0 A. At this point the regulator shuts down immediately. The

regulator remains off for a 100 ms retry timeout period ($t_{TIMEOUT}$), after which the regulator will attempt a soft start cycle.

- The device reaches the thermal shutdown limit (T_{SD}), the regulator turns off.

10.2.8 Thermal shutdown

A thermal limit condition occurs when a power device reaches the thermal shutdown threshold (T_{SD}). The temperature of the power MOSFETs in the switching regulators and the LDO are monitored using a thermal sensing transistor located near the power devices.

If the temperature of a switcher or an LDO reaches the thermal shutdown threshold, the switcher or LDO regulator will switch off and the PGOOD output would indicate a fault by pulling low. The regulator will stay in this mode of operation until the temperature of the die has decreased by the hysteresis value, and the regulator will attempt a soft start cycle.

10.2.9 Power supplies

10.2.9.1 DC/DC1

This is a nonsynchronous switching buck regulator, utilizing a feed-forward voltage mode control, with external compensation. This is the only converter in this IC that will regulate from a wide input supply voltage of 9.0 V to 18 V. It is capable of generating a 2.0 V to 5.25 V output at 1.5 A.

10.2.9.2 DC/DC2

This is a synchronous switching buck regulator whose input can be fed from DC/DC1, or an external 1.5 V to 6.0 V source. It utilizes voltage mode control with external compensation. It is capable of generating a 0.7 V to 3.6 V output at 1.25 A.

10.2.9.3 DC/DC3

This buck regulator is identical to DC/DC2. Note that all three switching regulators switch at 800 kHz, and are 120° out of phase to help reduce system noise and input surge currents.

10.2.9.4 LDO

This low-dropout regulator can feed off of any of the switching regulators or from an external 1.5 V to 6.0 V source. The dropout voltage is 250 mV at the rated load. It is capable of generating a 0.7 V to 3.6 V output at 400 mA.

10.3 Design and component guidelines

10.3.1 Input/output configuration

The 34700 has independent inputs for each regulator. This allows a high degree of flexibility regarding the IC configuration.

First, consider what supplies are available in the application, and the input voltage range for each regulator. Only Buck Converter 1 has a 9.0 V to 18 V input voltage range. All the other regulators have a 1.5 V to 6.0 V input voltage range.

Next, consider the output voltages and currents required, and how best to match them to the 34700. Buck Converter 1 is capable of 2.0 V to 5.25 V at 1.5 A, while Buck Converters 2 and 3 are capable of 0.7 V to 3.6 V at 1.25 A each. The LDO is capable of 0.7 V to 3.6 V at a 400 mA output.

Some sample configurations are show in Figure 22 through Figure 24. Note that not all combinations are shown, and all the regulators require an input voltage higher than the output voltage.

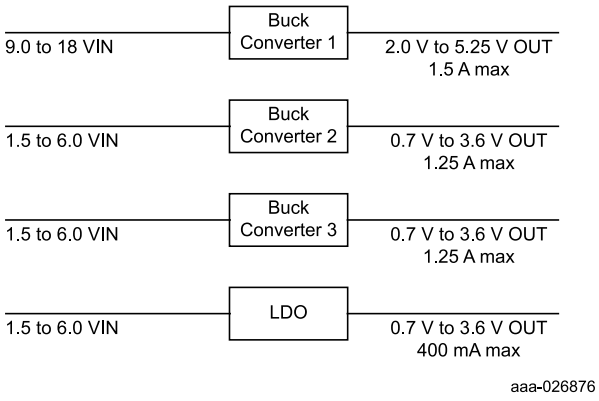


Figure 22. General configuration

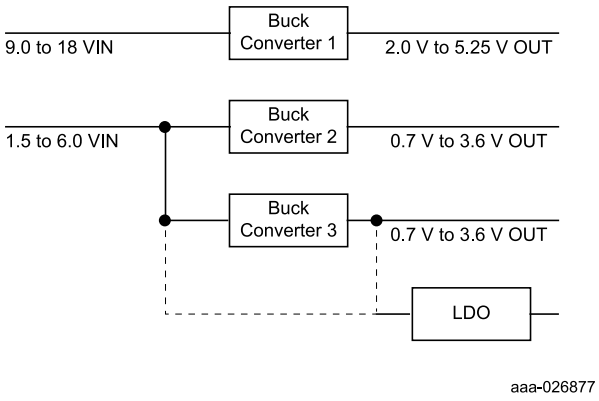


Figure 23. Dual input supply configuration

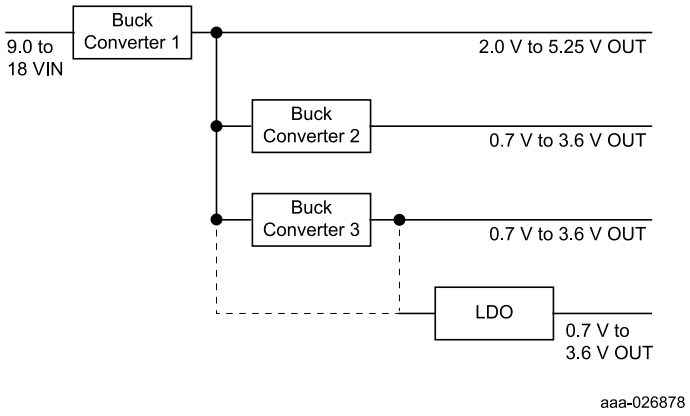


Figure 24. Single input supply configuration

10.3.2 Input/output power

Based on the application specifications and the regulator's configuration, the input and output power requirements need to be checked. For the LDO, the input and output powers are calculated:

$$P_{OUT(LDO)} = V_{OUT} \times I_{OUT}$$

$$P_{IN(LDO)} = V_{IN} \times I_{IN}$$

$$I_{IN} = I_{OUT}$$

For the buck converters, the input and output powers are calculated:

$$P_{OUT(BUCK)} = V_{OUT} \times I_{OUT}$$

$$P_{IN(BUCK)} = \frac{P_{OUT(BUCK)}}{\eta}$$

$$I_{IN} = \frac{P_{IN(BUCK)}}{V_{IN}}$$

Where η is the estimated efficiency of the buck converters, use 0.85 for the initial estimate.

When making the power calculations, be sure to include any input currents from regulators that are connected to the converter as part of the output current. For example, the input currents of Buck Converters 2 and 3 should be added to the system load current of Buck Converter 1 shown in Figure 24. After completing the calculations for all the regulators, check to make sure there are no violations of the power budget –

input currents exceeding supply current capabilities, or output currents exceeding the regulator's rating.

10.3.3 Minimum/maximum duty limit

Based on the application specifications, the minimum and maximum duty cycle of the buck converters need to be checked against the limits. For Buck Converter 1, there is a minimum limit of 16 % and a maximum limit of 68.4 %. For Buck Converters 2 and 3 there is a maximum limit of 83.6 %. The duty cycle for a buck converter is calculated using:

$$D = \frac{V_{OUT}}{V_{IN}} \times 100\%$$

This equation works for calculating the minimum duty cycle, however, the above formula does not take into account load currents and losses. A more accurate equation for calculating the maximum duty under load follows:

$$D_{MAX} = \frac{V_{OUT} + (R_{DO}+R_{DC}) \times I_{OUT}}{V_{IN(MIN)}} \times 100\,\%$$

Where R_{DO} is the equivalent dropout resistance of the buck converter and R_{DC} is the DC resistance of the inductor.

Check to make sure all the buck converters are within the duty cycle limit. Converters, where the calculated maximum duty cycle exceeds the limit, run the risk of dropping out of regulation under load. Conversely, the maximum duty cycle limit can be used to predict the maximum load current that can be drawn without the output dropping out of regulation.

$$I_{OUT(MAX)} = \frac{\frac{D_{MAX}-V_{IN}}{100\%}-V_{OUT}}{(R_{DO}+R_{DC})}$$

10.3.4 LDO dropout and power dissipation

The input of the LDO needs to exceed the output voltage by a minimum of 250 mV, in order to maintain regulation. If the input voltage falls below the dropout level, the output voltage will also start to fall and begin to track the input voltage down. However, choosing an input voltage that exceeds the output voltage by a large amount is not recommended either. This is due to increased power dissipation. The linear regulators power dissipation is calculated using:

$$P_{DISS} = (V_{OUT} - V_{IN}) \times I_{OUT}$$

Since the maximum power dissipation for the LDO is 375 mW, the user can determine what the limits are for the LDO's input voltage.

$$V_{OUT} + 0.25V \leq V_{IN} \leq V_{OUT} + \frac{0.375}{I_{OUT}}$$

10.3.5 Cascaded operation, sequencing, and leakage

When the 34700 is configured for cascaded operation, where the output of one regulator powers the input of another regulator (see Figure 24), the startup sequence also needs to be cascaded. The output voltage of the first regulator needs to be up and stable before enabling the downstream regulator, otherwise startup overshoot can occur.

Even without being configured for cascaded operation, the user may prefer the cascaded sequence to prevent startup latch-up or race conditions. With the four independent enables provided, the user can program any power up sequence that the application requires. The enable pins can be controlled by a host processor, a programmable logic device, or a power supply sequencer IC. If the application requires a simpler implementation of the cascaded sequence startup, a single enable signal can be used to start the first regulator in the sequence. When the first regulator is near or in regulation, its output is used to enable the next regulator in the sequence. See Figure 25. Note that there is a time delay from when the enable signal is asserted, until when the soft start ramp begins. For Buck Converter 1, the delay is typically 1.0 ms. For Buck Converter 2 and 3, the delay is typically 160 µs.

When sequencing the regulators on, one parameter that must be considered is the leakage specification. Buck Converters 2 and 3 exhibit 400 µA of leakage current between VIN and the switch node. This results in the output voltage floating up if the load impedance is high. In cases where the output voltage is floating, it is recommended adding a 1.0 KOhm resistor between the output and ground.

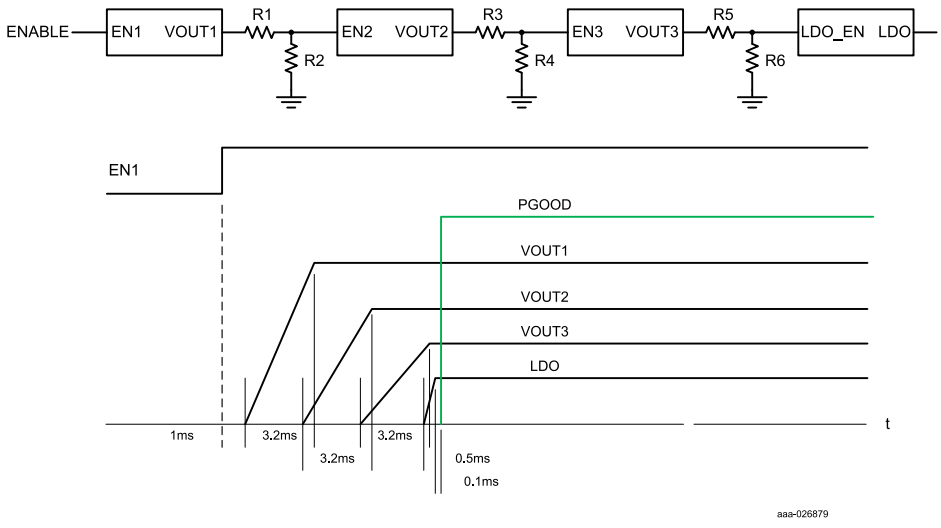


Figure 25. Cascade sequence

10.3.6 Shutdown sequence

The shutdown sequence is controlled by the enable pins. By pulling the ENABLE pin low or letting it float, the corresponding regulator is disabled. If the application is being controlled by the host processor or programmable logic device, the regulators can be shutdown in any order. Most power supply sequencer ICs shutdown the regulators in the

reverse order of their startup. The first regulator that is turned on is the last regulator to be turned off. For the single ENABLE pin sequencer shown in Figure 25, the shutdown order is the same as for startup; the first regulator that is turned on, is the first regulator turned off.

10.3.7 Layout guidelines

The layout of any switching regulator requires careful consideration. First, there are high di/dt signals present, and the traces carrying these signals need to be kept as short and as wide as possible to minimize the trace inductance, and therefore reduce the voltage spikes they can create. To do this an understanding of the major current carrying loops is important. See Figure 26. These loops, and their associated components, should be placed in such a way as to minimize the loop size to prevent coupling to other parts of the circuit. Also, the current carrying power traces and their associated return traces should run adjacent to one another, to minimize the amount of noise coupling. If sensitive traces must cross the current carrying traces, they should be made perpendicular to one another to reduce field interaction.

Second, small signal components which connect to sensitive nodes need consideration. The critical small signal components are the ones associated with the feedback circuit. The high impedance input of the error amp is especially sensitive to noise, and the feedback and compensation components should be placed as far from the switch node, and as close to the input of the error amplifier as possible. Other critical small signal components include the bypass capacitors for VIN, VGREG, and VDDI. Locate the bypass capacitors as close to the pin as possible.

The use of a multi-layer printed circuit board is recommended. Dedicate one layer, usually the layer under the top layer, as a ground plane. Make all critical component ground connections with vias to this layer. Make sure that the power grounds, GND2 and GND3, are connected directly to the ground plane and not routed through the thermal pad or analog ground. Dedicate another layer as a power plane and split this plane into local areas for common voltage nets.

The IC input supply (VIN) should be connected through an RC filter to the 9.0 to 18 V input supply, to prevent noise from Buck Regulator 1's power input (VIN1) from injecting switching noise into the analog circuitry. If possible, further isolation can be made by routing a dedicated trace for VIN, and a separate trace for VIN1.

In order to effectively transfer heat from the top layer to the ground plane and other layers of the printed circuit board, thermal vias need to be used in the thermal pad design. It is recommended that 5 to 9 vias be spaced evenly and have a finished diameter of 0.3 mm.

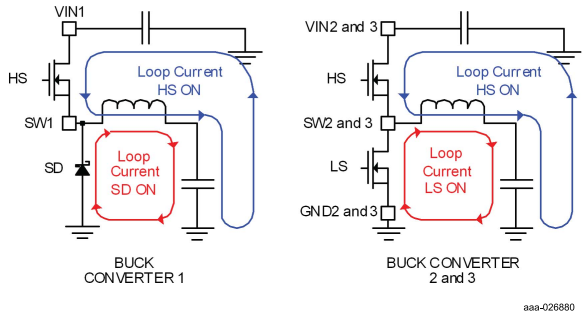


Figure 26. Current loops

10.3.8 Component selection

10.3.8.1 Setting the output voltage

For all the regulators, the feedback resistor divider sets the output voltage. See Figure 27 for the feedback and compensation components referred to in the equations. For the buck regulators, choose a value of about 20 K for the upper resistor, and calculate the lower resistor using the following equations:

$$R_{BOT} = \frac{R_{TOP} \times V_{REF}}{V_{OUT} - V_{REF}}$$

$$V_{OUT} = V_{REF}\left(\frac{R_{TOP}}{R_{BOT}} + 1\right)$$

where, V_{REF} = 0.7 V

For the LDO regulator choose a value of about 10 K for the lower resistor, and calculate the upper resistor using the following equations:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

$$V_{OUT} = V_{REF}\left(\frac{R_{TOP}}{R_{BOT}} + 1\right)$$

where, V_{REF} = 0.7 V

Choose the closest standard resistance values, check the output voltage by using the equations above, and adjust the values if necessary.

10.3.8.2 Setting the Enable for Cascade sequencing

For the cascaded startup sequence shown in Figure 25, the resistor divider sets the output voltage level where the next the next regulator in the sequence will start or shutdown. For top resistors R1, R3, and R5, choose a value of 10 K, and calculate the value for the bottom resistors R2, R4, and R6, using the following equation:

$$R_{BOT} = \frac{0.78 \times R_{TOP}}{0.95V_{OUT} - 0.78}$$

where, V_{OUT} is the value calculated above using standard value resistors.

Choose the closest standard resistance values and check the output voltage levels that enable and disable the regulator in sequence, using the following equations, and adjust if necessary:

$$V_{OUT(EN)} = 0.78\left(\frac{R_{TOP}+R_{BOT}}{R_{BOT}}\right)$$

$$V_{OUT(DISABLE)} = 0.61\left(\frac{R_{TOP}+R_{BOT}}{R_{BOT}}\right)$$

These equations should give an enable of ~95 % of V_{OUT}, and a disable of ~75 % of V_{OUT}.

10.3.8.3 Catch diode

An external catch diode is required for Buck Converter 1 to provide a return path for the inductor current when the high-side switch is off. The catch diode should be located close to the 34700 and connected using short, wide traces. See Section 10.3.7 "Layout guidelines" for more details.

It is recommended to use a Schottky diode, due to their low forward voltage drop and fast switching speed. This provides the best efficiency and performance, and is especially true when the output voltage is less than 5.0 V. Choose a Schottky with a 2.0 to 3.0 A average output current rating and a reverse voltage specified for 30 V.

10.3.8.4 Inductor

The output inductor is sized to meet the output voltage ripple requirements, and to minimize the load transient response time. For continuous conduction mode (CCM) operation, where the inductor does not fully discharge during the switch off time, and assuming an ideal switch and catch diode, the following equation is used:

$$L = \left(V_{IN(MAX)} - V_{OUT}\right) \times \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{I}{f_{SW}} \times \frac{I}{N \times I_{OUT(MAX)}}$$

where, f_{SW} is the switching frequency and N is the ripple current to output current ratio.

A high ripple current to output current ratio gives improved load transient response, but also increases output ripple, and results in lower efficiency. A value of 0.3 to 0.4 for N represents a good trade off between efficiency, ripple, and load transient response.

After calculating a value for the inductor, choose the closest standard value and then determine the ripple current and peak current using the following equations:

$$\Delta = \frac{\left(V_{IN(MAX)} - V_{OUT}\right)}{L} \times \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{I}{f_{SW}}$$

$$I_{PEAK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

The peak inductor current determines the required saturation current rating of the inductor. Choose an inductor with a saturation current rating that's large enough to

compensate for circuit tolerances. The minimum acceptable margin for this purpose is at least 20 % above the calculated rating.

To minimize copper losses, choose an inductor with the lowest possible DCR. As a general rule of thumb, look for a DCR of approximately 5.0 mOhms per µH of inductance.

10.3.8.5 Output capacitor

The output capacitor is required to minimize the voltage overshoot and undershoot in response to load transients, and to reduce the ripple present at the output of a buck regulator. The same holds true for the linear regulator.

For the LDO, a 10 µF, low ESR capacitor is required as the output capacitor. Other values may result in instability. Make sure the capacitor has good temperature characteristics, and a suitable voltage rating. As a general rule, choose ceramic capacitors with a X5R, or X7R dielectric and a voltage rating of 1.5 to 2 times the output voltage, but check with the manufacturer for detailed information.

For the buck converters, large transient load overshoots are caused by insufficient capacitance, and large voltage ripple is caused by insufficient capacitance, as well as high equivalent series resistance (ESR) in the capacitor. To meet the application requirements, the output capacitor must be specified with ample capacitance and low ESR.

To deal with overshoot, where the output voltage overshoots its regulated value when a full load is removed from the output, the output capacitor must be large enough to prevent the energy stored in the inductor from causing the voltage to spike above the specified maximum output voltage. The amount of capacitance required can be estimated using the following equation:

$$C_{OUT} = \frac{L(I_{PEAK})^2}{(\Delta V + V_{OUT})^2 - V_{OUT}^2}$$

where, ΔV is the maximum output voltage overshoot.

Allow a 20 % capacitance tolerance and choose the closest standard value.

The ESR of the output capacitor usually dominates the output voltage ripple. The maximum ESR can be calculated using the equation:

$$C_{ESR} = \frac{V_{RIPPLE}}{\Delta I_L}$$

where, V_{RIPPLE} is the specified ripple voltage allowed.

10.3.8.6 Input capacitor

Generally, a mix of bypass capacitors is used for the input supply. Use a small ceramic capacitor for high frequency decoupling, and bulk capacitors to supply the surge of current required each time the high-side MOSFET turns on. Place the small ceramic capacitor close to the power input pins.

For reliable operation, select the bulk input capacitors with voltage and RMS ripple current ratings above the maximum input voltage, and the largest RMS current required

by the application. As a general guideline, the capacitor's voltage rating should be around 1.5 times the maximum input voltage, but the manufacturer's de-rating information should be followed. The RMS ripple current rating that the bulk input capacitors require can be estimated by the following equation:

$$I_{IN(RMS)} = I_{OUT}\sqrt{D - D^2}$$

where $D = V_{OUT}/V_{IN}$.

The worst case occurs when $V_{IN} = 2 \times V_{OUT}$, yielding a worst case ripple current of $I_{IN(RMS)} = I_{OUT}/2$.

The bulk input capacitance required for a buck converter depends on the impedance of the input supply. For common laboratory supplies, 10 to 20 µF of capacitance per ampere of input ripple current is usually sufficient. Use this general guideline as a starting point and adjust the input capacitance based on actual test results.

Tantalum capacitors can be used as input capacitors, but proper de-rating must be used or they can fail "short" and present a fire hazard. Ceramic capacitors and aluminum electrolytic capacitors don't have this failure mechanism, making them a preferred choice. However, ceramic capacitors can exhibit piezo effect and emit an audible buzz. Polymer capacitors do not have this audible noise problem, but they can also fail "short". However, polymer capacitors are much more robust than tantalums, and therefore are suitable as input capacitors. Consult the manufacturer for more information on the use and de-rating of capacitors.

10.3.8.7 Bootstrap capacitor

The external bootstrap capacitor is part of a charge pump circuit which is used to drive the gate of the high-side N- MOSFET. This capacitor develops a floating voltage supply which is referenced to the switch node (SW) or the source of the high-side MOSFET. The bootstrap capacitor is charged every cycle, when the low-side MOSFET or the catch diode conducts, to a voltage of about V_{GREG}. To turn the high side switch on, the bootstrap capacitor needs to be large enough to charge the gate-source capacitance of the N-MOSFET without a significant drop in voltage. For the 34700, the bootstrap capacitor should be 0.1 µF.

10.3.8.8 Compensation

The voltage mode buck converters used in the 34700 require a Type III compensation network as shown in Figure 27. The Type III network utilizes two zeroes to give a phase boost of 180°. This phase boost is necessary to counteract the double pole of the output LC filter.

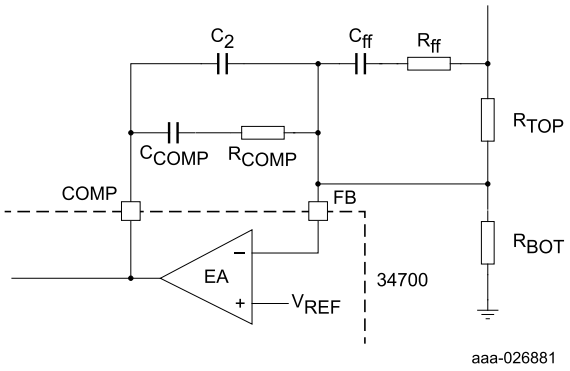


Figure 27. Type III compensation network

The closed loop transfer function is comprised of the modulator, the filter, and the compensation transfer functions. Before we can determine the compensation we need to first calculate the gains and break frequencies of the modulator and filter.

$$G_{MOD} = \frac{D_{MAX} \times V_{IN}}{V_{RAMP}}$$

where, G_{MOD} is the modulator gain, and D_{MAX} and V_{RAMP} are given in the electrical table.

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}}$$

where, f_{LC} is the location of the LC filter double pole.

$$f_{ESR} = \frac{1}{2\pi \times C \times ESR}$$

where, f_{ESR} is the location of the ESR zero, and ESR is the equivalent series resistance of the output capacitors.

As shown in Figure 27, the compensation network consists of the error amplifier (internal to the 34700), and the external resistors and capacitors. If designed properly, the compensation network will yield a closed loop transfer function with a high crossover (0 dB) frequency, and adequate phase margin to be stable. Use the following steps to calculate the compensation components.

1. Using the value for R_{TOP} and R_{BOT}, selected in Section 10.3.8.1 "Setting the output voltage", calculate the value of R_{COMP} for the desired converter bandwidth, f_0. Typically f_0 is chosen to be 1/10th of the switching frequency.

$$R_{COMP} = \frac{V_{RAMP} \times R_{TOP} \times f_0}{D_{MAX} \times V_{IN} \times f_{LC}}$$

This will set the high frequency gain of the error amplifier (R_{COMP}/R_{TOP}), and shift the open loop gain up to give the desired bandwidth.

2. Using the value for R_{COMP}, calculate the value of C_{COMP}, to place a zero, to cancel one of the double poles. This zero (f_{Z1}) is placed at a fraction of the LC double pole frequency.

$$C_{COMP} = \frac{1}{2\pi \times R_{COMP} \times K_{LC} \times f_{LC}}$$

where, K_{LC} is the fraction of the LC filter frequency = f_{Z1}/f_{LC}. Typical values for K_{LC} are 0.2 to 0.7, but begin with 0.5.

3. Using the values of R_{COMP} and C_{COMP}, calculate the value of C_2 to place a pole (f_{P1}) at the ESR zero frequency. Note that if ceramic capacitors are used for the output capacitors, the ESR zero will be at a very high frequency, making the calculated value of C_2 very small. If this is the case, C_2 may not be needed, saving a component and space.

$$G_{MOD}(f) = \frac{D_{MAX} \times V_{IN}}{V_{RAMP}} \times \frac{1 + s(f) \times ESR \times C}{1 + s(f) \times (ESR + DCR) \times C + s^2(f) \times L \times C}$$

$$H_{comp}(f) = \frac{1 + s(f) \times R_{COMP} \times C_{COMP}}{s(f) \times R_{TOP} \times (C_{COMP} + C_2)} \times \frac{1 + s(f) \times (R_{TOP} + R_{ff}) \times C_{ff}}{1 + s(f) \times R_{ff} \times C_{ff} \times \left(1 + s(f) \times R_{COMP} \times \left(\frac{C_{COMP} \times C_2}{C_{COMP} + C_2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \times H_{COMP}(f)$$

where s(f) = j × 2π × f

$$C_2 = \frac{C_{COMP}}{(2\pi \times R_{COMP} \times C_{COMP} \times f_{ESR})^{-1}}$$

4. Calculate the value of R_{ff} and C_{ff}, to place a zero (f_{Z2}) at the LC double pole frequency, and a pole (f_{P2}) at half the switching frequency.

$$R_{ff} = \frac{R_{TOP}}{\left(\frac{f_{SW}}{2 \times f_{LC}}\right)^{-1}}$$

$$C_{ff} = \frac{1}{\pi \times R_{ff} \times f_{SW}}$$

Choose the closest standard value for the compensation components. Although precision components are not required, do not use poor quality components that have large tolerances overtemperature. As a double check, it is recommended to use a mathematical model to plot the closed loop response. Check that the closed loop gain is within the error amplifier's open loop gain, and there is enough phase margin, and make adjustments as necessary. A stable control loop has a gain crossing with close to –20dB/decade, and a phase margin of at least 45°. The following equations describe the frequency response of the modulator, feedback compensation, and the closed loop.

A more intuitive representation of the mathematical model, is an asymptotic bode plot of the buck converter's gain versus frequency, as shown in Figure 28. Use of the previous steps should result in a compensation gain similar to the one shown in the bode plot. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at f_{P1} or f_{P2}, whichever is greater, against the capabilities of the error amplifier. For reference, the equations for the compensation break frequencies are given.

$$f_{Z1} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}}$$

$$f_{P1} = \frac{1}{2\pi \times R_{COMP} \times \left(\frac{C_{COMP} \times C_2}{C_{COMP} + C_2}\right)}$$

$$f_{Z2} = \frac{1}{2\pi \times (R_{TOP} + R_{ff}) \times C_{ff}}$$

$$f_{P2} = \frac{1}{2\pi \times + R_{ff} \times C_{ff}}$$

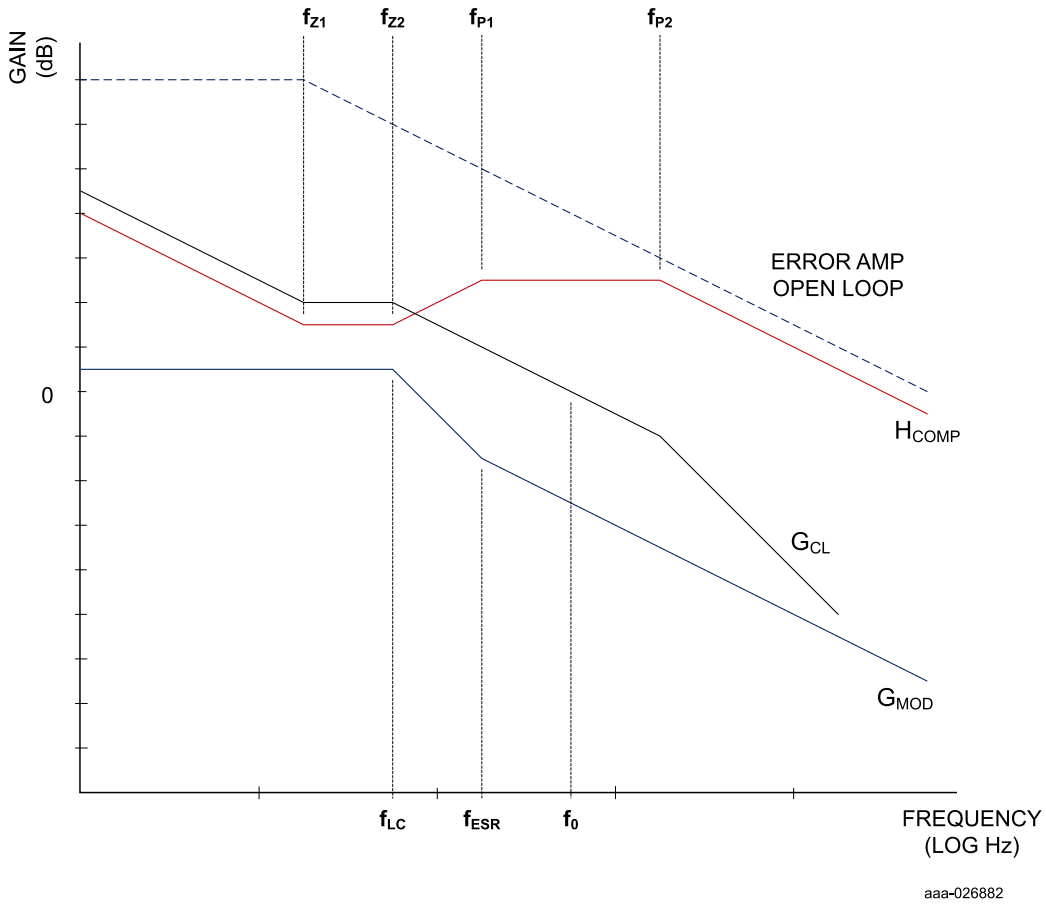


Figure 28. Bode plot of the buck converter

11 Application example

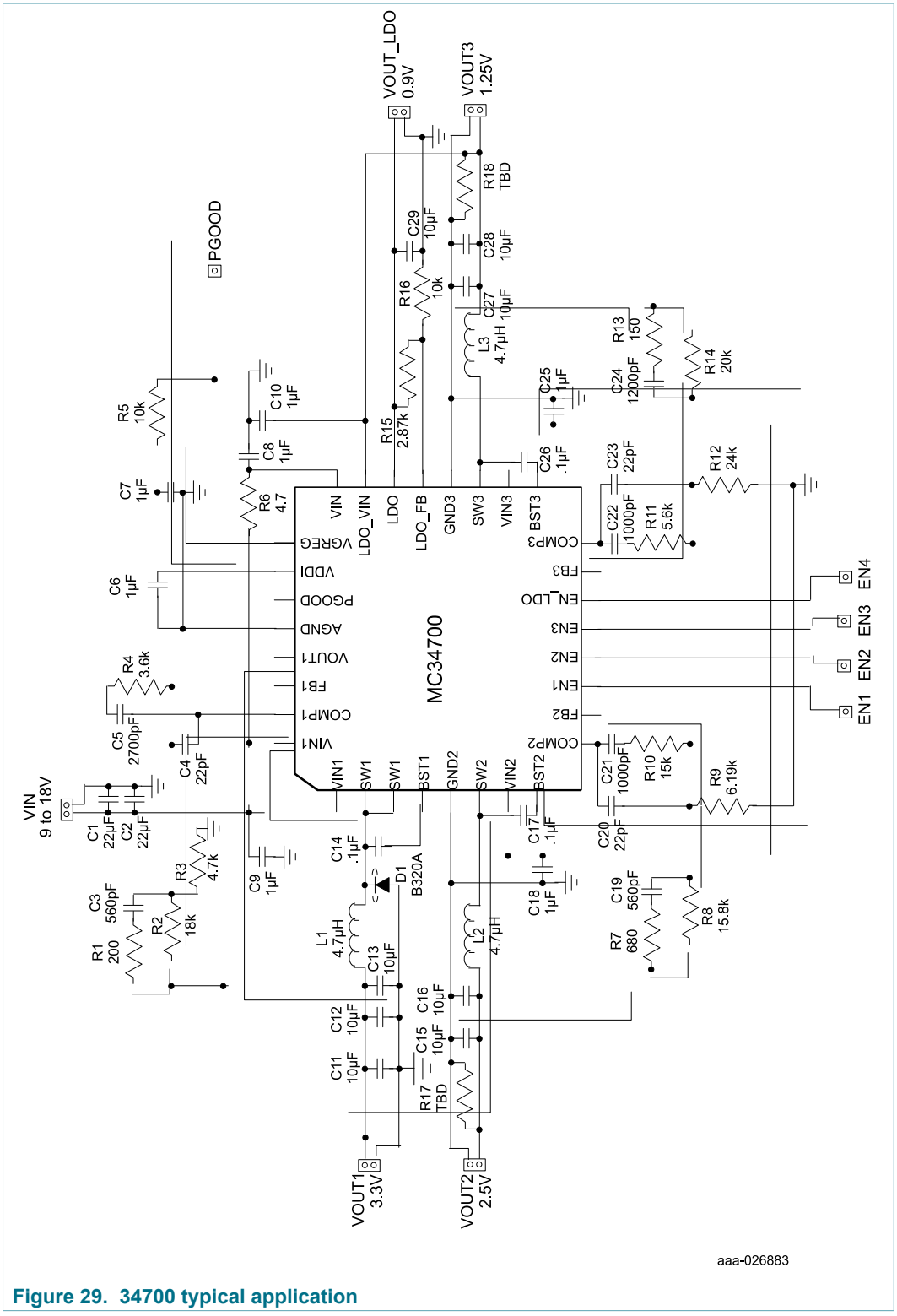


Figure 29. 34700 typical application

12 Bill of material

Table 4. MC34700 bill of material

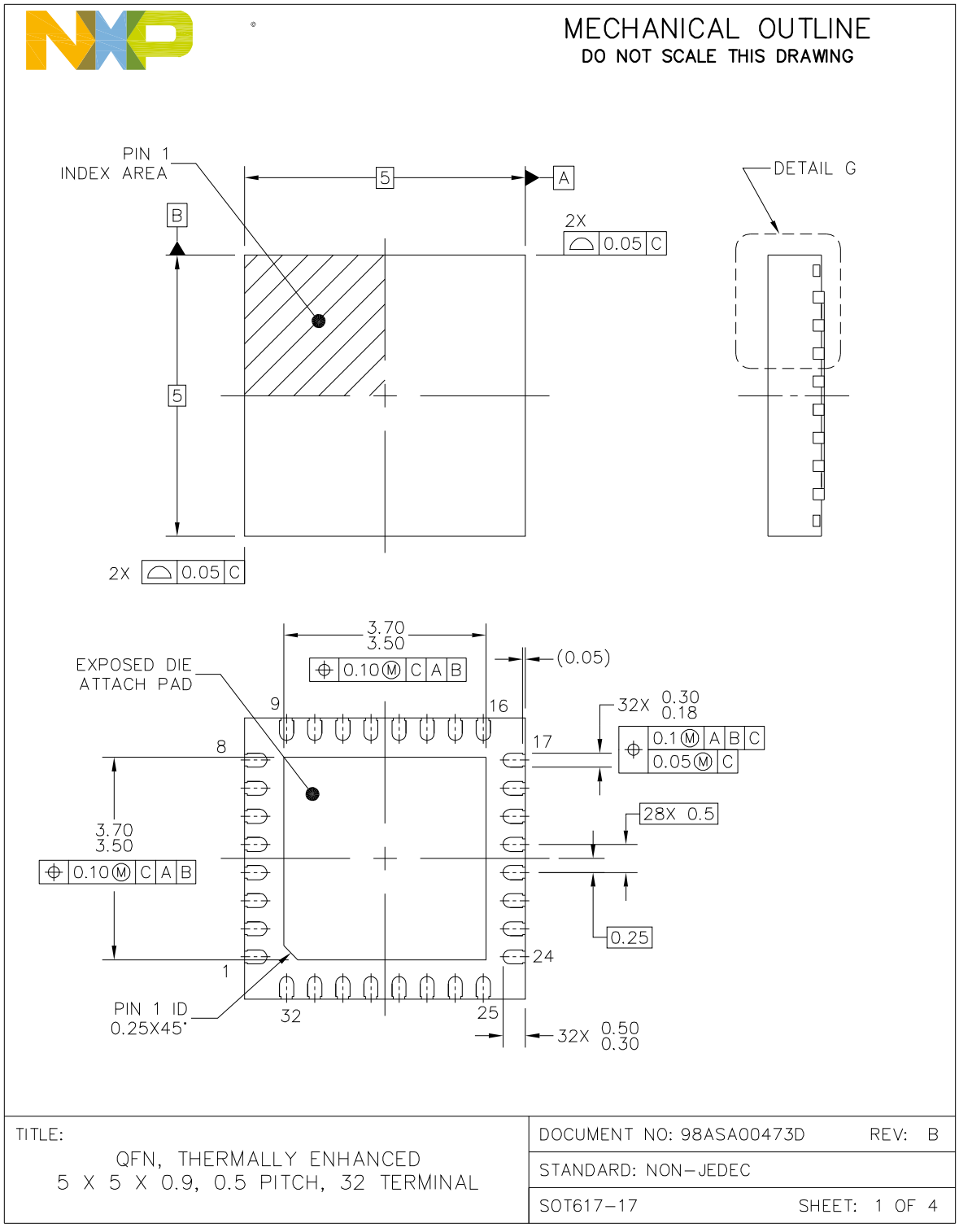
Item	Qty	Part designer	Value/rating	Part number/ manufacturer
R1	1	201/402/603 Metal or Thin Film Resistors	200 Ω	
R2	1	201/402/603 Metal or Thin Film Resistors	18.0 kΩ	
R3	1	201/402/603 Metal or Thin Film Resistors	4.70 kΩ	
R4	1	201/402/603 Metal or Thin Film Resistors	3.60 kΩ	
R5, R16	2	201/402/603 Metal or Thin Film Resistors	10.0 kΩ	
R6	1	201/402/603 Metal or Thin Film Resistors	4.7 Ω	
R7	1	201/402/603 Metal or Thin Film Resistors	680 Ω	
R8	1	201/402/603 Metal or Thin Film Resistors	15.8 kΩ	
R9	1	201/402/603 Metal or Thin Film Resistors	6.19 kΩ	
R10	1	201/402/603 Metal or Thin Film Resistors	15.0 kΩ	
R11	1	201/402/603 Metal or Thin Film Resistors	5.6 kΩ	
R12	1	201/402/603 Metal or Thin Film Resistors	24.0 kΩ	
R13	1	201/402/603 Metal or Thin Film Resistors	150 Ω	
R14	1	201/402/603 Metal or Thin Film Resistors	20.0 kΩ	
R15	1	201/402/603 Metal or Thin Film Resistors	2.87 kΩ	
C1, C2	2	25V 1210/1206 MLCC Capacitors X5R/X7R	22 µF	
C3, C19	2	50V 0402/0603 MLCC Capacitors COG	560 pF	
C4, C20, C23	3	50V 0402/0603 MLCC Capacitors COG	22 pF	
C5	1	50V 0402/0603 MLCC Capacitors X5R/X7R	2700 pF	
C6 - C10, C18, C25	7	25V 0402/0603 MLCC Capacitors X5R/X7R	1.0 µF	
C11-C13, C15, C16, C27 - C29	8	10V 1210/1206 MLCC Capacitors X5R/X7R	10 µF	
C14, C17, C26	3	25V 0402/0603 MLCC Capacitors X5R/X7R	0.1 µF	
C21, C22	2	50V 0402/0603 MLCC Capacitors X5R/X7R	1000 pF	
C24	2	50V 0402/0603 MLCC Capacitors X5R/X7R	1200 pF	
L1, L2, L3	3	3A Shielded Inductor	4.7 µH	
D1	1	2A, 30V Schottky Diode	B230A	

Note:

NXP does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

13 Package outline

For the most current package revision, visit www.nxp.com and perform a keyword search using the 98ASA00473D listed.



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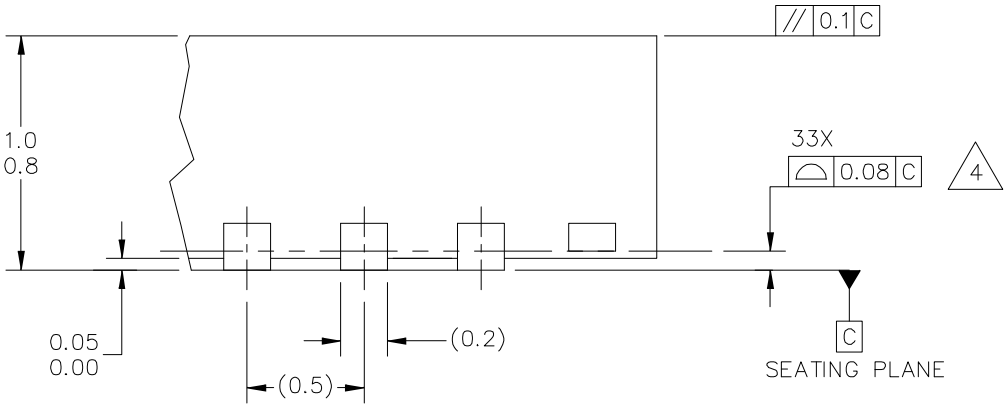

DETAIL G
VIEW ROTATED 90°CW

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	STANDARD: NON-JEDEC
	SOT617-17 SHEET: 2

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	STANDARD: NON–JEDEC	
	SOT617–17	SHEET: 3

Figure 30. Package outline

14 Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supercedes
MC34700 v6.0	20170911	Product	PCN 201612003F01	MC34700 v5.0
Modifications	• Changed the 98A package drawing from 98ASA10800D to 98ASA00473D			

15 Legal information

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Date of release: 11 September 2017