Mono 7W Class D Amplifier

ABSOLUTE MAXIMUM RATINGS

PVDD to PGND .....-0.3V to +30V
AGND to PGND .....-0.3V to +0.3V
IN, PRE, PC, COM to AGND .....-0.3V to (V_{REG} + 0.3V)
$\overline{MUTE}$, $\overline{SHDN}$ to AGND .....-0.3V to +6V
REG to AGND .....-0.3V to (V_S + 0.3V)
V_S to AGND .....-0.3V to +6V
OUT+, OUT- to PGND .....-0.3V to (PVDD + 0.3V)
C1N to PGND .....-0.3V to (PVDD + 0.3V)
C1P to PGND .....(PVDD - 0.3V) to (V_{CHOLD} + 0.3V)
CHOLD to PGND .....(V_{C1P} - 0.3V) to +36V
OUT+, OUT-, Short Circuit to PGND or PVDD .....Continuous
Thermal Limits (Notes 1, 2)
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN Single-Layer PCB (derate 20.8mW/°C above +70°C).....1666.7mW
θ_{JA}.....48°C/W
θ_{JC}.....3°C/W
Continuous Power Dissipation
24-Pin TQFN Multiple-Layer PCB (derate 27.8mW/°C above +70°C).....2222.2mW
θ_{JA}.....36°C/W
θ_{JC}.....3°C/W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Thermal performance of this device is highly dependent on PCB layout. See the *Applications Information* section for more detail.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PVDD} = 12V, V_{AGND} = V_{PGND} = 0, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, C1 = 0.1µF, C_{IN} = 0.47µF, C2 = C_{COM} = C_{REG} = 1µF, R_{IN} = R_{FB} = 20kΩ, R_L = ∞, AC measurement bandwidth 22Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLIFIER DC CHARACTERISTICS						
Speaker-Supply Voltage Range	PVDD	Inferred from PSRR test	8		28	V
Undervoltage Lockout	UVLO			6.8		V
Quiescent Supply Current	I_{PVDD}	T_A = +25°C		15	20	mA
					25	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0, T_A = +25°C		1	10	µA
REG Voltage	V_{REG}		4.0	4.2	4.5	V
Preregulator Voltage	V_S			4.85		V
COM Voltage	V_{COM}		1.94	2.06	2.16	V
INPUT AMPLIFIER CHARACTERISTICS						
Capacitive Drive	C_L	No sustained oscillation		30		pF
Output Swing		Sinking ±1mA (Note 4)		2.05		V
Open-Loop Gain	A_{VO}			88		dB
Input Offset Voltage	V_{OS}	IN to COM		±2		mV
Input Amplifier Slew Rate				2.5		V/µs
Input Amplifier Unity-Gain Bandwidth				3.5		MHz

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ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = 12V, V_{AGND} = V_{PGND} = 0, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, C1 = 0.1µF, C_{IN} = 0.47µF, C2 = C_{COM} = C_{REG} = 1µF, R_{IN} = R_{FB} = 20kΩ, R_L = ∞, AC measurement bandwidth 22Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT AMPLIFIER CHARACTERISTICS							
Output Amplifier Gain	A_V	Preamplifier gain = 0dB (Note 7)		13.1	13.6	14.1	dB
Output Current Limit				3	4.6		A
Output Offset	V_{OS}	OUT+ to OUT-, T_A = +25°C			±2	±10	mV
Power-Supply Rejection Ratio	PSRR	V_{PVDD} = 8V to 28V, T_A = +25°C		65	80		dB
		f = 1kHz, 100mV_{P-P} ripple			88		
Output Power	P_{OUT}	THD+N = 10%, R_L = 8Ω (Note 5)		6	7.4		W
		THD+N = 10%, R_L = 4Ω (Note 6)			13		
THD + Noise	THD+N	P_{OUT} = 2W, f = 1kHz, R_L = 8Ω (Note 5)			0.06		%
Signal-to-Noise Ratio	SNR	A-weighted, P_{OUT} = THD+N at 1%, f_{IN} = 1kHz			97		dB
Noise	V_N	A-weighted (Note 4)			100		μV_{RMS}
Efficiency	η	P_{OUT} = 4W			85		%
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples/second, A-weighted (Notes 4, 5, 8)	Into shutdown		38		dBV
			Out of shutdown		38		
			Into mute		38		
			Out of mute		38		
Switching Frequency				270	300	330	kHz
Spread-Spectrum Bandwidth					±4		kHz
Thermal-Shutdown Level					+160		°C
Thermal-Shutdown Hysteresis					30		°C
Turn-On Time	t_{ON}	From shutdown to full operation			9	10	ms
DIGITAL INTERFACE ($\overline{SHDN}$, $\overline{MUTE}$)							
Input-Voltage High	V_{INH}			2			V
Input-Voltage Low	V_{INL}					0.8	V
Input-Voltage Hysteresis					50		mV
Input Leakage Current		T_A = +25°C				±10	µA

Note 3: All devices are 100% production tested at T_A = +25°C, and all temperature limits are guaranteed by design.
Note 4: Amplifier inputs AC-coupled to GND.
Note 5: 8Ω resistive load in series with 68mH inductive load connected across OUT+ and OUT- outputs.
Note 6: 4Ω resistive load in series with 33µH inductive load connected across OUT+ and OUT- outputs for V_{PVDD} ≤ 12V.
Note 7: Output amplifier gain is defined as:

$$20 \times \log\left(\frac{|(V_{OUT+}) - (V_{OUT-})|}{|V_{PRE}|}\right)$$

Note 8: Mode transition controlled by $\overline{SHDN}$ and $\overline{MUTE}$.

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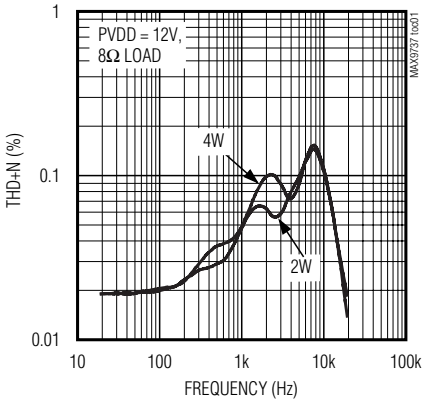
Mono 7W Class D Amplifier

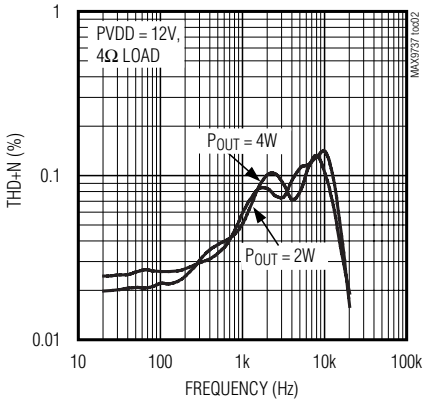
Typical Operating Characteristics

(V_{PVDD} = 12V, V_{GND} = V_{PGND} = 0, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, R_{IN} = R_{FB} = 20kΩ, unless otherwise noted.)

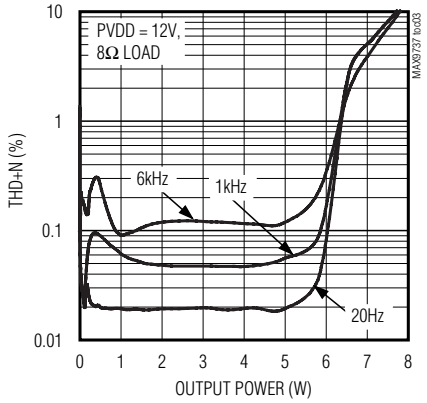
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



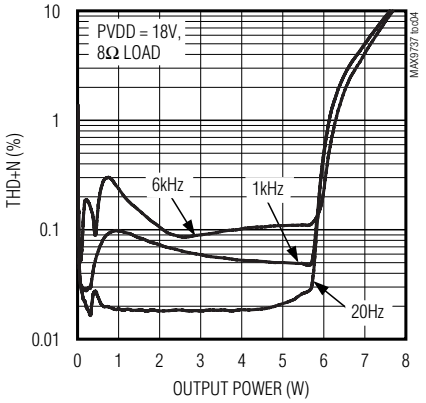
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



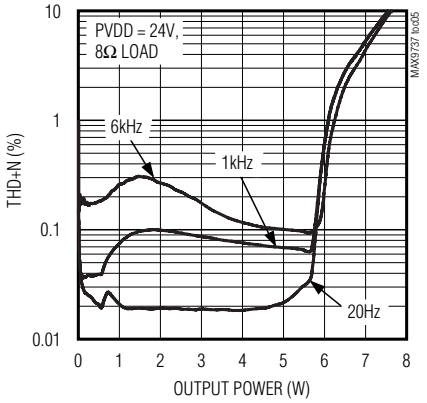
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



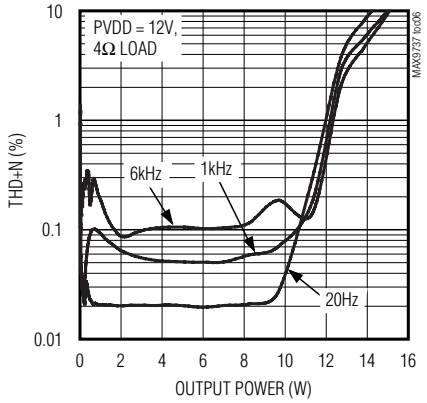
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



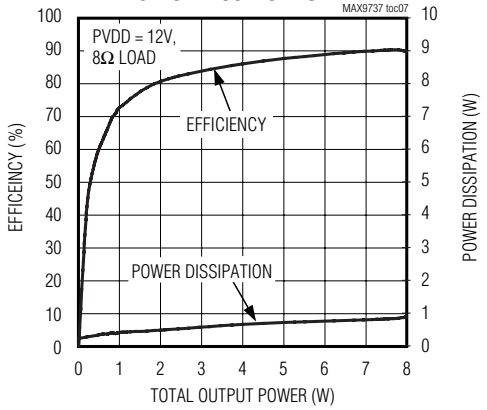
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



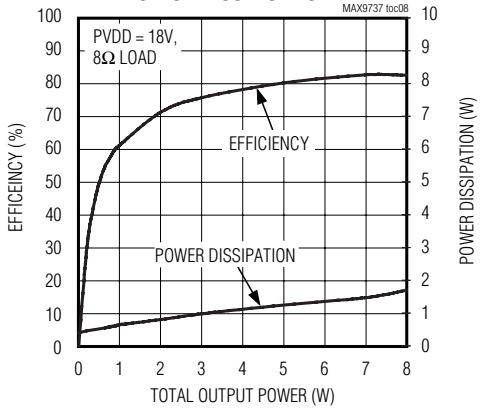
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



EFFICIENCY vs. TOTAL OUTPUT POWER



EFFICIENCY vs. TOTAL OUTPUT POWER



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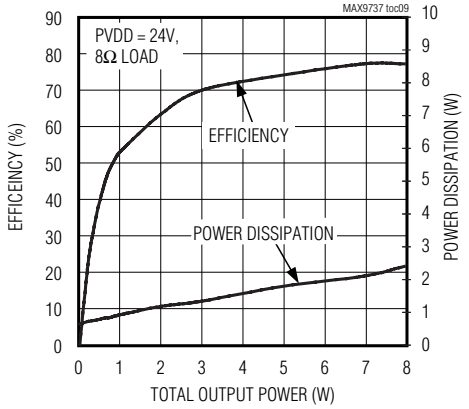
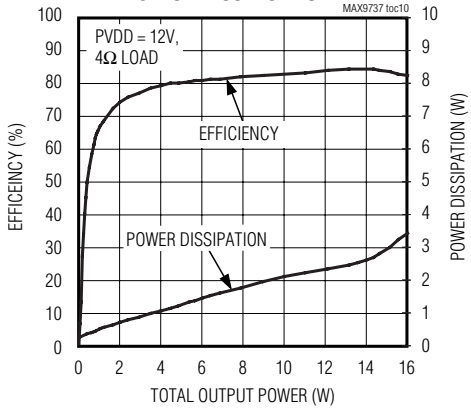
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{GND} = V_{PGND} = 0, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, R_{IN} = R_{FB} = 20kΩ, unless otherwise noted.)

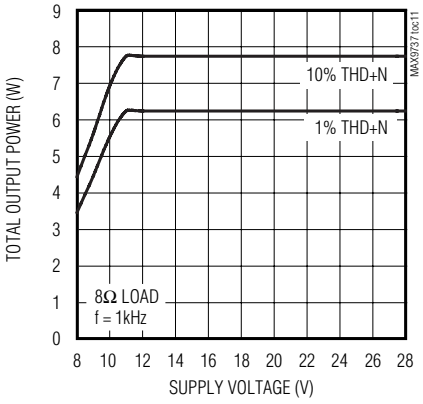
EFFICIENCY vs. TOTAL OUTPUT POWER



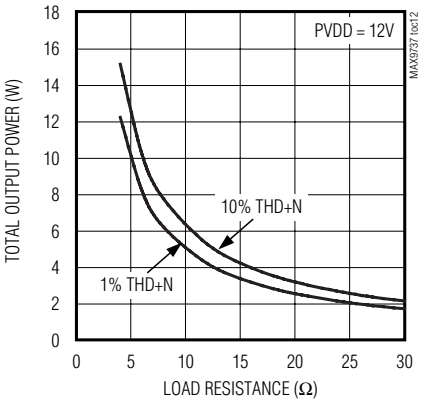
EFFICIENCY vs. TOTAL OUTPUT POWER



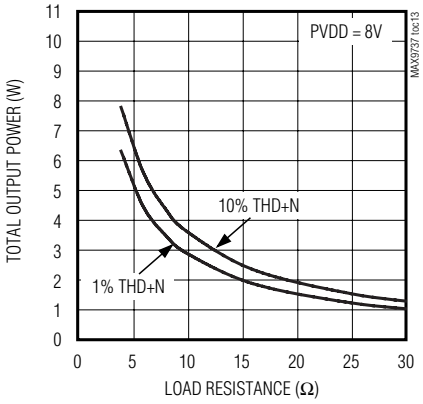
TOTAL OUTPUT POWER vs. PVDD



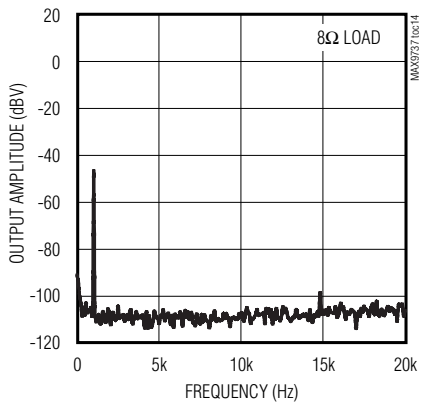
TOTAL OUTPUT POWER vs. LOAD RESISTANCE



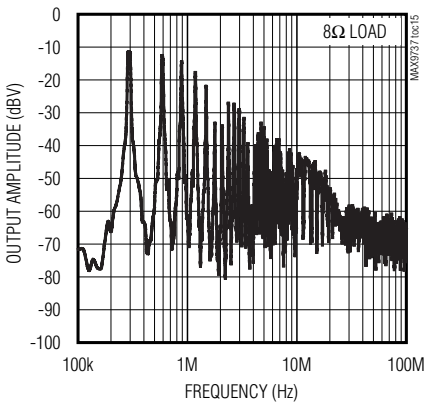
TOTAL OUTPUT POWER vs. LOAD RESISTANCE



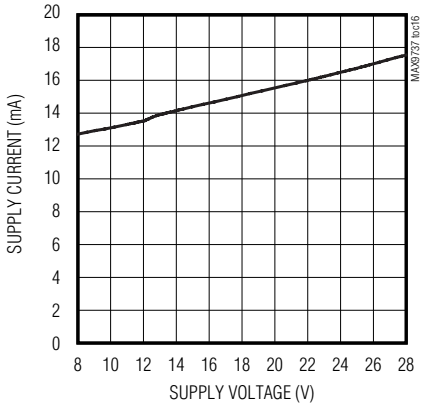
INBAND OUTPUT SPECTRUM



WIDEBAND OUTPUT SPECTRUM



SUPPLY CURRENT vs. PVDD SUPPLY VOLTAGE



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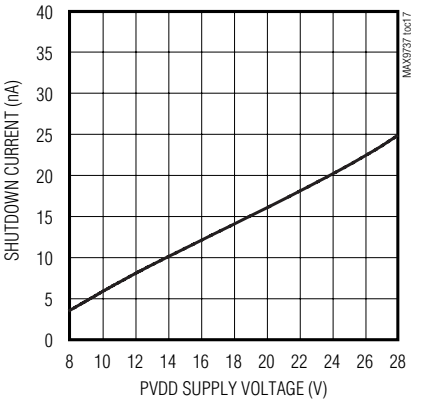
Mono 7W Class D Amplifier

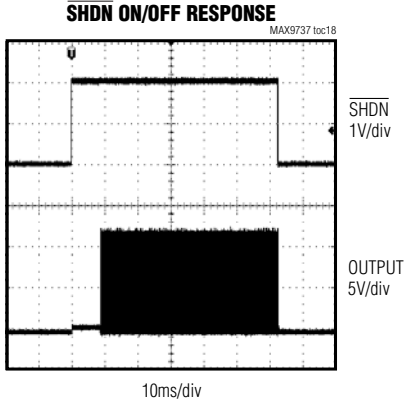
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{GND} = V_{PGND} = 0, $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, R_{IN} = R_{FB} = 20kΩ, unless otherwise noted.)

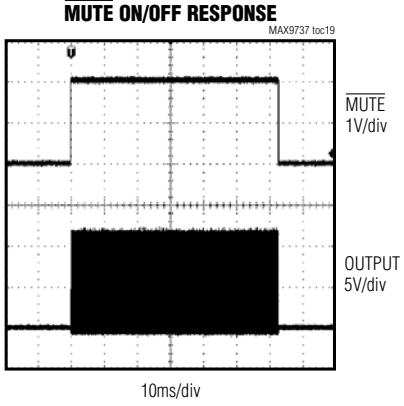
SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



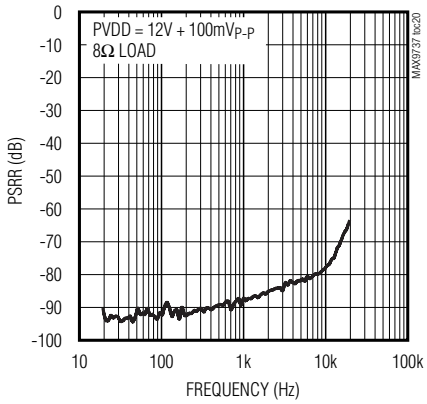
$\overline{SHDN}$ ON/OFF RESPONSE



$\overline{MUTE}$ ON/OFF RESPONSE



PSRR



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Pin Description

PIN	NAME	FUNCTION
1, 17, 18	PVDD	Power Supply. Bypass PVDD to PGND with a 1µF capacitor connected to pin 1 and a 1µF capacitor connected to pins 17 and 18.
2	CHOLD	Charge-Pump Output. Connect a 1µF capacitor to PVDD.
3, 10, 11	AGND	Analog Ground
4	$\overline{MUTE}$	Mute Input. Drive $\overline{MUTE}$ low to place the device in mute mode.
5	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ low to place the part in shutdown mode.
6	PC	Input Capacitor Precharge Connection. Connect between input resistor, R_{IN}, and input coupling capacitor, C_{IN}.
7	IN	Op Amp Inverting Input.
8	PRE	Op Amp Output. PRE is the output of the input operational amplifier.
9	COM	Internal 2.0V Bias. Bypass COM to AGND with a 1µF capacitor.
12	REG	Internal 4.2V Bias. Bypass REG to AGND with a 1µF capacitor.
13, 14	V_S	Internal 5.0V Bias. Bypass V_S to AGND with a 1µF capacitor.
15	C1N	Charge-Pump, Flying-Capacitor Negative Terminal. Connect C1N to C1P through a 0.1µF capacitor.
16	C1P	Charge-Pump, Flying-Capacitor Positive Terminal. Connect C1P to C1N through a 0.1µF capacitor.
19, 20	OUT-	Negative Speaker Output
21, 22	PGND	Power Ground
23, 24	OUT+	Positive Speaker Output
—	EP	Exposed Pad. Must be externally connected to PGND.

Detailed Description

The MAX9737 filterless, mono class D audio power amplifier offers Class AB audio performance and Class D efficiency with minimal board space. The device operates from an 8V to 28V supply range.

The MAX9737 features filterless, spread-spectrum modulation, externally set gain and a low-power shutdown mode that reduces supply current to less than 1µA. Comprehensive click-and-pop suppression and precharge circuitry reduce noise into and out of shutdown or mute within 10ms.

Spread-Spectrum Modulation

The MAX9737 features a unique spread-spectrum switching modulation that flattens EMI wideband spectral components, reducing radiated emissions from the speaker and cables. The switching frequency of the Class D amplifier varies randomly by ±4kHz around the 300kHz center frequency. Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is spread over a bandwidth that increases with frequency. Above a few MHz, the wideband spectrum looks like white noise for EMI purposes. A proprietary amplifier topology ensures this white noise does not corrupt the noise floor in the audio bandwidth.

Efficiency

The high efficiency of a Class D amplifier is due to the output transistors acting as switches and therefore consume negligible power. Power loss associated with the Class D output stage is due to the MOSFET I^2R losses, switching losses, and quiescent current.

Although the theoretical best efficiency of a linear amplifier is 78% at peak output power, under typical music reproduction levels, the efficiency falls to below 40%. The MAX9737 exhibits > 80% efficiency under the same conditions (Figure 1).

Shutdown

The MAX9737 features a shutdown mode that reduces power consumption to less than 1µA (typ), extending battery life in portable applications. Drive $\overline{SHDN}$ low to place the device in low-power shutdown mode. In shutdown mode, the outputs are high impedance and the common-mode voltage at the output decays to zero.

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Mono 7W Class D Amplifier

Mute Function

The MAX9737 features a mute mode where the signal is attenuated at the speaker and the outputs stop switching. To mute the MAX9737, drive $\overline{MUTE}$ low.

Click-and-Pop Suppression

The MAX9737 features comprehensive click-and-pop suppression and precharge circuitry that reduce audible transients on startup and shutdown. The precharge circuit enables the amplifier within 10ms without any clicks or pops. Connect PC between the input resistor (R_{IN}) and the input capacitor (C_{IN}). For optimal click-and-pop suppression, use a 0.47µF input coupling capacitor (C_{IN}).

Current Limit

When output current exceeds the current limit, 4.6A (typ), the MAX9737 disables the outputs and initiates a 450µs startup sequence. The shutdown and startup sequence is repeated until the output fault is removed. Properly designed applications do not enter current-limit mode unless the output is short circuited or connected incorrectly.

Thermal Shutdown

When the die temperature exceeds the thermal-shutdown threshold, +160°C (typ), the MAX9737 outputs are disabled. When the die temperature decreases by 30°C, normal operation resumes. Some causes of thermal shutdown are excessively low load impedance, poor thermal contact between the MAX9737's exposed pad and the PCB, elevated ambient temperature, or poor PCB layout and assembly.

Applications Information

Filterless Class D Operation

The MAX9737 meets EN55022B EMC radiation limits with an inexpensive ferrite bead and capacitor filter when the speaker leads are less than or equal to 1m (Figure 3). Select a ferrite bead with 100Ω to 600Ω impedance, and rated for 2A. The capacitor value varies based on the ferrite bead chosen and the speaker lead length. See Figure 2 for the correct connections of these components.

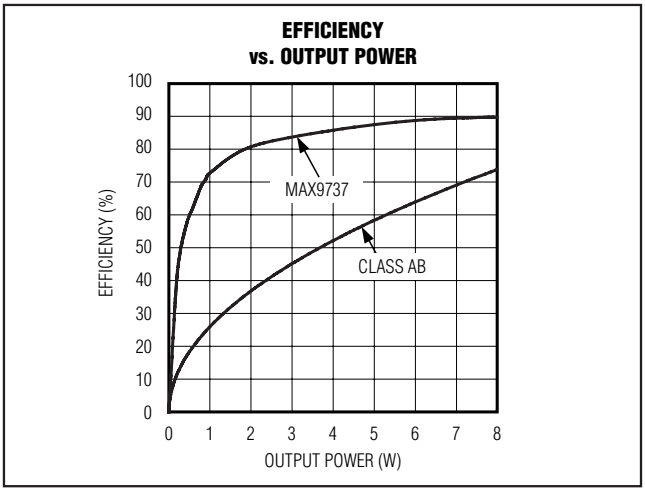

Figure 1. MAX9737 Efficiency vs. Class AB Efficiency

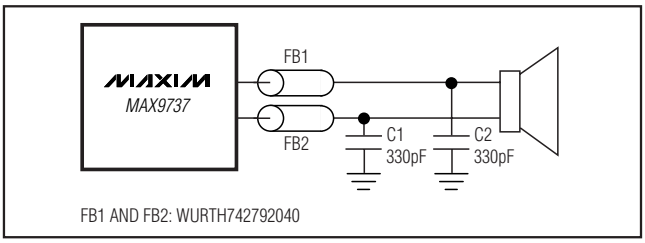

Figure 2. Ferrite Bead Filter Configuration

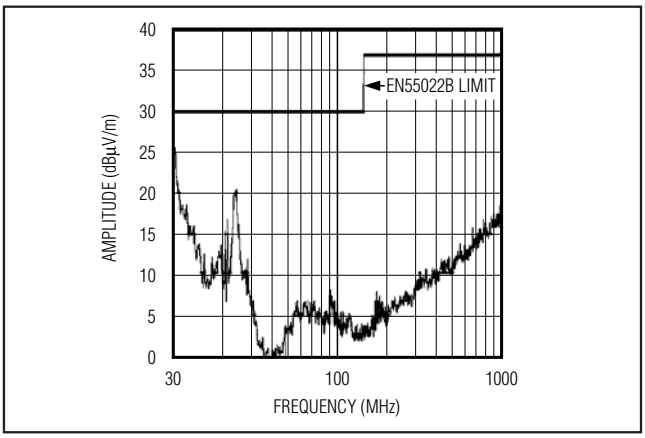

Figure 3. MAX9737 EMI Performance with 1m Twisted-Pair Speaker Cable

Table 1. Suggested Values for LC Filter

R_L (Ω)	L1, L2 (µH)	C1 (µF)	C2, C3 (µF)	C4, C5 (µF)	R1, R2 (Ω)
4	10	0.47	0.10	0.22	10
8	15	0.15	0.15	0.15	15

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When evaluating the MAX9737 with a ferrite bead filter and resistive load, include a series inductor (68µH for 8Ω load and 33µH for 4Ω load) to model typical loudspeaker's behavior. Omitting the series inductor reduces the efficiency, the THD+N performance and the output power of the MAX9737. When evaluating with a loudspeaker, no series inductor is required.

Inductor-Based Output Filters

Some applications use the MAX9737 with a full inductor/capacitor-based (LC) output filter. See Figure 4 for the correct connections of these components.

The load impedance of the speaker determines the filter component selection (see Table 1).

Inductors L1 and L2 and capacitor C1 form the primary output filter. Capacitors C2 and C3 provide common-mode filtering to reduce radiated emissions. Capacitors C4 and C5, plus resistors R1 and R2, form a Zobel at the output. A Zobel corrects the output loading to compensate for the rising impedance of the loudspeaker. Without a Zobel, the filter exhibits peaking near the cut-off frequency.

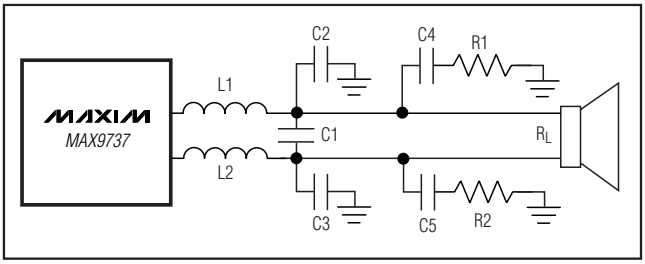

Figure 4. LC Filter Configuration

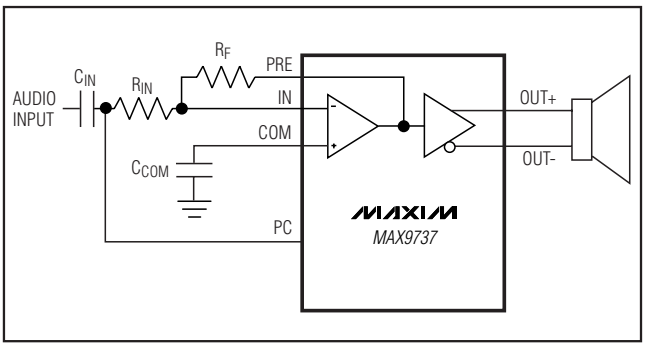

Figure 5. Preamplifier Gain Configuration

Component Selection

Gain-Setting Resistors

The output stage provides a fixed internal gain in addition to the externally set input stage gain. The fixed-output stage gain is set at 13.6dB (4.8V/V). Set overall gain by using resistors R_F and R_{IN} (Figure 5) as follows:

$$A_V = -4.8\left(\frac{R_F}{R_{IN}}\right) V/V$$

where A_V is the desired voltage gain. Choose R_F between 10kΩ and 50kΩ.

The PRE terminal is an operational amplifier output, allowing the MAX9737 to be configured as a filter or an equalizer.

Input Capacitor

An input capacitor, C_{IN}, in conjunction with the input resistor, R_{IN}, of the MAX9737 forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming negligible source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. To reduce low-frequency distortion, use capacitors whose dielectrics have low-voltage coefficients. Capacitors with high-voltage coefficients cause increased distortion close to f_{-3dB}. For best click-and-pop suppression, use a 0.47µF input capacitor.

COM Capacitor

COM is the output of the internally generated DC bias voltage. Bypass COM with a 1µF capacitor to AGND.

Regulator Capacitor

REG is the output of the internally generated DC bias voltage. Bypass REG with a 1µF capacitor to AGND.

Power Supplies

The MAX9737 features separate supplies for signal and power portions of the device, allowing for the optimum combination of headroom, power dissipation and noise immunity. The speaker amplifiers are powered from PVDD and can range from 8V to 28V. The remainder of the device is powered by an internal 5V regulator, V_S.

Internal Regulator

The MAX9737 features an internal 5V regulator, V_S, powered from PVDD. Bypass V_S with a 1µF capacitor to AGND.

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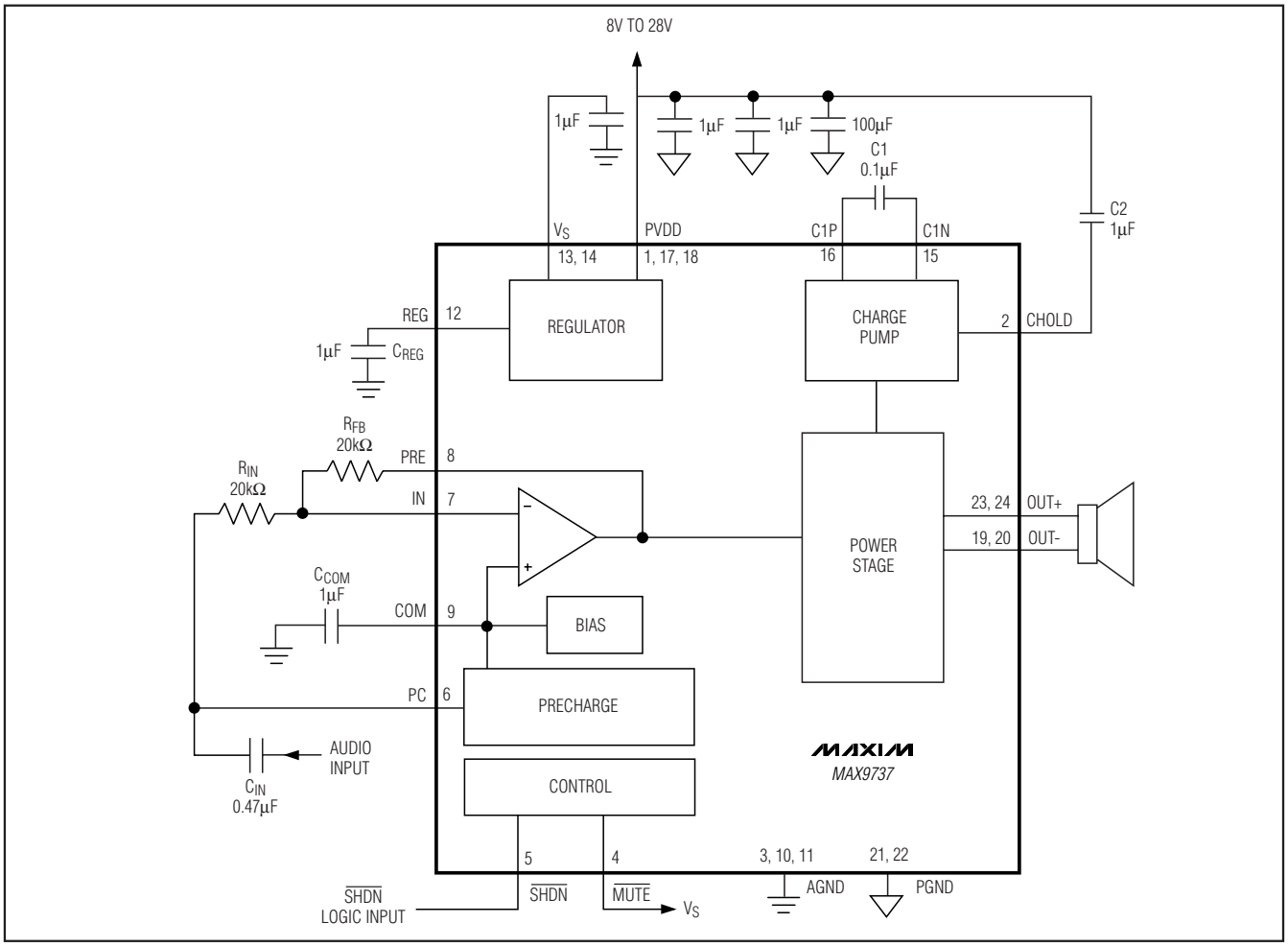
Mono 7W Class D Amplifier

Typical Application Circuit



Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. Use wide traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents switching noise from coupling into the audio signal. Connect PGND and AGND together at a single point on the PCB. Route all traces that carry switching transients away from AGND and the traces/components in the audio signal path.

Bypass PVDD with two 1µF capacitors to PGND. Place the bypass capacitors as close as possible to the MAX9737. Place a 100µF capacitor between PVDD and PGND. Bypass V_S, V_{COM}, and V_{REG} with a 1µF capacitor to AGND.

Use wide, low-resistance output traces. Current drawn from the outputs increases as load impedance decreases. High-output trace resistance decreases the power delivered to the load. The MAX9737 TQFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a heat conduction path from the die to the PCB. Connect the exposed thermal pad to PGND by using a large pad and multiple vias to the PGND plane.

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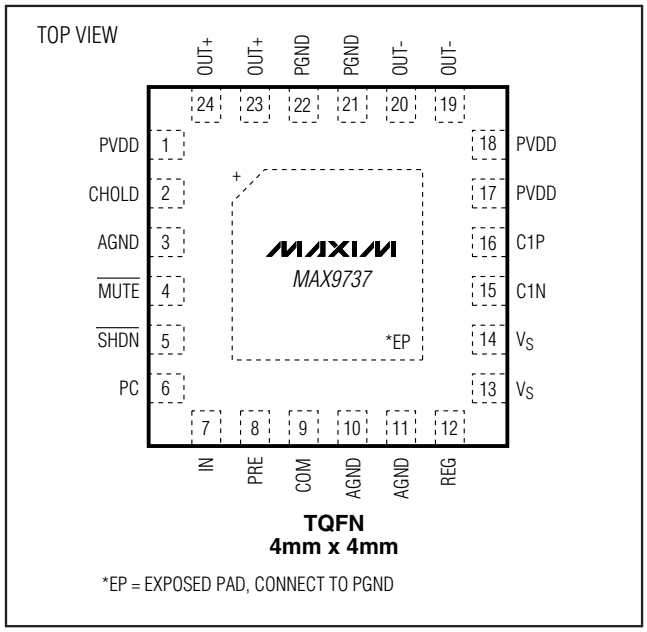
Pin Configuration



TQFN
4mm x 4mm

*EP = EXPOSED PAD, CONNECT TO PGND

Chip Information

PROCESS: BiCMOS

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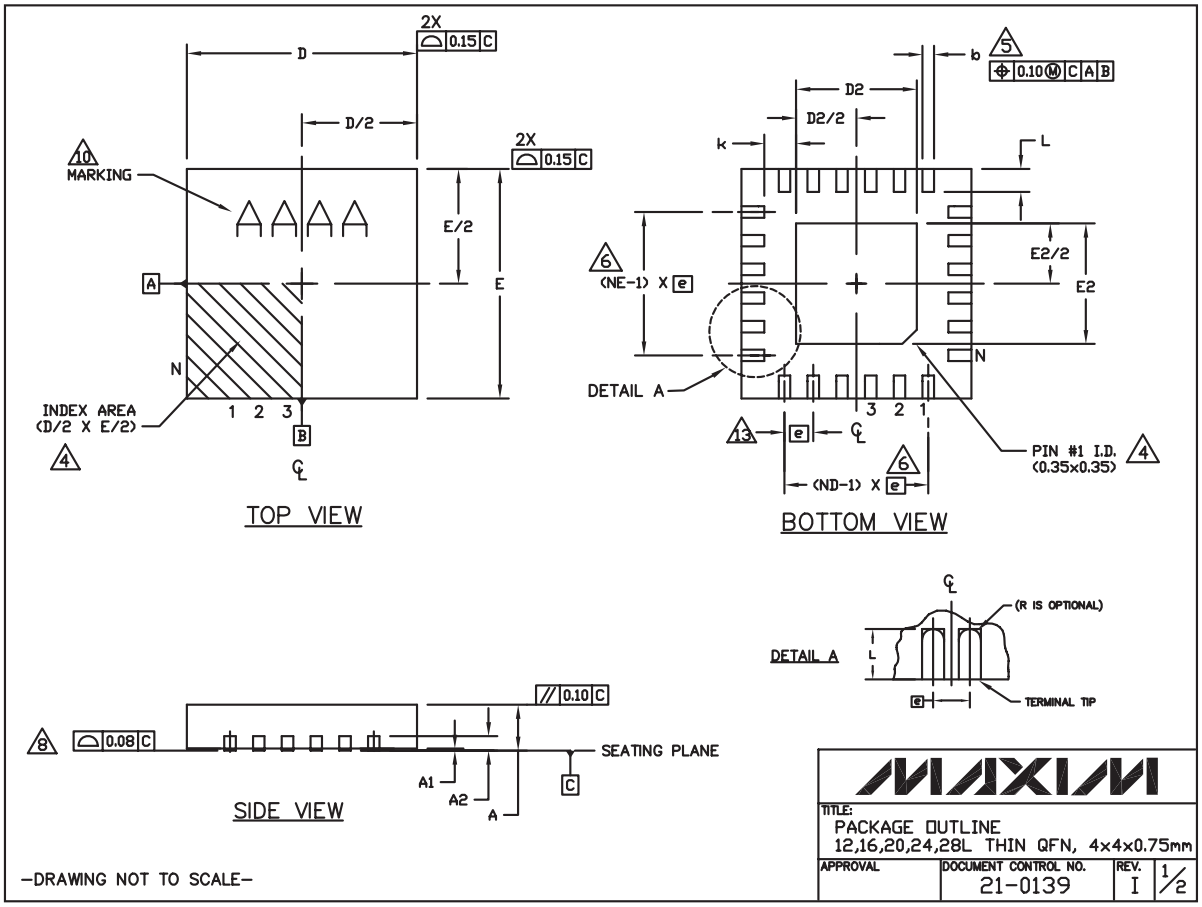
Mono 7W Class D Amplifier

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TQFN-EP	T2444+4	21-0139



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Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

COMMON DIMENSIONS																
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	12			16			20			24			28			
ND	3			4			5			6			7			
NE	3			4			5			6			7			
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE 12,16,20,24,28L THIN QFN, 4x4x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0139	REV. I	2/2

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