4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} .....-0.3V to 6.0V
- All Other Inputs.....-0.3V to (V_{CC} + 0.3V)

Input Current, V_{CC}, SRT.....20mA
Output Current, RESET or $\overline{RESET}$.....20mA

Continuous Power Dissipation (T_A = +70°C)
- SOT143-4 (derate 4mW/°C above +70°C).....320mW

Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full range, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Range		T_A = 0°C to +70°C		1.0		5.5	V
		T_A = -40°C to +85°C		1.2		5.5	
Supply Current	I_{CC}	MAX82_L/M/P, V_{CC} = 5.5V, I_{OUT} = 0	T_A = +25°C		2.5	7.0	µA
			T_A = T_{MIN} to T_{MAX}			12	
		MAX82_R/S/T/U, V_{CC} = 5.5V, I_{OUT} = 0	T_A = +25°C		1.8	5.5	
			T_A = T_{MIN} to T_{MAX}			9	
Reset Threshold (Note 1)	V_{TH}	MAX82_L	T_A = +25°C	4.56	4.63	4.70	V
			T_A = -40°C to +125°C	4.50		4.75	
		MAX82_M	T_A = +25°C	4.31	4.38	4.45	
			T_A = -40°C to +125°C	4.25		4.50	
		MAX82_P	T_A = +25°C	3.97	4.00	4.04	
			T_A = -40°C to +125°C	3.91		4.09	
		MAX82_T	T_A = +25°C	3.04	3.08	3.11	
			T_A = -40°C to +125°C	3.00		3.15	
		MAX82_S	T_A = +25°C	2.89	2.93	2.96	
			T_A = -40°C to +125°C	2.85		3.00	
		MAX82_U	T_A = +25°C	2.74	2.78	2.81	
			T_A = -40°C to +125°C	2.70		2.85	
		MAX82_R	T_A = +25°C	2.59	2.63	2.66	
			T_A = -40°C to +125°C	2.55		2.70	
Reset Threshold Tempco					30		ppm/°C
V_{CC} to Reset Delay (Note 1)		V_{CC} falling at 1mV/µs			50		µs
Reset Active Timeout Period	t_{RP}	SRT = GND		0.5	0.8	1	ms
		SRT = V_{CC}		20	32	40	
		SRT = unconnected		100	160	200	
SRT Input Current (Note 2)		$\overline{RESET}$ = low for MAX821, RESET = high for MAX822	SRT = GND	-100			µA
			SRT = V_{CC}			100	
			SRT = unconnected	-1		1	
SRT Input Threshold	V_{IL}	$\overline{RESET}$ = low for MAX821, RESET = high for MAX822				0.07V_{CC}	V
	V_{IH}			0.9V_{CC}			
	V_{OPEN}				0.5V_{CC}		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = full range, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

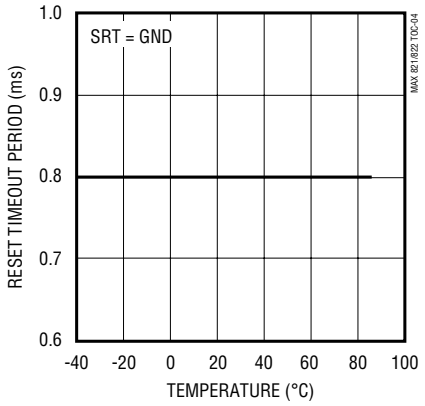
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SRT Input Capacitance (Note 3) (see *Setting the Reset Timeout Delay* section)		Internal			20	pF
$\overline{RESET}$ Output Voltage (MAX821)	V_{OL}	MAX821L/M/P only, I_{SINK} = 3.2mA, V_{CC} = $V_{TH(MIN)}$			0.4	V
		MAX821R/S/T/U only, I_{SINK} = 1.2mA, V_{CC} = $V_{TH(MIN)}$			0.3	
		I_{SINK} = 50µA, T_A = 0°C to +70°C, V_{CC} ≥ 1V			0.3	
		I_{SINK} = 50µA, T_A = -40°C to +85°C, V_{CC} ≥ 1.2V			0.3	
	V_{OH}	MAX821L/M/P only, I_{SOURCE} = 800µA, V_{CC} ≥ $V_{TH(MAX)}$	V_{CC} -1.5			
		MAX821R/S/T/U only, I_{SOURCE} = 500µA, V_{CC} ≥ $V_{TH(MAX)}$	0.8V_{CC}			
RESET Output Voltage (MAX822)	V_{OL}	MAX822L/M only, I_{SINK} = 3.2mA, V_{CC} = $V_{TH(MAX)}$			0.4	V
		MAX822R/S/T only, I_{SINK} = 1.2mA, V_{CC} = $V_{TH(MAX)}$			0.3	
	V_{OH}	I_{SOURCE} = 150µA, 1.4V ≤ V_{CC} ≤ $V_{TH(MIN)}$	0.8V_{CC}			

Note 1: $\overline{RESET}$ output for MAX821; RESET output for MAX822.
Note 2: During reset active timeout period only.
Note 3: Guaranteed by design.

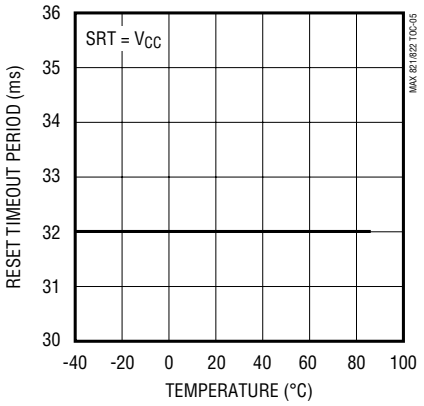
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

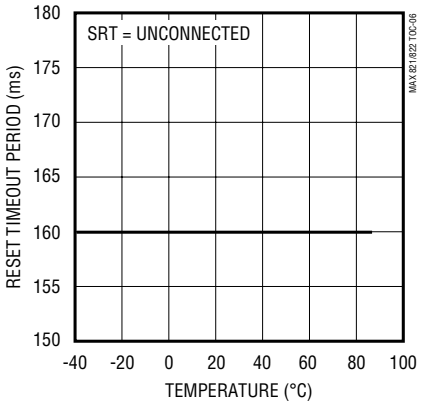
RESET TIMEOUT PERIOD vs. TEMPERATURE



RESET TIMEOUT PERIOD vs. TEMPERATURE



RESET TIMEOUT PERIOD vs. TEMPERATURE

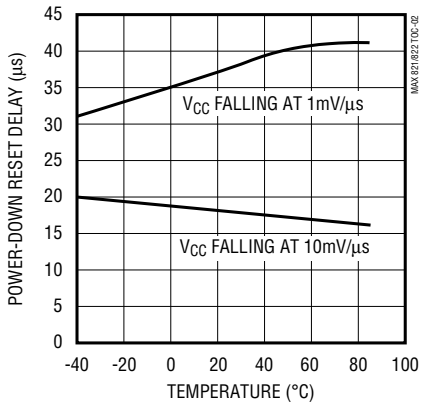


4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

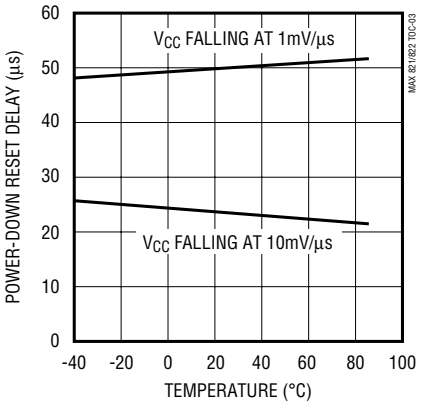
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

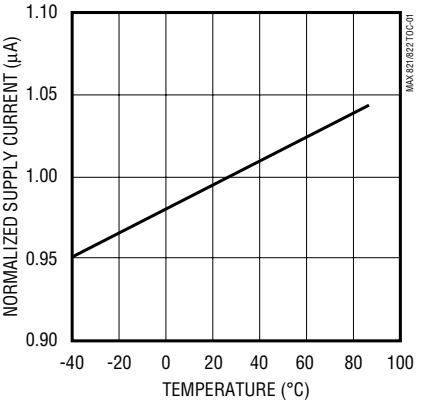
MAX82_R/S/T POWER-DOWN RESET DELAY vs. TEMPERATURE



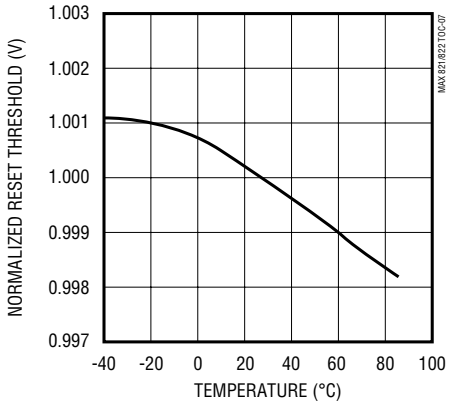
MAX82_L/M POWER-DOWN RESET DELAY vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED RESET THRESHOLD vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX821	MAX822		
1	1	GND	Ground
2	–	$\overline{\text{RESET}}$	Active-Low Reset Output. $\overline{\text{RESET}}$ is low while V_{CC} is below the reset threshold. It remains low for the reset timeout period after the reset condition is terminated. The reset timeout period is determined by the SRT input.
–	2	RESET	Active-High Reset Output. RESET is high while V_{CC} is below the reset threshold. It remains high for the reset timeout period after the reset condition is terminated. The reset timeout period is determined by the SRT input.
3	3	SRT	Set Reset Timeout Input. Connect to GND for 1ms (max) delay; connect to V_{CC} for 20ms (min) delay; leave unconnected for 100ms (min) delay.
4	4	V_{CC}	Supply Voltage

4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. These µP supervisory circuits assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They also provide a reset timeout delay that is pin programmable to 1ms (max), 20ms (min), or 100ms (min). This feature allows flexibility in designing bar-code scanners, hand-held devices, and other applications that require quick or nonstandard power-up times.

The MAX821's $\overline{RESET}$ output is guaranteed to be a logic low for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the reset timeout period, as determined by the Set Reset Timeout (SRT) input. See the *Setting the Reset Timeout Delay* section.

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{RESET}$ goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{RESET}$ goes low. The internal timer begins counting after V_{CC} returns above the reset threshold, and $\overline{RESET}$ remains low for the reset timeout period.

The MAX822 has an active-high RESET output that is the inverse of the MAX821's $\overline{RESET}$ output.

Setting the Reset Timeout Delay

Use the three-level Set Reset Timeout (SRT) input to set the reset timeout delay. Connect SRT to GND for a 1ms (max) delay; connect it to V_{CC} for a 20ms (min) delay; or leave it unconnected for a 100ms (min) delay.

If you choose to drive the SRT pin with an external signal, make sure the signal source can charge/discharge the capacitance on SRT quickly enough (<500µs) to avert an unintended reset timeout delay.

To ensure proper operation when selecting the 100ms timeout (SRT = unconnected), minimize capacitive loading on the SRT pin (< 200pF). Excessive capacitive loading can select an unintended faster timeout mode.

Reset Threshold Accuracy

The MAX821/MAX822 are designed to meet their worst-case specifications over their entire operating temperature range. Choose a reset threshold guaranteed to assert at a voltage below the power supply's regulation range and above the minimum specified operating voltage range for the system's ICs.

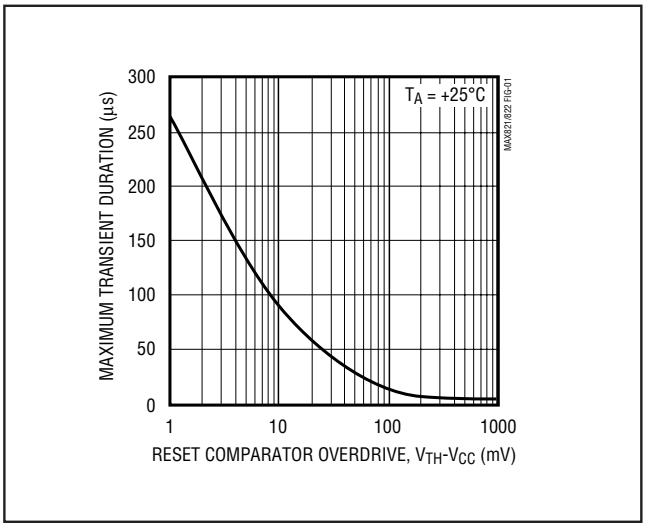


Figure 1. Maximum Transient Duration Without Causing a Reset Pulse vs. Comparator Overdrive

Applications Information

Negative-Going V_{CC} Transients

While designed to issue a reset to the microprocessor (µP) during power-up, power-down, and brownout conditions, the MAX821/MAX822 are relatively immune to short-duration, negative-going V_{CC} transients (glitches).

Figure 1 shows the maximum transient duration vs. reset comparator overdrive for which the MAX821/MAX822 typically do not generate a reset pulse. This graph was generated using a negative-going pulse applied to V_{CC}, starting above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going V_{CC} transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, for the MAX821/MAX822, a V_{CC} transient that goes 100mV below the reset threshold and lasts 12µs or less will not cause a reset pulse to be issued. A 0.1µF capacitor mounted as close as possible to V_{CC} can provide additional transient immunity, if desired.

4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the MAX821 $\overline{RESET}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to the $\overline{RESET}$ output can drift to undetermined voltages. This presents no problem in most applications, since most µP and other circuitry is inoperative with V_{CC} below 1V. However, in applications where the $\overline{RESET}$ output must be valid down to 0V, adding a pull-down resistor to the $\overline{RESET}$ pin will cause any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (Figure 2a). R1's value is not critical; 100kΩ is large enough not to load $\overline{RESET}$, and small enough to pull $\overline{RESET}$ to ground.

A 100kΩ pull-up resistor to V_{CC} is also recommended for the MAX822 if RESET is required to remain valid for V_{CC} < 1V (Figure 2b).

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins (such as the Motorola 68HC11 series) can contend with the MAX821 reset output. For example, if the MAX821 $\overline{RESET}$ output is asserted high and the µP wants to pull it low, indeterminate logic levels may result. To correct such cases, connect a 4.7kΩ resistor between the MAX821 $\overline{RESET}$ output and the µP reset I/O (Figure 3). Buffer the reset output to other system components.

Chip Information

TRANSISTOR COUNT: 492

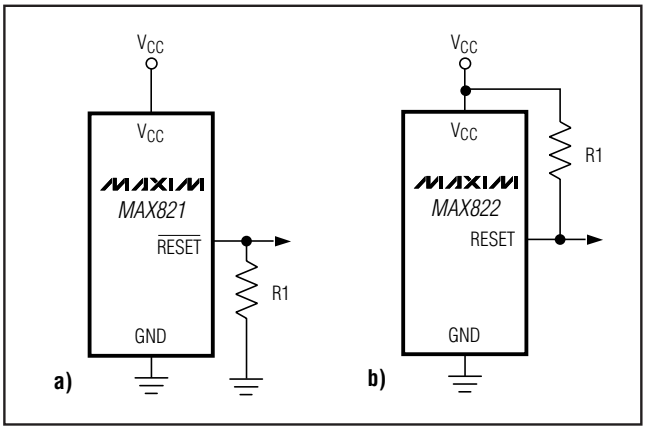


Figure 2. $\overline{RESET}$/RESET Valid to V_{CC} = Ground Circuit

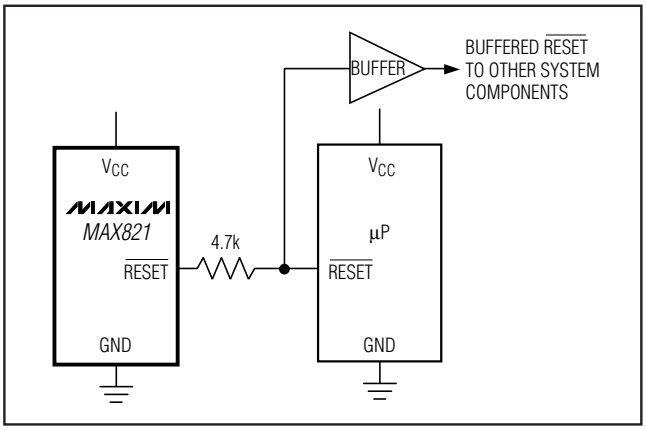


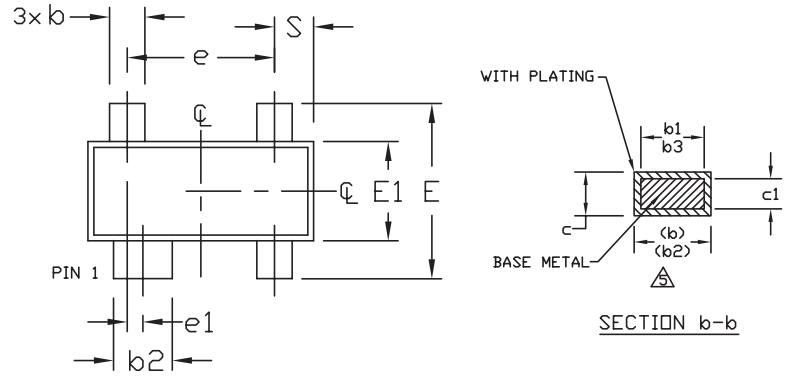
Figure 3. Interfacing to µPs with Bidirectional Reset I/O

4-Pin µP Voltage Monitors with Pin-Selectable Power-On Reset Timeout Delay

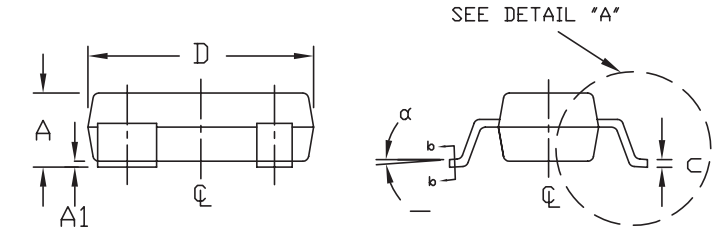
Package Information

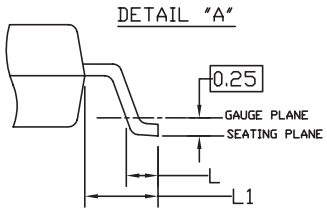
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOT-143 4L.EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.048	0.80	1.22
A1	0.000	0.006	0.01	0.15
b	0.014	0.020	0.35	0.50
b1	0.012	0.018	0.30	0.45
b2	0.030	0.035	0.76	0.89
b3	0.012	0.033	0.76	0.84
c	0.003	0.008	0.08	0.20
c1	0.003	0.006	0.08	0.16
D	0.110	0.120	2.80	3.04
E	0.083	0.104	2.10	2.64
E1	0.047	0.055	1.20	1.40
e	0.076 BSC.		1.92 BSC.	
e1	0.008 BSC.		0.20 BSC.	
L	0.016	0.024	0.40	0.60
L1	0.021 REF.		0.54 REF.	
S	0.018	0.024	0.45	0.60
α	0°	8°	0°	8°





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC TO253.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08mm AND 0.15mm FROM THE LEAD TIP.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-143, 4L

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0052	E	1/1