

Absolute Maximum Ratings

(All voltages referenced to GND.)

Supply Voltage V+	-0.3V to +6V
SCL, SDA, AD0, AD2, $\overline{\text{RST}}$, $\overline{\text{INT}}$, P2–P5	-0.3V to +6V
O0, O1, O6, O7	-0.3 to (V+ + 0.3V)
O0, O1, O6, O7 Output Current	±25mA
P2–P5 Sink Current	±25mA
SDA Sink Current	10mA
INT Sink Current	10mA
Total V+ Current	50mA

Total GND Current	100mA
Continuous Power Dissipation (T _A = +70°C)	
16-Pin QSOP (derate 8.3mW/°C above +70°C)	667mW
16-Pin TQFN (derate 15.6mW/°C above +70°C)	1250mW
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		1.71		5.50	V
Power-On Reset Voltage	V _{POR}	V+ falling			1.6	V
Standby Current (Interface Idle)	I _{STB}	SCL and SDA and other digital inputs at V+		0.6	1.5	μA
Supply Current (Interface Running)	I+	f _{SCL} = 400kHz; other digital inputs at V+		23	55	μA
Input High Voltage SDA, SCL, AD0, AD2, $\overline{\text{RST}}$, P2–P5	V _{IH}	V+ ≤ 1.8V	0.8 x V+			V
		V+ ≥ 1.8	0.7 x V+			
Input Low Voltage SDA, SCL, AD0, AD2, $\overline{\text{RST}}$, P2–P5	V _{IL}	V+ ≤ 1.8V			0.2 x V+	V
		V+ ≥ 1.8V			0.3 x V+	
Input Leakage Current SDA, SCL, AD0, AD2, $\overline{\text{RST}}$, P2–P5	I _{IH} , I _{IL}	SDA, SCL, AD0, AD2, $\overline{\text{RST}}$, P2–P5 at V+ or GND, internal pullup disabled	-0.2		+0.2	μA
Input Capacitance SDA, SCL, AD0, AD2, $\overline{\text{RST}}$, P2–P5				10		pF
Output Low Voltage O0, O1, O6, O7, P2–P5	V _{OL}	V+ = +1.71V, I _{SINK} = 5mA		105	180	mV
		V+ = +2.5V, I _{SINK} = 10mA		131	240	
		V+ = +3.3V, I _{SINK} = 15mA		154	290	
		V+ = +5V, I _{SINK} = 20mA		160	310	
Output High Voltage O0, O1, O6, O7	V _{OH}	V+ = +1.71V, I _{SOURCE} = 2mA	V+ - 250	V+ - 30		mV
		V+ = +2.5V, I _{SOURCE} = 5mA	V+ - 360	V+ - 70		
		V+ = +3.3V, I _{SOURCE} = 5mA	V+ - 260	V+ - 100		
		V+ = +5V, I _{SOURCE} = 10mA	V+ - 350	V+ - 120		
Output Low Voltage SDA	V _{OLSDA}	I _{SINK} = 6mA			250	mV
Output Low Voltage INT	V _{OLINT}	I _{SINK} = 5mA		130	250	mV
Port Input Pullup Resistor	R _{PU}		25	40	55	kΩ

Port and Interrupt $\overline{\text{INT}}$ Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Output Data Valid	t _{PPV}	C _L ≤ 100pF			4	μs
Port Input Setup Time	t _{PSU}	C _L ≤ 100pF	0			μs
Port Input Hold Time	t _{PH}	C _L ≤ 100pF	4			μs
$\overline{\text{INT}}$ Input Data Valid Time	t _{IV}	C _L ≤ 100pF			4	μs
$\overline{\text{INT}}$ Reset Delay Time from STOP	t _{IP}	C _L ≤ 100pF			4	μs
$\overline{\text{INT}}$ Reset Delay Time from Acknowledge	t _{IR}	C _L ≤ 100pF			4	μs

Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f _{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t _{BUF}		1.3			μs
Hold Time (Repeated) START Condition	t _{HD, STA}		0.6			μs
Repeated START Condition Setup Time	t _{SU, STA}		0.6			μs
STOP Condition Setup Time	t _{SU, STO}		0.6			μs
Data Hold Time	t _{HD, DAT}	(Note 2)			0.9	μs
Data Setup Time	t _{SU, DAT}		100			ns
SCL Clock Low Period	t _{LOW}		1.3			μs
SCL Clock High Period	t _{HIGH}		0.7			μs
Rise Time of Both SDA and SCL Signals, Receiving	t _R	(Notes 3, 4)		20 + 0.1C _b	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t _F	(Notes 3, 4)		20 + 0.1C _b	300	ns
Fall Time of SDA, Transmitting	t _{F, TX}	(Notes 3, 4)		20 + 0.1C _b	250	ns
Pulse Width of Spike Suppressed	t _{SP}	(Note 5)		50		ns
Capacitive Load for Each Bus Line	C _b	(Note 3)			400	pF
RST Pulse Width	t _W		500			ns
RST Rising to START Condition Setup Time	t _{RST}		1			μs

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

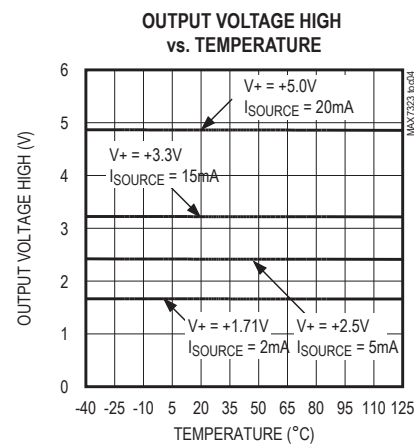
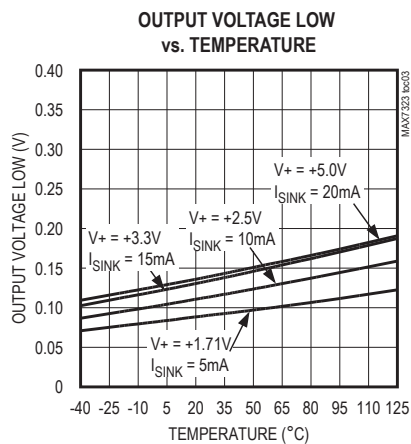
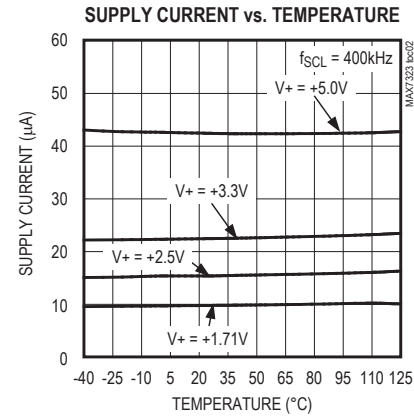
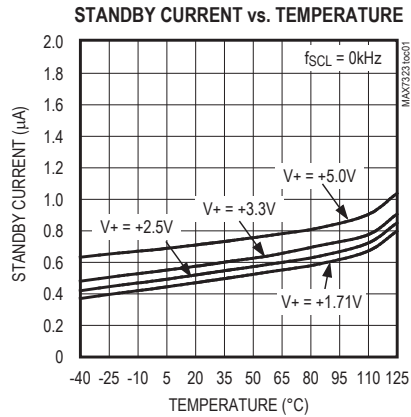
Note 3: Guaranteed by design.

Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 x V+ and 0.7 x V+ with I_{SINK} ≤ 6mA.

Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1, 3	15, 1	AD0, AD2	Address Inputs. Select device slave address with AD0 and AD2. Connect AD0 and AD2 to either GND, V ₊ , SCL, or SDA to give four logic combinations (see Table 3).
2	16	RST	Reset Input, Active Low. Drive RST low to clear the 2-wire interface.
4, 5, 11, 12	2, 3, 9, 10	O0, O1, O6, O7	Output Ports. O0, O1, O6, and O7 are push-pull outputs.
6, 7, 9, 10	4, 5, 7, 8	P2–P5	I/O Ports. P2 to P5 are open-drain I/Os rated to +6V, 20mA.
8	6	GND	Ground
13	11	INT	Interrupt Output. INT is an open-drain output.
14	12	SCL	I ² C-Compatible Serial Clock Input
15	13	SDA	I ² C-Compatible Serial Data I/O
16	14	V ₊	Positive Supply Voltage. Bypass V ₊ to GND with a ceramic capacitor of at least 0.047µF as close to the device as possible.
—	EP	EP	Exposed Pad. Connect exposed pad to GND.

MAX7323

I²C Port Expander with 4 Push-Pull Outputs and 4 Open-Drain I/Os

Detailed Description

MAX7319–MAX7329 Family Comparison

The MAX7319–MAX7323 family consists of five pin-compatible, eight-port expanders. Each version is optimized for different applications. The MAX7328 and MAX7329 are industry-standard parts.

The MAX7324–MAX7327 family consists of four pin-compatible, 16-port expanders that integrate the functions of the MAX7320 and one of either the MAX7319, MAX7321, MAX7322, or MAX7323.

Functional Overview

The MAX7323 is a general-purpose port expander, operating from a +1.71V to +5.5V supply, that provides four push-pull output ports with 20mA sink, 10mA source drive capability, and four open-drain I/O ports with a 20mA sink capability. The four open-drain outputs are overvoltage protected to +6V independent of supply voltage.

The MAX7323 is set to one of 16 I²C slave addresses (0x60 to 0x6F) using the address select inputs AD0 and AD2, and is accessed over an I²C serial interface up to 400kHz. The $\overline{\text{RST}}$ input clears the serial interface in case of a bus lockup, terminating any serial transaction to or from the MAX7323.

Table 1. MAX7319–MAX7329 Family Comparison

PART	I ² C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	APPLICATION
8-PORT EXPANDERS						
MAX7319	110xxxx	8	Yes	—	—	Input-only versions: 8 input ports with programmable latching transition detection interrupt and selectable pullups. Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7320	101xxxx	—	—	—	8	Output-only versions: 8 push-pull outputs with selectable power-up default levels. Push-pull outputs offer faster rise time than open-drain outputs, and require no pullup resistors.
MAX7321	110xxxx	Up to 8	—	Up to 8	—	I/O versions: 8 open-drain I/O ports with latching transition detection interrupt and selectable pullups. Open-drain outputs can level shift the logic-high State to a higher or lower voltage than V+ using external pullup resistors. Any port can be used as an input by setting the open-drain output to logic-high. Transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7322	110xxxx	4	Yes	—	4	4 input-only, 4 output-only versions: 4 input ports with programmable latching transition detection interrupt and selectable pullups; 4 push-pull outputs with selectable power-up default levels.

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I ² C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN- DRAIN OUTPUTS	PUSH- PULL OUTPUTS	APPLICATION
MAX7323	110xxxx	Up to 4	—	Up to 4	4	4 I/O, 4 output-only versions: 4 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 4 push-pull outputs with selectable power-up default levels.
MAX7328 MAX7329	0100xxx 0111xxx	Up to 8	—	Up to 8	—	8 open-drain I/O ports with nonlatching transition detection interrupt and pullups on all ports. All ports power up as inputs (or logic-high outputs). Any port can be used as an input by setting the open-drain output to logic-high.
16-PORT EXPANDERS						
MAX7324	101xxxx and 110xxxx	8	Yes	—	8	Software equivalent to a MAX7320 plus a MAX7319.
MAX7325		Up to 8	—	Up to 8	8	Software equivalent to a MAX7320 plus a MAX7321.
MAX7326		4	Yes	—	12	Software equivalent to a MAX7320 plus a MAX7322.
MAX7327		Up to 4	—	Up to 4	12	Software equivalent to a MAX7320 plus a MAX7323.

Any of the four open-drain ports can be configured as a logic input by setting the port output logic-high (logic-high for an open-drain output is high impedance). When the MAX7323 is read through the serial interface, the actual logic levels at the ports are read back.

The four ports offer latching transition detection functionality. All input ports are continuously monitored for changes. An input change sets 1 of 4 flag bits that identify changed input(s). All flags are cleared upon a subsequent read or write transaction to the MAX7323.

A latching interrupt output, $\overline{\text{INT}}$, automatically flags data changes on any of the I/O ports used as inputs. The interrupt output $\overline{\text{INT}}$, and all transition flags are deasserted when the MAX7323 is next accessed through the serial interface.

Internal pullup resistors to V₊ are selected by the address select inputs, AD0 and AD2. Pullups are enabled on the input ports in groups of two (see Table 3).

Use the slave address selection to ensure that I/O ports used as inputs are logic-high on power-up. I/O ports with internal pullups enabled default to a logic-high output state. I/O ports with internal pullups disabled default to a logic-low output state. Output port power-up logic states are selected by the address select inputs AD0 and AD2. Ports default to logic-high or logic-low on power-up in groups of two (see Table 3).

Initial Power-Up

On power-up, the transition detection logic is reset, and $\overline{\text{INT}}$ is deasserted. The interrupt mask register is set to 0x3C, enabling the interrupt output for transitions on all four input ports. The transition flags are cleared to indicate no data changes. The power-up default state of the four push-pull outputs is set according to the I²C slave address selection inputs, AD0 and AD2 (see Table 3).

Power-On Reset

The MAX7323 contains an integral power-on-reset (POR) circuit that ensures all registers are reset to a known state on power-up. When V₊ rises above V_{POR} (1.6V max), the POR circuit releases the registers and 2-wire interface for normal operation. When V₊ drops to less than V_{POR}, the MAX7323 resets all ports to the POR defaults (see Table 3).

$\overline{\text{RST}}$ Input

The active-low $\overline{\text{RST}}$ input operates as a reset that voids any current I²C transaction involving the MAX7323, forcing the MAX7323 into the I²C STOP condition. The reset action does not clear the interrupt output ($\overline{\text{INT}}$).

Standby Mode

When the serial interface is idle, the MAX7323 automatically enters standby mode, drawing minimal supply current.

Table 2. Read and Write Access to Eight-Port Expander Family

PART	I ² C SLAVE ADDRESS	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	I ² C DATA WRITE	I ² C DATA READ
MAX7319	110xxxx	8	Yes	—	—	<I7–I0 interrupt mask>	<I7–I0 port inputs> <I7–I0 transition flags>
MAX7320	101xxxx	—	—	—	8	<O7–O0 port outputs>	<O7–O0 port inputs>
MAX7321	110xxxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs> <P7–P0 transition flags>
MAX7322	110xxxx	4	Yes	—	4	<O7, O6 outputs, I5–I2 interrupt mask, O1, O0 outputs>	<O7, O6, I5–I2, O1, O0 port inputs> <O, 0, I5–I2 transition flags, 0, 0>
MAX7323	110xxxx	Up to 4	—	Up to 4	4	<port outputs>	<O7, O6, P5–P2, O1, O0 port inputs> <O, 0, P5–P2 transition flags, 0, 0>
MAX7328	0100xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>
MAX7329	0111xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>

Slave Address and Input Pullup Selection

Address inputs AD0 and AD2 determine the MAX7323 slave address, select which inputs have pullup resistors, and set the default logic state on outputs. Pullups are enabled on the input ports in groups of two (see Table 3). The MAX7319, MAX7321, MAX7322, and MAX7323 use a different range of slave addresses (110xxxx) than the MAX7320 (101xxxx).

The MAX7323 slave address is determined on each I²C transmission, regardless of whether the transmission is actually addressing the MAX7323. The MAX7323 distinguishes whether address inputs AD2 and AD0 are connected to SDA or SCL instead of fixed logic levels V+ or GND during this transmission. Therefore, the MAX7323 slave address can be configured dynamically in the application without cycling the device supply.

On initial power-up, the MAX7323 cannot decode address inputs AD2 and AD0 fully until the first I²C transmission. AD0 and AD2 initially appear to be connected to V+ or GND. This is important because the address selection determines the power-up default states of the output ports and I/O port initial logic state, and whether pullups are enabled. However, at power-up, the I²C SDA and SCL bus interface lines are high impedance at the pins of every device (master or slave)

connected to the bus, including the MAX7323. This is guaranteed as part of the I²C specification. Therefore, address inputs AD2 and AD0 that are connected to SDA or SCL normally appear at power-up to be connected to V+. The pullup selection logic uses AD0 to select whether pullups are enabled for ports P2 and P3, and to set the initial logic state for O0 and O1. AD2 selects whether pullups are enabled for ports P4 and P5 and sets the initial logic state for O6 and O7. The rule is that a logic-high, SDA, or SCL connection selects the pullups and sets the default logic state to high. A logic-low deselects the pullups and sets the default logic state low (see Table 3). The port configuration is correct on power-up for a standard I²C configuration, where SDA or SCL are pulled up to V+ by the external I²C pullup resistors.

There are circumstances where the assumption that SDA = SCL = V+ on power-up is not true—for example, in applications in which there is legitimate bus activity during power-up. Also, if SDA and SCL are terminated with pullup resistors to a different supply voltage than the MAX7323's supply voltage, and if that pullup supply rises later than the MAX7323's supply, then SDA or SCL may appear at power-up to be connected to GND. In such applications, use the four address combinations that are selected by connecting address inputs AD2

Table 3. MAX7323 Address Map

PIN CONNECTION		DEVICE ADDRESS								OUTPUTS POWER-UP DEFAULT								40kΩ INPUT PULLUPS ENABLED							
AD2	AD0	A6	A5	A4	A3	A2	A1	A0	O7	O6	P5	P4	P3	P2	O1	O0	O7	O6	P5	P4	P3	P2	O1	O0	
SCL	GND	1	1	0	0	0	0	0	1	1	1	1	0	0	0	0	Pullups are not enabled for push-pull outputs.		Y	Y	—	—	Pullups are not enabled for push-pull outputs.		
SCL	V+	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y			
SCL	SCL	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1			Y	Y	Y	Y			
SCL	SDA	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y			
SDA	GND	1	1	0	0	1	0	0	1	1	1	1	0	0	0	0			Y	Y	—	—			
SDA	V+	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y			
SDA	SCL	1	1	0	0	1	1	0	1	1	1	1	1	1	1	1			Y	Y	Y	Y			
SDA	SDA	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y			
GND	GND	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0			—	—	—	—			
GND	V+	1	1	0	1	0	0	1	0	0	0	0	1	1	1	1			—	—	Y	Y			
GND	SCL	1	1	0	1	0	1	0	0	0	0	0	1	1	1	1			—	—	Y	Y			
GND	SDA	1	1	0	1	0	1	1	0	0	0	0	1	1	1	1			—	—	Y	Y			
V+	GND	1	1	0	1	1	0	0	1	1	1	1	0	0	0	0			Y	Y	—	—			
V+	V+	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y			
V+	SCL	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1			Y	Y	Y	Y			
V+	SDA	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y			

and AD0 to V+ or GND (shown in **bold** in Table 3). These selections are guaranteed to be correct at power-up, independent of SDA and SCL behavior. If one of the other 12 address combinations is used, an unexpected combination of pullups might be asserted until the first I²C transmission (to any device, not necessarily the MAX7323) is put on the bus.

I/O Port Inputs

I/O port inputs switch at the CMOS logic levels as determined by the expander's supply voltage, and are overvoltage tolerant to +6V, independent of the expander's supply voltage.

I/O Port Input Transition Detection

All four I/O ports configured as inputs are monitored for changes since the expander was last accessed through the serial interface. The state of the I/O ports is stored in an internal "snapshot" register for transition monitoring. The snapshot is continuously compared with the actual input conditions, and if a change is detected for any port input, $\overline{\text{INT}}$ is asserted to signal a state change. An internal transition flag is set for that port. The input ports are sampled (internally latched into the snapshot register) and the old transition flags cleared during the I²C acknowledge of every MAX7323 read and write access. The previous port transition

flags are read through the serial interface as the second byte of a 2-byte read sequence.

A long read sequence (more than 2 bytes) can be used to poll the expander continuously without the overhead of resending the slave address. If more than 2 bytes are read from the expander, the expander repeatedly returns the input port data, alternating with the transition flags. The inputs are repeatedly resampled and the transition flags repeatedly reset for each pair of bytes read. All changes that occur during a long read sequence are detected and reported.

The $\overline{\text{INT}}$ output is not reasserted during a read sequence to avoid recursive reentry into an interrupt service routine. Instead, if a data change occurs that would normally cause the $\overline{\text{INT}}$ output to be set, the $\overline{\text{INT}}$ assertion is delayed until the STOP condition. $\overline{\text{INT}}$ is not reasserted upon a STOP condition if the changed input data is read before the STOP occurs. The $\overline{\text{INT}}$ logic ensures that unnecessary interrupts are not asserted, yet data changes are detected and reported no matter when the change occurs.

Port Outputs

Write 1 byte to the MAX7323 to set the output port levels for the four push-pull outputs, and the four open-drain I/O ports simultaneously.

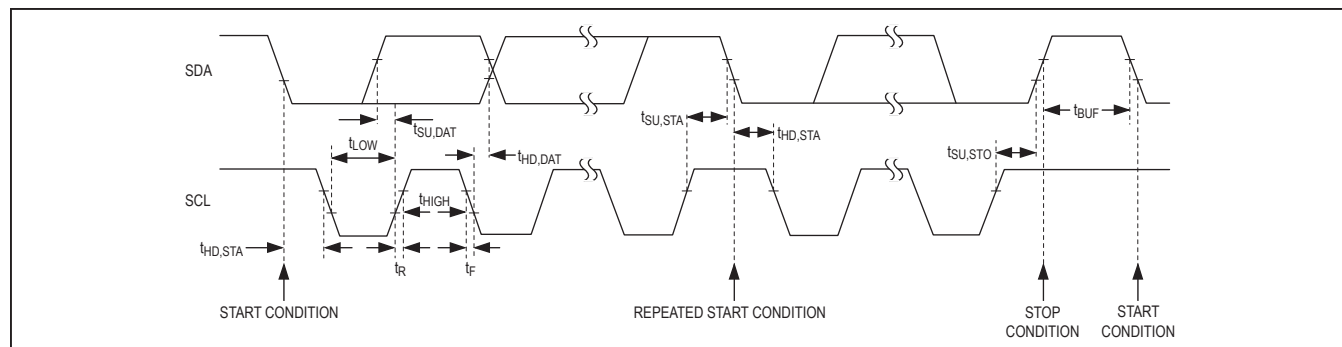


Figure 1. 2-Wire Serial Interface Timing Details

Serial Interface

Serial Addressing

The MAX7323 operates as a slave that sends and receives data through an I²C interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). The master initiates all data transfers to and from the MAX7323 and generates the SCL clock that synchronizes the data transfer (Figure 1).

SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7k Ω , is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7k Ω , is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition sent by a master, followed by the MAX7323's 7-bit slave address plus R/W bit, 1 or more data bytes, and finally a STOP condition (Figure 2).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 2).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 3).

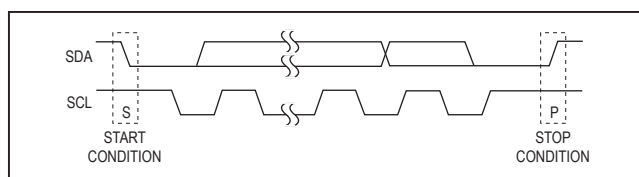


Figure 2. START and STOP Conditions

Acknowledge

The acknowledge bit is a clocked 9th bit the recipient uses to acknowledge receipt of each byte of data (Figure 4). Each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7323, the device generates the acknowledge bit because the MAX7323 is the recipient. When the MAX7323 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7323 has a 7-bit-long slave address (Figure 5). The 8th bit following the 7-bit slave address is the R/W bit. It is low for a write command, and high for a read command.

The first (A6), second (A5), and third (A4) bits of the MAX7323 slave address are always 1, 1, and 0. Connect AD2 and AD0 to GND, V+, SDA, or SCL to select slave address bits A3, A2, A1, and A0. The MAX7323 has 16 possible slave addresses (Table 3), allowing up to 16 MAX7323 devices on an I²C bus.

Accessing the MAX7323

The MAX7323 is accessed through an I²C interface. The transition flags are cleared, and $\overline{\text{INT}}$ is deasserted each time the device acknowledges the I²C slave address.

A **single-byte read** from the MAX7323 returns the status of the four I/O ports and the four output ports (read back as inputs).

A **2-byte read** returns first the status of the four I/O ports and the four output ports (as for a single-byte read), followed by the four transition flags for the four I/O ports.

A **multibyte read** (more than 2 bytes before the I²C STOP bit) repeatedly returns the port data, alternating with the transition flags. As the input data is resampled for each transmission, and the transition flags are reset each time, a multibyte read continuously returns the current data and identifies any changing I/O ports.

If a port data change occurs during the read sequence, $\overline{\text{INT}}$ is reasserted after the I²C STOP bit. The MAX7323 does not generate another interrupt during a single-byte or multibyte read.

Port data is sampled during the preceding I²C acknowledge bit (the acknowledge bit for the I²C slave address in the case of a single-byte or 2-byte read).

A **single-byte write** to the MAX7323 sets the logic state of the four open-drain I/O ports and four push-pull outputs.

In a **2-byte write** to the MAX7323, the first byte sets the logic state of the four open-drain I/O ports and four push-pull outputs, while the second byte sets the interrupt mask bits for the four open-drain I/O ports.

Reading from the MAX7323

A read from the MAX7323 starts with the master transmitting the MAX7323's slave address with the R/W bit set high. The MAX7323 acknowledges the slave address, and samples the ports during the acknowledge bit. $\overline{\text{INT}}$ deasserts during the slave address acknowledge.

Typically, the master reads 1 or 2 bytes from the MAX7323, each byte being acknowledged by the master upon reception, with the exception of the last byte.

When the master reads 1 byte from the MAX7323 it subsequently issues a STOP condition (Figure 6).

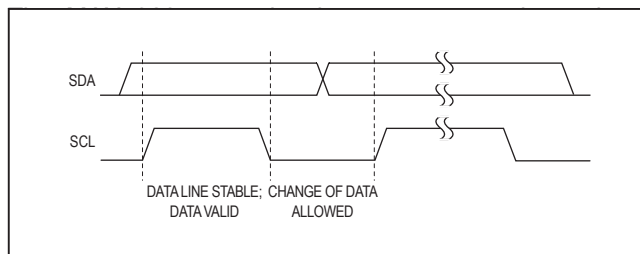


Figure 3. Bit Transfer

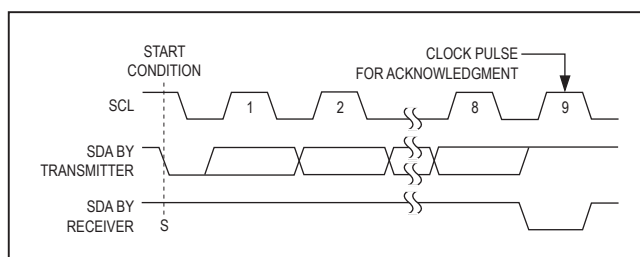


Figure 4. Acknowledge

the change flags, and resets the transition detection. $\overline{\text{INT}}$ deasserts during the slave acknowledge. The new snapshot data is the current input port data transmitted to the master, so any input port changes that occur during the transmission are detected. $\overline{\text{INT}}$ remains high until the STOP condition.

The master can read 2 bytes from the MAX7323 and then issues a STOP condition (Figure 7). In this case, the MAX7323 transmits the current port data, followed by the change flags. The change flags are cleared, and transition detection restarted. $\overline{\text{INT}}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave acknowledge. The new snapshot data is the current port data transmitted to the master, so any port changes occurring during the transmission are detected. $\overline{\text{INT}}$ remains high until the STOP condition.

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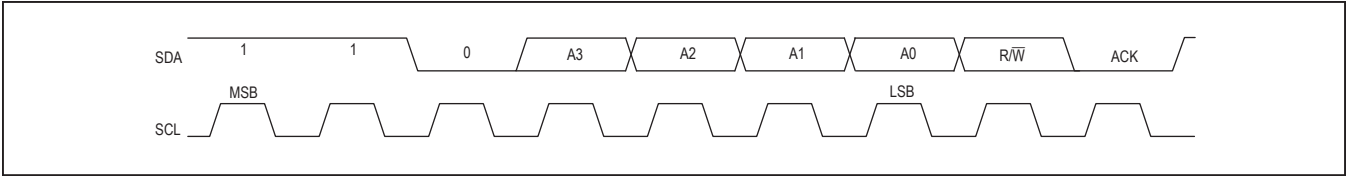


Figure 5. Slave Address

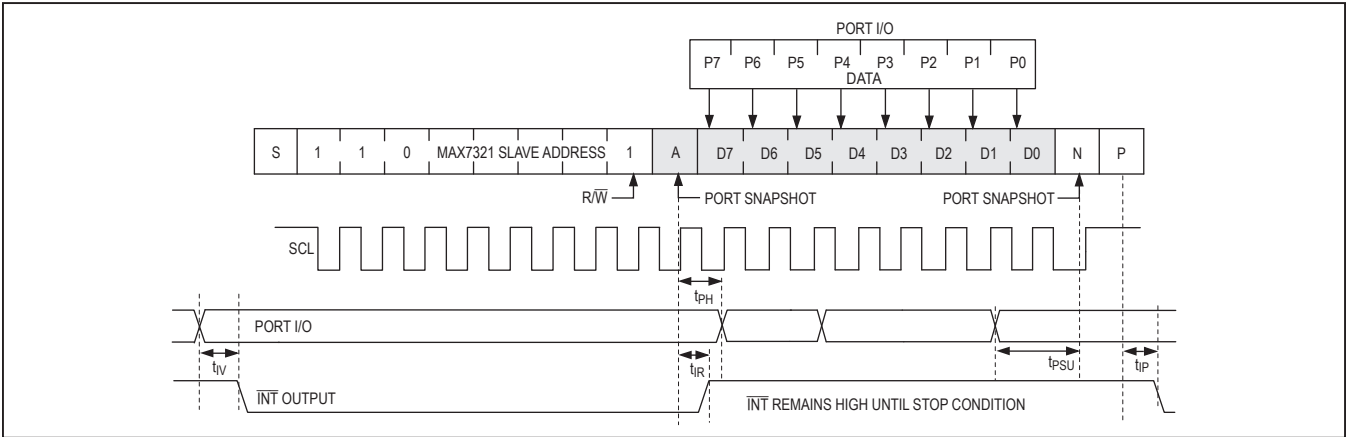


Figure 6. Reading the MAX7323 (1 Data Byte)

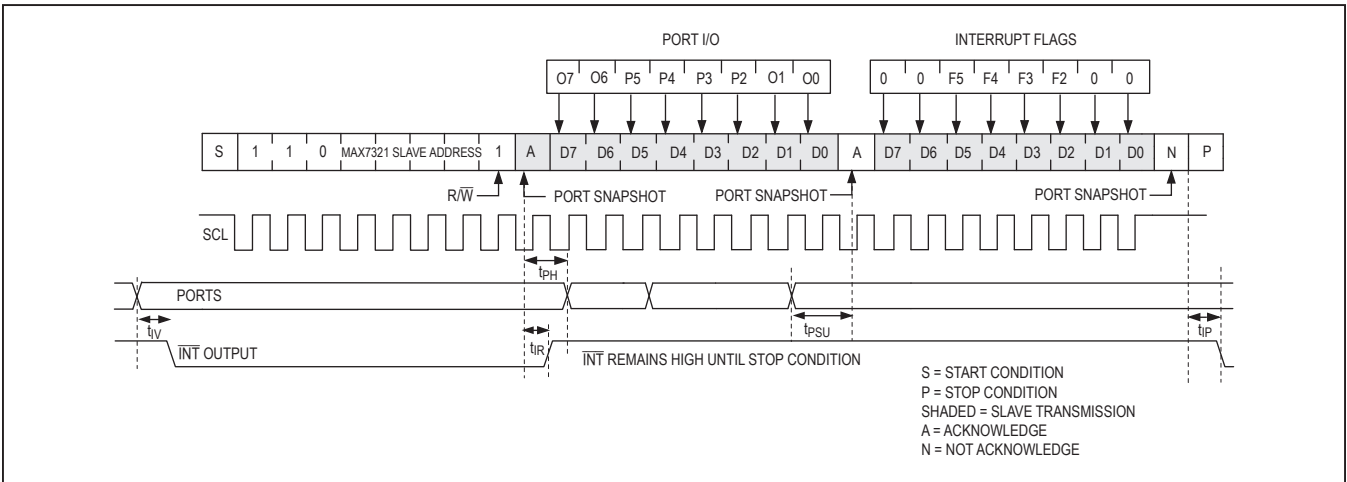


Figure 7. Reading the MAX7323 (2 Data Bytes)

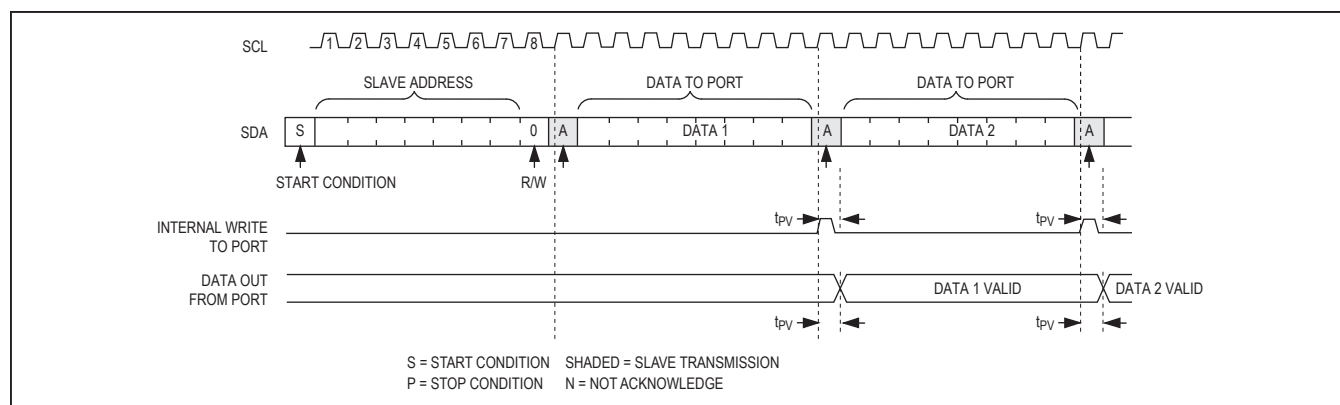


Figure 8. Writing to the MAX7323

Writing to the MAX7323

A write to the MAX7323 starts with the master transmitting the MAX7323's slave address with the R/W bit set low. The MAX7323 acknowledges the slave address, and samples the input ports during acknowledge. $\overline{\text{INT}}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave acknowledge. The master can now transmit 1 or more bytes of data. The MAX7323 acknowledges these subsequent bytes of data and updates the interrupt mask register with each new byte until the master issues a STOP condition (Figure 8).

Applications Information

Port Input and I²C Interface Level Translation from Higher or Lower Logic Voltages

The MAX7323's SDA, SCL, AD0, AD2, $\overline{\text{RST}}$, $\overline{\text{INT}}$, and P2–P5 are overvoltage protected to +6V independent of V^+ . This allows the MAX7323 to operate from a lower supply voltage, such as +3.3V, while the I²C interface and/or some of the four I/O ports are driven from a higher logic level, such as +5V.

The MAX7323 can operate from a higher supply voltage, such as +3V, while the I²C interface and/or some of the four I/O ports P2–P5 are driven from a lower logic level, such as +2.5V. Apply a minimum voltage of $0.7 \times V^+$ to assert a logic-high on any input. For example, a MAX7323 operating from a +5V supply may not recognize a +3.3V nominal logic-high. One solution for input-level translation is to drive the MAX7323 inputs from open-drain outputs. Use a pullup resistor to V^+ or a

higher supply to ensure a high logic voltage greater than $0.7 \times V^+$.

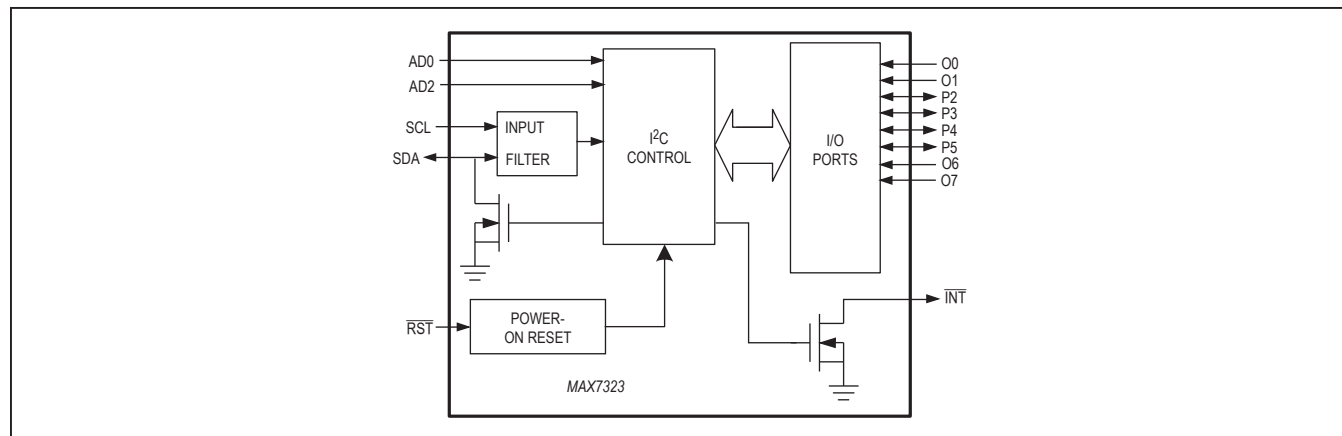
Port-Output Port-Level Translation

The open-drain output architecture allows for level translation to higher or lower voltages than the MAX7323's supply. Use an external pullup resistor on any output to convert the high-impedance logic-high condition to a positive voltage level. The resistor can be connected to any voltage up to +6V, and the resistor value chosen to ensure no more than 20mA is sunk in the logic-low condition. For interfacing CMOS inputs, a pullup resistor value of 220k Ω is a good starting point. Use a lower resistance to improve noise immunity, in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.

Each of the four output ports O0, O1, O6, and O7 has protection diodes to GND (Figure 9). When a port is driven to a voltage lower than GND, the protection diode clamps the output to a diode drop below GND.

Each of the four I/O ports P2–P5 also has a 40k Ω (typ) pullup resistor that can be enabled or disabled. When a port is driven to a voltage higher than V^+ , the body diode of the pullup enable switch conducts and the 40k Ω pullup resistor is enabled. When the MAX7323 is powered down ($V^+ = 0$), each I/O port appears as a 40k Ω resistor in series with a diode connected to zero. Each port is protected to +6V under any of these circumstances (Figure 10).

Functional Diagram



Driving LED Loads

When driving LEDs from one of the four output ports (O0, O1, O6, or O7), a resistor must be connected in series with the LED to limit the LED current to no more than 20mA. Connect the LED cathode to the MAX7323 port, and the LED anode to V⁺ through the series current-limiting resistor, R_{LED}. Set the port output low to illuminate the LED. Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL}) / I_{LED}$$

where:

R_{LED} is the resistance of the resistor in series with the LED (Ω).

V_{SUPPLY} is the supply voltage used to drive the LED (V).

V_{LED} is the forward voltage of the LED (V).

V_{OL} is the output-low voltage of the MAX7323 when sinking I_{LED} (V).

I_{LED} is the desired operating current of the LED (A).

For example, to operate a 2.2V red LED at 10mA from a +5V supply:

$$R_{LED} = (5 - 2.2 - 0.07) / 0.010 = 270\Omega.$$

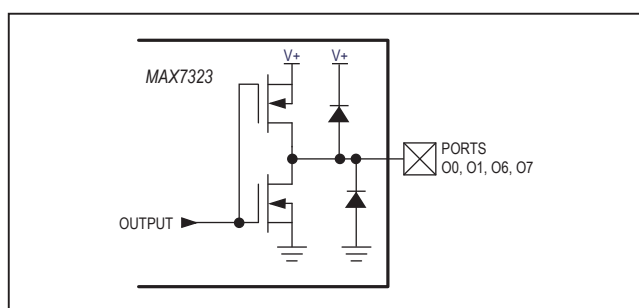


Figure 9. MAX7323 Push-Pull Output Port Structure

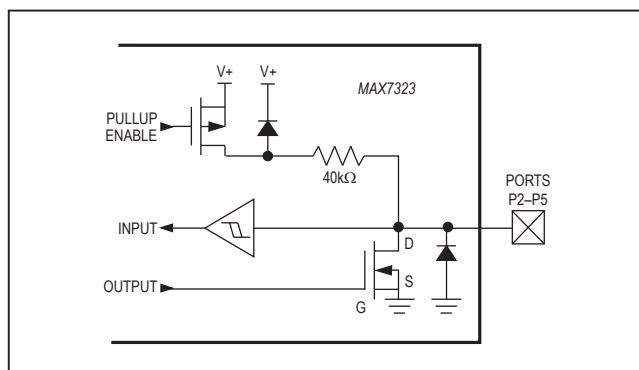


Figure 10. MAX7323 I/O Port Structure

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I²C Port Expander with 4 Push-Pull Outputs and 4 Open-Drain I/Os

Driving Load Currents Higher than 20mA

The MAX7323 can be used to drive loads, such as relays, that draw more than 20mA by paralleling outputs. Use at least one output per 20mA of load current; for example, a 5V, 330mW relay draws 66mA, and therefore, requires four paralleled outputs. Any combination of outputs can be used as part of a load-sharing design because any combination of ports can be set or cleared at the same time by writing to the MAX7323. Do not exceed a total sink current of 100mA for the device.

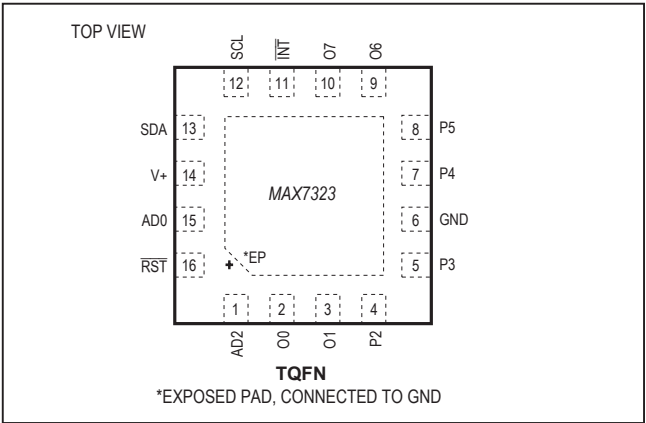
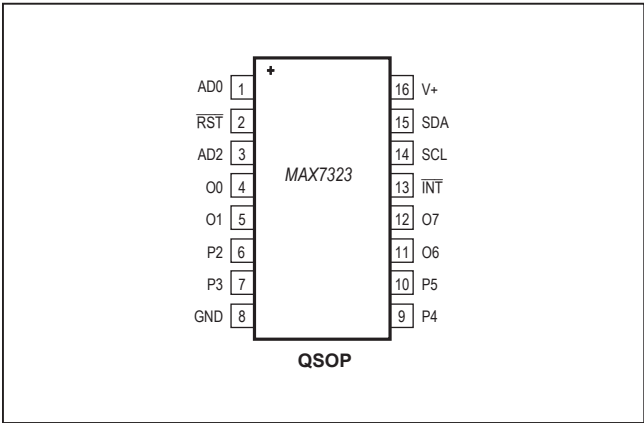
The MAX7323 must be protected from the negative voltage transient generated when switching off inductive loads (such as relays), by connecting a reverse-

biased diode across the inductive load. Choose the peak current for the diode to be greater than the inductive load's operating current.

Power-Supply Considerations

The MAX7323 operates with a supply voltage of +1.71V to +5.5V over the -40°C to +125°C temperature range. Bypass the supply to GND with a ceramic capacitor of at least 0.047μF as close as possible to the device. For the TQFN version, additionally connect the exposed pad to GND.

Pin Configurations



Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+4	21-0055	90-0167
16 TQFN-EP	T1633+4	21-0136	90-0031

MAX7323

I²C Port Expander with 4 Push-Pull
Outputs and 4 Open-Drain I/Os

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	7/07	—	1–17
2	5/14	No /V OPNs; removed automotive reference from <i>Applications</i> section; updated <i>Packaging Information</i>	1

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