High-Efficiency, 4A, Step-Down Regulator with Integrated Switches in 2mm x 2mm Package

ABSOLUTE MAXIMUM RATINGS

IN, V_{DD}, PWRGD to GND .....-0.3V to +4.5V
LX to GND.....-0.3V to the lower of 4.5V or (V_{IN} + 0.3V)
LX Transient .....(V_{GND} - 1.5V, <50ns), (V_{IN} + 1.5V, <50ns)
COMP, FB, REFIN/SS,
EN to GND.....-0.3V to the lower of 4.5V or (V_{DD} + 0.3V)
LX RMS Current (Note 1) 5A
BST to LX.....-0.3V to +4V
BST to GND .....-0.3V to +8V

Continuous Power Dissipation (T_A = +70°C)
16-Bump (4 x 4 Array), 0.5mm Pitch WLP
(derated 12.5mW/°C above +70°C).....1000mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Continuous Operating Temperature at
Full Load Current (Note 2) .....+105°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Note 1: LX has internal clamp diodes to GND and IN. Applications that forward bias these diodes should take care not to exceed the package power dissipation limit of the device.

Note 2: Continuous operation at full current beyond +105°C may degrade product life.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DD} = 3.3V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN/V_{DD}						
IN and V_{DD} Voltage Range			2.40		3.60	V
IN Supply Current	No load, no switching	V_{IN} = 2.5V		0.52	1	mA
		V_{IN} = 3.3V		0.8	1.5	
V_{DD} Supply Current	No load, no switching	V_{IN} = 2.5V		3.7	5.5	mA
		V_{IN} = 3.3V		4	6	
Total Supply Current (IN + V_{DD})	No load	V_{IN} = V_{DD} = 2.5V		12		mA
		V_{IN} = V_{DD} = 3.3V		23		
Total Shutdown Current from IN and V_{DD}	V_{IN} = V_{DD} = V_{BST} - V_{LX} = 3.6V, V_{EN} = 0V			0.1	2	µA
V_{DD} Undervoltage Lockout Threshold	LX starts/stops switching	V_{DD} rising		2	2.2	V
		V_{DD} falling	1.75	1.9		
V_{DD} UVLO Deglitching				2		µs
BST						
BST Leakage Current	V_{BST} = V_{DD} = V_{IN} = 3.6V, V_{LX} = 3.6V or 0V, V_{EN} = 0V	T_A = +25°C			2	µA
		T_A = +85°C		0.025		
PWM COMPARATOR						
PWM Comparator Propagation Delay	10mV overdrive			10		ns
COMP						
COMP Clamp Voltage High	V_{DD} = 2.4V to 3.6V			2.03		V
COMP Clamp Voltage Low	V_{DD} = 2.4V to 3.6V			0.73		V
COMP Slew Rate				1.6		V/µs
PWM Ramp Valley	V_{DD} = 2.4V to 3.6V			830		mV
PWM Ramp Amplitude				1		V
COMP Shutdown Resistance	From COMP to GND, V_{EN} = 0V			8		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = 3.3V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
ERROR AMPLIFIER							
FB Regulation Accuracy	Using internal reference			0.594	0.600	0.606	V
Open-Loop Voltage Gain	1kΩ from COMP to GND (Note 4)				115		dB
Error-Amplifier Unity-Gain Bandwidth	Series 5kΩ, 100nF from COMP to GND (Note 4)				26		MHz
Error-Amplifier Common-Mode Input Range	V_{DD} = 2.4V to 2.6V			0		V_{DD} - 1.80	V
	V_{DD} = 2.6V to 3.6V			0		V_{DD} - 1.85	
Error-Amplifier Minimum Output Current	V_{COMP} = 1.2V, sinking			500			µA
	V_{COMP} = 1.0V, sourcing			1000			
FB Input Bias Current	V_{FB} = 0.7V, using internal reference, T_A = +25°C			-200	-100		nA
REFIN/SS							
REFIN/SS Charging Current	$V_{REFIN/SS}$ = 0.45V			7	8	9	µA
REFIN/SS Discharge Resistance					520		Ω
REFIN/SS Common-Mode Range	V_{DD} = 2.4V to 2.6V			0		V_{DD} - 1.80	V
	V_{DD} = 2.6V to 3.6V			0		V_{DD} - 1.85	
REFIN/SS Offset Voltage	Error amplifier offset	T_A = +25°C			30		µV
				-4.5		+4.5	mV
LX (ALL BUMPS COMBINED)							
LX On-Resistance, High Side	I_{LX} = -0.4A	V_{IN} = V_{BST} - V_{LX} = 2.5V			21		mΩ
		V_{IN} = V_{BST} - V_{LX} = 3.3V			19		
LX On-Resistance, Low Side	I_{LX} = 0.4A	V_{IN} = 2.5V			16		mΩ
		V_{IN} = 3.3V			15		
LX Peak Current-Limit Threshold	V_{IN} = 2.5V	High-side sourcing		5.5	7		A
		Low-side sinking		5.5	7		
LX Leakage Current	V_{IN} = 3.6V, V_{EN} = 0V	T_A = +25°C	V_{LX} = 0V	-2			µA
			V_{LX} = 3.6V			+2	
		T_A = +85°C			0.2		
LX Switching Frequency	V_{IN} = 2.5V to 3.3V, T_A = +25°C			0.92	1	1.03	MHz
LX Maximum Duty Cycle	V_{IN} = 2.5V to 3.3V, T_A = +25°C			92	96		%
LX Minimum On-Time					80		ns
RMS LX Output Current				4			A
ENABLE							
EN Input Logic-Low Threshold						0.7	V
EN Input Logic-High Threshold				1.7			V
EN Input Current	V_{EN} = 0 or 3.6V, V_{IN} = V_{DD} = 3.6V	T_A = +25°C				1	µA
		T_A = +85°C			0.3		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = 3.3V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 3)

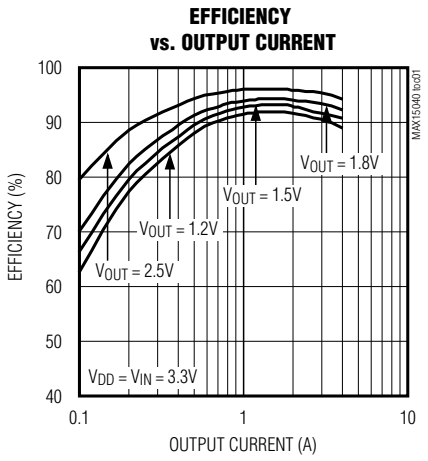
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL SHUTDOWN					
Thermal-Shutdown Threshold	Rising		+165		°C
Thermal-Shutdown Hysteresis			20		°C
POWER-GOOD (PWRGD)					
Power-Good Threshold Voltage	V_{FB} falling, $V_{REFIN/SS}$ = 0.6V	87	90	93	% of $V_{REFIN/SS}$
	V_{FB} rising, $V_{REFIN/SS}$ = 0.6V		92.5		
Power-Good Edge Deglitch	V_{FB} falling or rising		48		Clock cycles
PWRGD Output-Voltage Low	I_{PWRGD} = 4mA (sinking)		0.03	0.15	V
PWRGD Leakage Current	V_{DD} = V_{PWRGD} = 3.6V, V_{FB} = 0.9V		0.01		µA
OVERCURRENT LIMIT (HICCUP MODE)					
Current-Limit Startup Blanking			112		Clock cycles
Restart Time			896		Clock cycles
FB Hiccup Threshold	V_{FB} falling		70		% of $V_{REFIN/SS}$
Hiccup Threshold Blanking Time	V_{FB} falling		36		µs

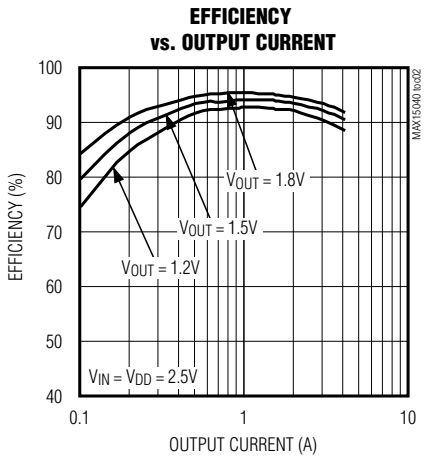
Note 3: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

Note 4: Guaranteed by design.

Typical Operating Characteristics

(V_{IN} = V_{DD} = 3.3V, output voltage = 1.8V, I_{LOAD} = 4A, and T_A = +25°C, circuit of Figure 1, unless otherwise noted.)

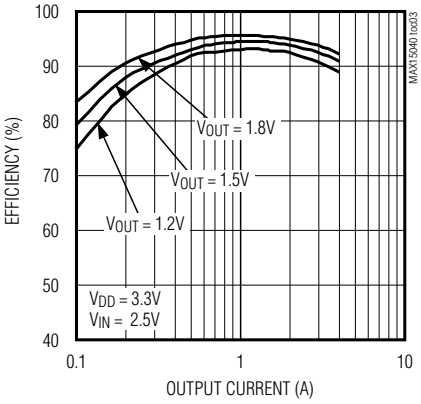




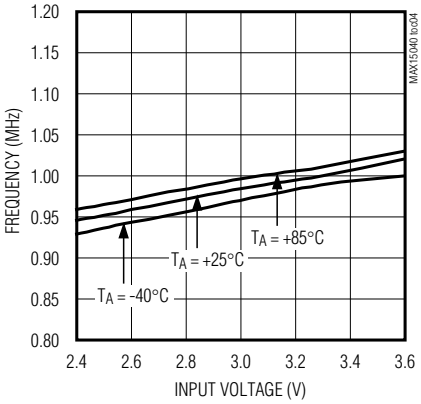
Typical Operating Characteristics (continued)

(V_{IN} = V_{DD} = 3.3V, output voltage = 1.8V, I_{LOAD} = 4A, and T_A = +25°C, circuit of Figure 1, unless otherwise noted.)

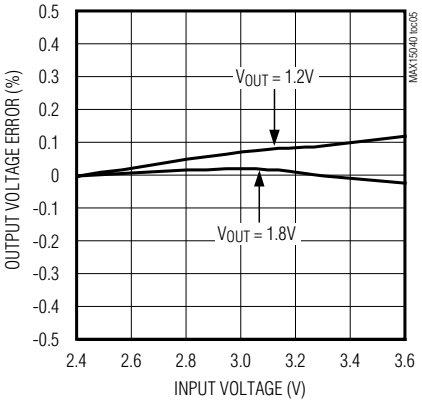
EFFICIENCY vs. OUTPUT CURRENT



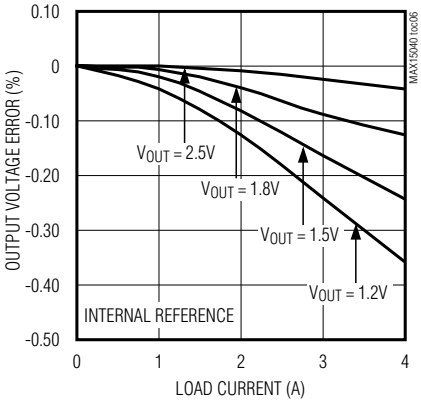
FREQUENCY vs. INPUT VOLTAGE



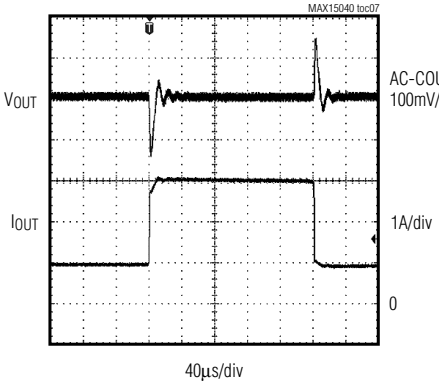
LINE REGULATION



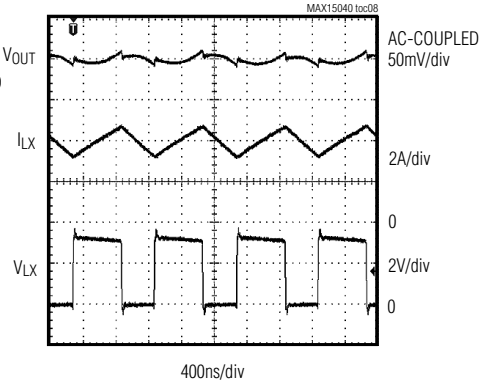
LOAD REGULATION



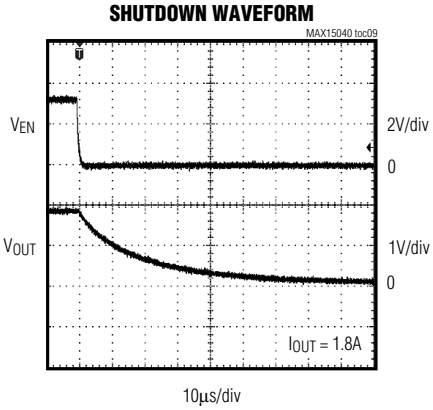
LOAD-TRANSIENT RESPONSE



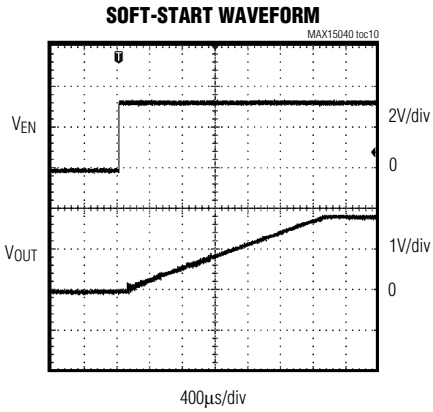
SWITCHING WAVEFORMS



SHUTDOWN WAVEFORM



SOFT-START WAVEFORM

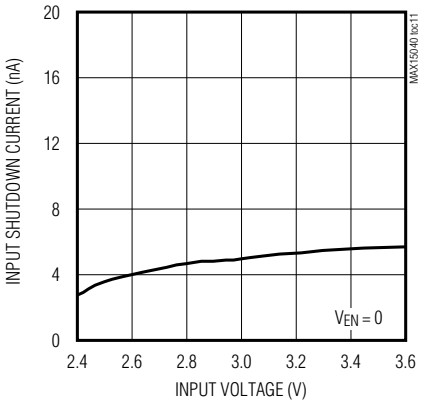


High-Efficiency, 4A, Step-Down Regulator with Integrated Switches in 2mm x 2mm Package

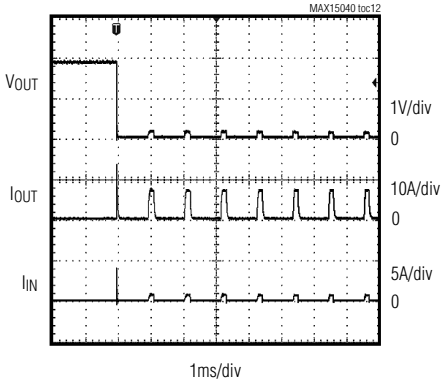
Typical Operating Characteristics (continued)

(V_{IN} = V_{DD} = 3.3V, output voltage = 1.8V, I_{LOAD} = 4A, and T_A = +25°C, circuit of Figure 1, unless otherwise noted.)

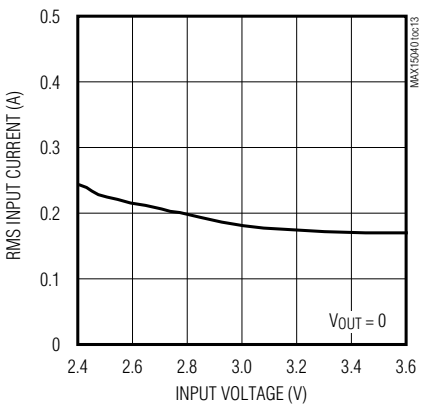
INPUT SHUTDOWN CURRENT vs. INPUT VOLTAGE



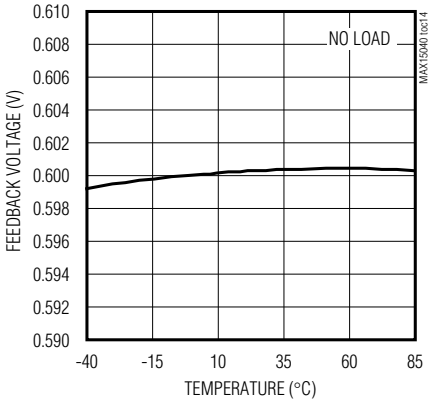
HICCUP CURRENT LIMIT



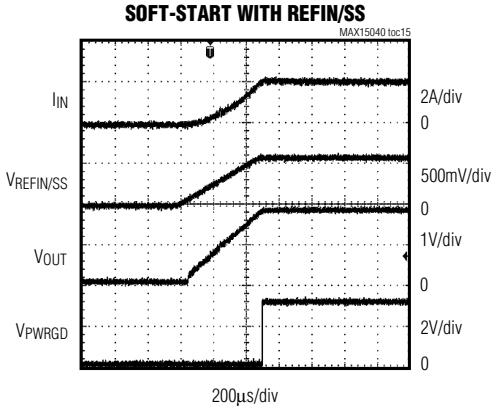
RMS INPUT CURRENT DURING SHORT CIRCUIT vs. INPUT VOLTAGE



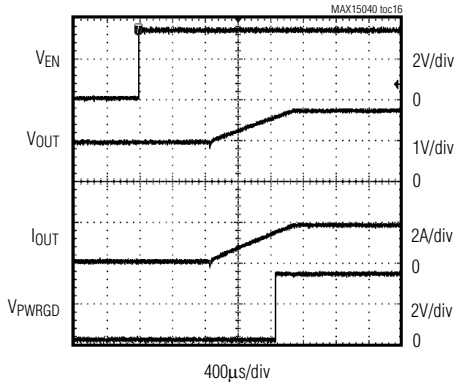
FEEDBACK VOLTAGE vs. TEMPERATURE



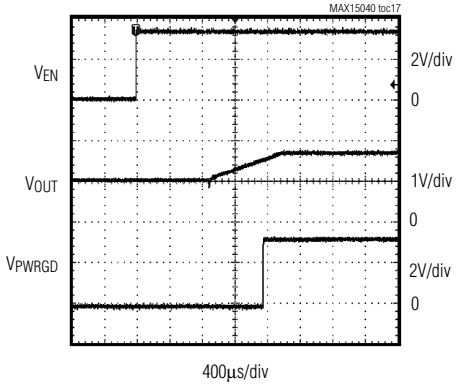
SOFT-START WITH REFIN/SS



STARTING INTO PREBIAS OUTPUT WITH 2A LOAD



STARTING INTO PREBIAS OUTPUT WITH NO LOAD

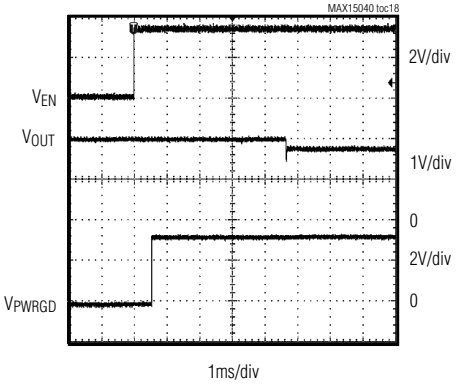


High-Efficiency, 4A, Step-Down Regulator with Integrated Switches in 2mm x 2mm Package

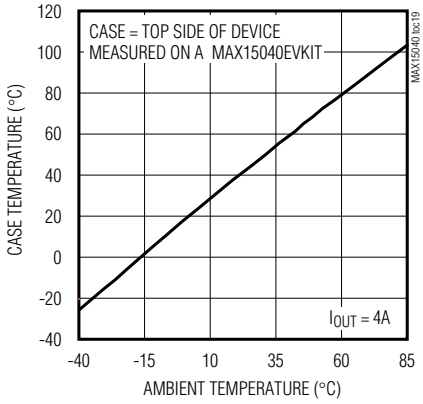
Typical Operating Characteristics (continued)

(V_{IN} = V_{DD} = 3.3V, output voltage = 1.8V, I_{LOAD} = 4A, and T_A = +25°C, circuit of Figure 1, unless otherwise noted.)

STARTING INTO PREBIAS OUTPUT ABOVE NOMINAL SETPOINT WITH NO LOAD



CASE TEMPERATURE vs. AMBIENT TEMPERATURE

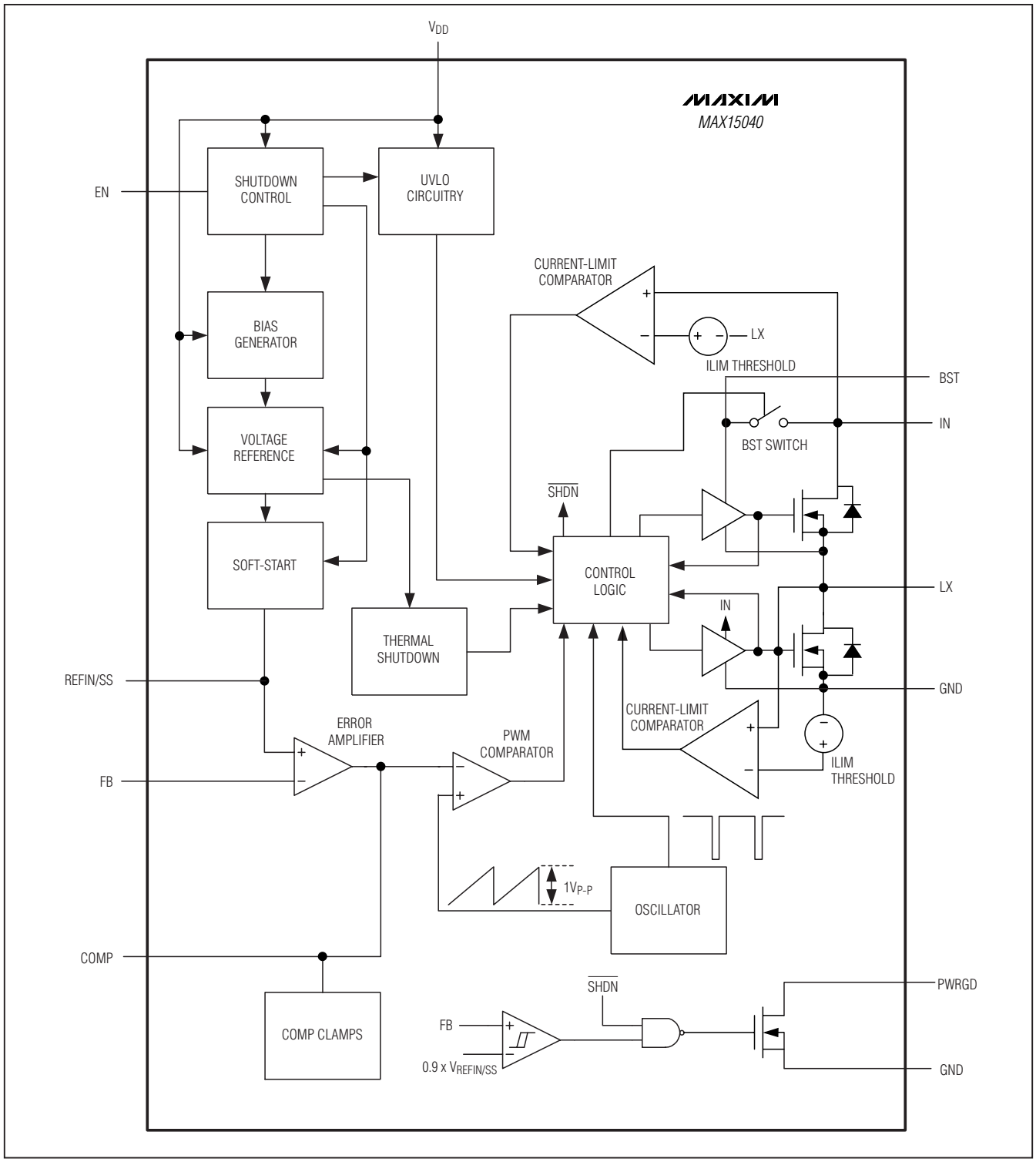


Pin Description

BUMP	NAME	FUNCTION
A1, A2	GND	Analog/Power Ground. Connect GND to the PCB ground plane at one point near the input bypass capacitor return terminal as close as possible to the device.
A3, A4	IN	Power-Supply Input. Input supply range is from 2.4V to 3.6V. Bypass IN to GND with a 22µF ceramic capacitor in parallel to a 0.1µ F ceramic capacitor as close as possible to the device.
B1, B2, B3	LX	Inductor Connection. All LX bumps are internally connected together. Connect all LX bumps to the switched side of the inductor. LX is high impedance when the device is in shutdown mode.
B4	V_{DD}	Supply Input. V_{DD} powers the internal analog core. Connect V_{DD} to IN with a 10Ω resistor. Connect a 1µF ceramic capacitor from V_{DD} to GND.
C1	BST	High-Side MOSFET Driver Supply. Bypass BST to LX with a 0.1µF capacitor.
C2, C3	I.C.	Internally Connected. Leave unconnected or connect to ground.
C4	EN	Enable Input. Connect EN to GND to disable the device. Connect EN to V_{DD} to enable the device.
D1	PWRGD	Power-Good Output. PWRGD is an open-drain output that goes high impedance when V_{FB} exceeds 92.5% of $V_{REFIN/SS}$ and $V_{REFIN/SS}$ is above 0.54V. PWRGD is internally pulled low when V_{FB} falls below 90% of $V_{REFIN/SS}$ or $V_{REFIN/SS}$ is below 0.54V. PWRGD is internally pulled low when the device is in shutdown mode, V_{DD} is below the internal UVLO threshold, or the device is in thermal shutdown.
D2	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to GND to set the output voltage from 0.6V to 90% of V_{IN}.
D3	COMP	Voltage-Error Amplifier Output. Connect the necessary compensation network from COMP to FB and the converter output (see the *Compensation Design* section). COMP is internally pulled to GND when the device is in shutdown mode.
D4	REFIN/SS	External Reference Input/Soft-Start Timing Capacitor Connection. Connect REFIN/SS to a system voltage to force FB to regulate to REFIN/SS voltage. REFIN/SS is internally pulled to GND when the device is in shutdown and thermal shutdown mode. If no external reference is applied, the internal 0.6V reference is automatically selected. REFIN/SS is also used to perform soft-start. Connect a minimum of 1nF capacitor from REFIN/SS to GND to set the startup time (see the *Soft-Start and Reference Input (REFIN/SS)* section).

High-Efficiency, 4A, Step-Down Regulator with Integrated Switches in 2mm x 2mm Package

Block Diagram



High-Efficiency, 4A, Step-Down Regulator with Integrated Switches in 2mm x 2mm Package

Typical Application Circuit

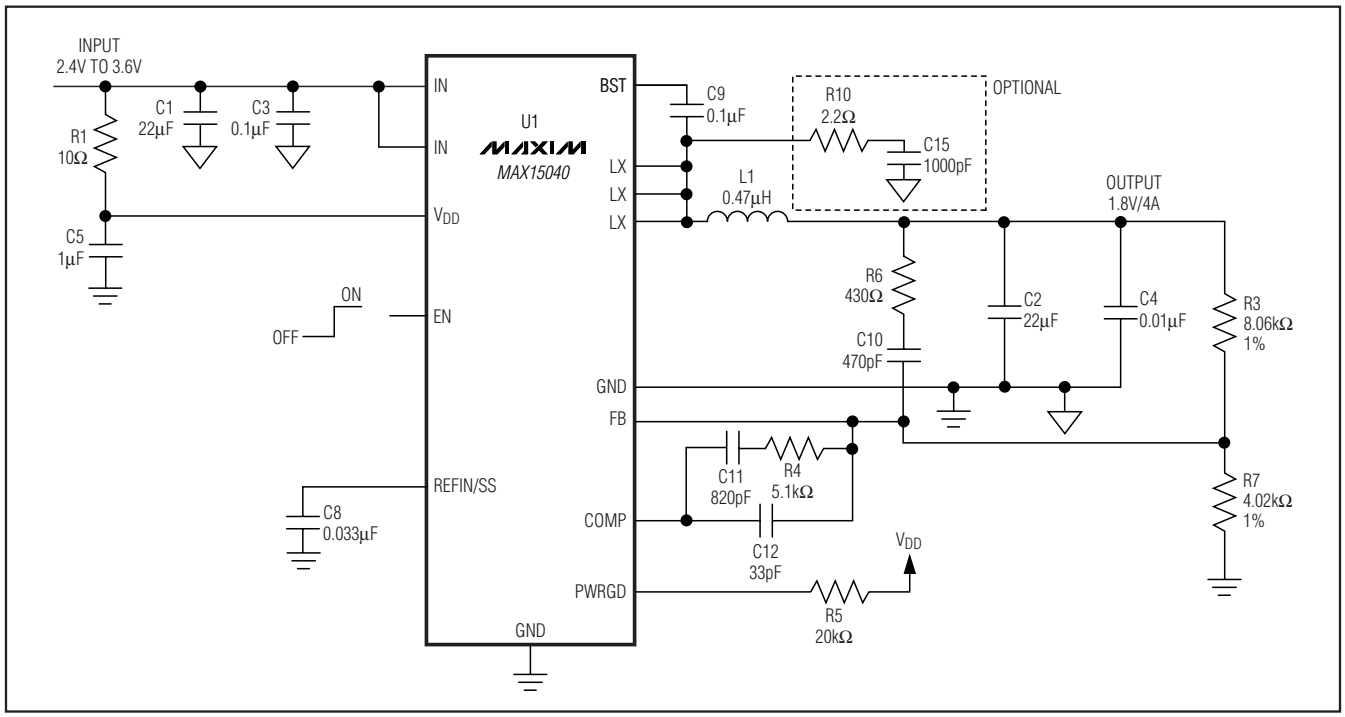


Figure 1. All-Ceramic Capacitor Design with V_{OUT} = 1.8V

Detailed Description

The MAX15040 high-efficiency, voltage-mode switching regulator is capable of delivering up to 4A of output current. The MAX15040 provides output voltages from 0.6V to (0.9 x V_{IN}) from 2.4V to 3.6V input supplies, making it ideal for on-board point-of-load applications. The output-voltage accuracy is better than ±1% over load, line, and temperature.

The MAX15040 features a 1MHz fixed switching frequency, allowing the user to achieve all-ceramic capacitor designs and fast transient responses. The high operating frequency minimizes the size of external components. The MAX15040 is available in a 2mm x 2mm, 16-bump (4 x 4 array), 0.5mm pitch WLP package. The REFIN/SS function makes the MAX15040 an ideal solution for DDR and tracking power supplies. Using internal low-R_{DSON} (15mΩ) n-channel MOSFETs for both high- and low-side switches maintains high efficiency at both heavy-load and high-switching frequencies.

The MAX15040 employs voltage-mode control architecture with a high-bandwidth (> 15MHz) error amplifier. The op-amp voltage-error amplifier works with Type III compensation to fully utilize the bandwidth of the high-frequency switching to obtain fast transient response. Adjustable soft-start time provides flexibilities to minimize input startup inrush current. An open-drain, power-good (PWRGD) output goes high impedance when V_{FB} exceeds 92.5% of $V_{REFIN/SS}$ and $V_{REFIN/SS}$ is above 0.54V. PWRGD goes low when V_{FB} falls below 90% of $V_{REFIN/SS}$ or $V_{REFIN/SS}$ is below 0.54V.

Controller Function

The controller logic block is the central processor that determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current-limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator and generates the driver signals for both high-side and low-side MOSFETs. The control logic block controls the break-before-make logic and the timing for charging the bootstrap capacitors. The error signal from the voltage-error amplifier is compared with the ramp signal generated by the oscillator at the PWM comparator to produce the required PWM signal. The high-side switch turns on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the V_{COMP} signal or the current-limit threshold is exceeded. The low-side switch then turns on for the remainder of the oscillator cycle.

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Current Limit

The internal, high-side MOSFET has a typical 7A peak current-limit threshold. When current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the low-side MOSFET turns on. The low-side MOSFET remains on until the inductor current falls below the low-side current limit. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. The MAX15040 uses a hiccup mode to prevent overheating during short-circuit output conditions.

During current limit, if V_{FB} drops below 70% of $V_{REFIN/SS}$ and stays below this level for typically 36µs (12µs min) or more, the device enters hiccup mode. The high-side MOSFET and the low-side MOSFET turn off and both COMP and REFIN/SS are internally pulled low. The device remains in this state for 896 clock cycles and then attempts to restart for 112 clock cycles. If the fault-causing current limit has cleared, the device resumes normal operation. Otherwise, the device reenters hiccup mode.

Soft-Start and Reference Input (REFIN/SS)

The MAX15040 utilizes an adjustable soft-start function to limit inrush current during startup. An 8µA (typ) current source charges an external capacitor connected to REFIN/SS. The soft-start time is adjusted by the value of the external capacitor from REFIN/SS to GND. The required capacitance value is determined as:

$$C = \frac{8\mu A \times t_{SS}}{0.6V}$$

where t_{SS} is the required soft-start time in seconds. Connect a minimum 1nF capacitor between REFIN/SS and GND. REFIN/SS is also an external reference input (REFIN/SS). The device regulates FB to the voltage applied to REFIN/SS. The internal soft-start is not available when using an external reference. Figure 2 shows a method of soft-start when using an external reference. If an external reference is not applied, the device uses the internal 0.6V reference.

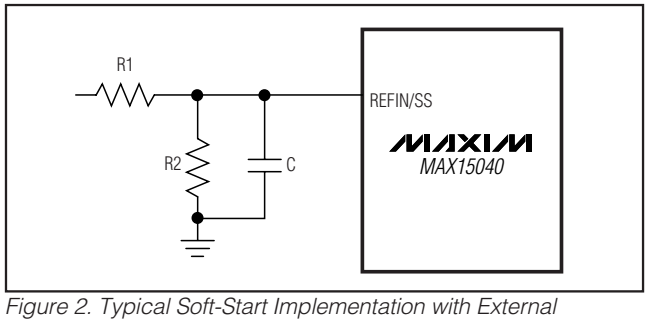

Figure 2. Typical Soft-Start Implementation with External Reference

Undervoltage Lockout (UVLO)

The UVLO circuitry inhibits switching when V_{DD} is below 1.9V (typ). Once V_{DD} rises above 2V (typ), UVLO clears and the soft-start function activates. A 100mV hysteresis is built in for glitch immunity.

BST

The gate-drive voltage for the high-side, n-channel switch is generated by a flying-capacitor boost circuit. The capacitor between BST and LX is charged from the V_{IN} supply while the low-side MOSFET is on. When the low-side MOSFET is switched off, the voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage for the high-side internal MOSFET.

Power-Good Output (PWRGD)

PWRGD is an open-drain output that goes high impedance when V_{FB} is above 92.5% x $V_{REFIN/SS}$ and $V_{REFIN/SS}$ is above 0.54V. PWRGD pulls low when V_{FB} is below 90% of $V_{REFIN/SS}$ for at least 48 clock cycles or $V_{REFIN/SS}$ is below 0.54V. PWRGD is low during shutdown.

Setting the Output Voltage

The MAX15040 output voltage is adjustable from 0.6V to 90% of V_{IN} by connecting FB to the center tap of a resistor-divider between the output and GND (Figure 3). To determine the values of the resistor-divider, first select the value of R3 between 2kΩ and 10kΩ. Then use the following equation to calculate R4:

$$R4 = (V_{FB} \times R3)/(V_{OUT} - V_{FB})$$

where V_{FB} is equal to the reference voltage at REFIN/SS and V_{OUT} is the output voltage. For V_{OUT} = 0.6V, remove R4. If no external reference is applied at REFIN/SS, the internal reference is automatically selected and V_{FB} becomes 0.6V.

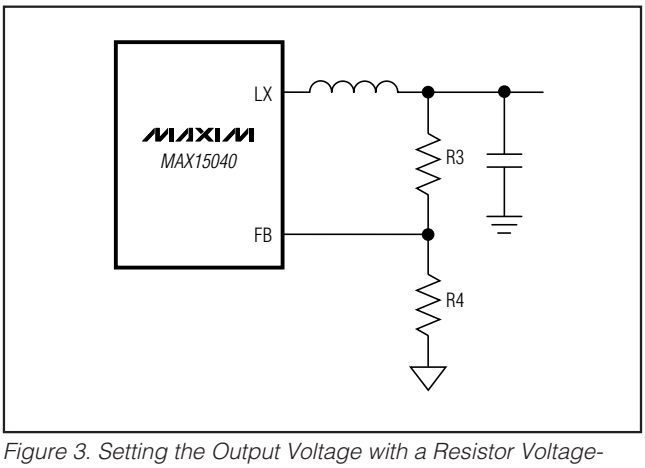

Figure 3. Setting the Output Voltage with a Resistor Voltage-Divider

Shutdown Mode

Drive EN to GND to shut down the device and reduce quiescent current to less than 0.1µA. During shutdown, LX is high impedance. Drive EN high to enable the MAX15040.

Thermal Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J = +165°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, causing a pulsed output during continuous overload conditions. The soft-start sequence begins after recovery from a thermal-shutdown condition.

Applications Information

IN and V_{DD} Decoupling

To decrease the noise effects due to the high switching frequency and maximize the output accuracy of the MAX15040, decouple V_{IN} with a 22µF capacitor in parallel with a 0.1µF capacitor from V_{IN} to GND. Also decouple V_{DD} with a 1µF capacitor from V_{DD} to GND. Place these capacitors as close as possible to the device.

Inductor Selection

Choose an inductor with the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_S \times V_{IN} \times LIR \times I_{OUT(MAX)}}$$

where LIR is the ratio of the inductor ripple current to full load current at the minimum duty cycle and f_S is the switching frequency (1MHz). Choose LIR between 20% to 40% for best performance and stability.

Use an inductor with the lowest possible DC resistance that fits in the allotted dimensions. Powdered iron or ferrite core types are often the best choice for performance. With any core material, the core must be large enough not to saturate at the current limit of the MAX15040.

Output-Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Estimate the output voltage ripple due to the output capacitance, ESR, and ESL as follows:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL \text{ or}$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{OFF}} \times ESL$$

or whichever is higher.

The peak-to-peak inductor current (I_{P-P}) is:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Use these equations for initial output capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

Load-transient response depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to its predetermined value. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, preventing the output from deviating further from its regulating value. See the *Compensation Design* section for more details.

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Input-Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the device. The total input capacitance must be equal to or greater than the value given by the following equation to keep the input ripple voltage within the specification and minimize the high-frequency ripple current being fed back to the input source:

$$C_{IN\_MIN} = \frac{D \times T_S \times I_{OUT}}{V_{IN-RIPPLE}}$$

where $V_{IN-RIPPLE}$ is the maximum allowed input ripple voltage across the input capacitors and is recommended to be less than 2% of the minimum input voltage, D is the duty cycle (V_{OUT}/V_{IN}), and T_S is the switching period ($1/f_S$) = 1µs.

The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source, but are instead shunted through the input capacitor. The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{RIPPLE} is the input RMS ripple current.

Compensation Design

The power transfer function consists of one double pole and one zero. The double pole is introduced by the inductor, L, and the output capacitor, C_O. The ESR of the output capacitor determines the zero. The double pole and zero frequencies are given as follows:

$$f_{P1\_LC} = f_{P2\_LC} = \frac{1}{2\pi \times \sqrt{L \times C_O \times \left(\frac{R_O + ESR}{R_O + R_L}\right)}}$$

$$f_{Z\_ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

where R_L is equal to the sum of the output inductor's DC resistance (DCR) and the internal switch resistance, R_{DSON}. A typical value for R_{DSON} is 15mΩ. R_O is the output load resistance, which is equal to the rated output voltage divided by the rated output current. ESR is the total equivalent series resistance of the output capacitor. If there is more than one output capacitor of the same type in parallel, the value of the ESR in the above equation is equal to that of the ESR of a single output capacitor divided by the total number of output capacitors.

The MAX15040 high switching frequency allows the use of ceramic output capacitors. Since the ESR of ceramic capacitors is typically very low, the frequency of the associated transfer function zero is higher than the unity-gain crossover frequency, f_C, and the zero cannot be used to compensate for the double pole created by the output inductor and capacitor. The double pole produces a gain drop of 40dB/decade and a phase shift of 180°. The compensation network must compensate for this gain drop and phase shift to achieve a stable high-bandwidth closed-loop system. Therefore, use type III compensation as shown in Figure 4 and Figure 5. Type III compensation possesses three poles and two zeros with the first pole, f_{P1_EA}, located at zero frequency (DC). Locations of other poles and zeros of the type III compensation are given by:

$$f_{Z1\_EA} = \frac{1}{2\pi \times R1 \times C1}$$

$$f_{Z2\_EA} = \frac{1}{2\pi \times R3 \times C3}$$

$$f_{P3\_EA} = \frac{1}{2\pi \times R1 \times C2}$$

$$f_{P2\_EA} = \frac{1}{2\pi \times R2 \times C3}$$

The above equations are based on the assumptions that C1 >> C2, and R3 >> R2, which are true in most applications. Placements of these poles and zeros are determined by the frequencies of the double pole and ESR zero of the power transfer function. It is also a function of the desired closed-loop bandwidth. The following section outlines the step-by-step design procedure to calculate the required compensation components for the MAX15040.

The output voltage is determined by:

$$R4 = \frac{0.6 \times R3}{(V_{OUT} - 0.6)}$$

For V_{OUT} = 0.6V, R4 is not needed.

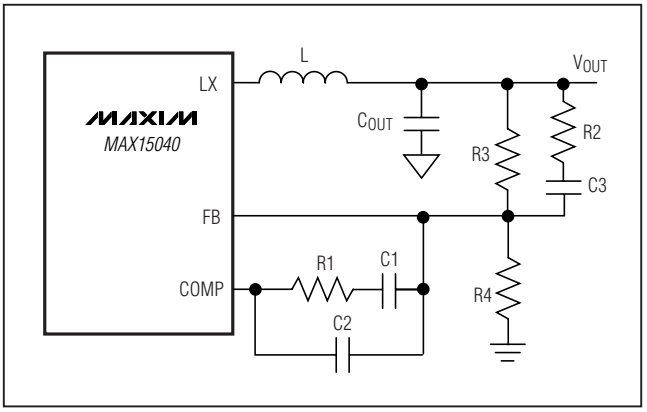

Figure 4. Type III Compensation Network

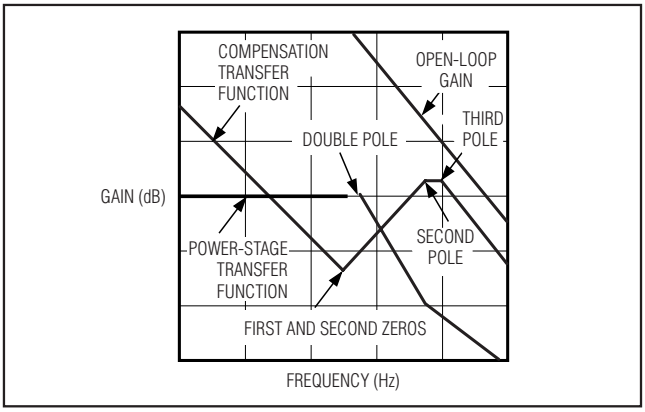

Figure 5. Type III Compensation Illustration

The zero-cross frequency of the closed-loop, f_C, should be between 10% and 20% of the switching frequency, f_S (1MHz). A higher zero-cross frequency results in faster transient response. Once f_C is chosen, C1 is calculated from the following equation:

$$C1 = \frac{2.5\left(\frac{V_{IN}}{V_{P-P}}\right)}{2 \times \pi \times R3 \times (1+\frac{R_L}{R_O}) \times f_C}$$

where V_{P-P} = 1V_{P-P} (typ).

Due to the underdamped nature of the output LC double pole, set the two zero frequencies of the type III compensation less than the LC double-pole frequency to provide adequate phase boost. Set the two zero frequencies to 80% of the LC double-pole frequency. Hence:

$$R1 = \frac{1}{0.8 \times C1} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

$$C3 = \frac{1}{0.8 \times R3} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

Setting the second compensation pole, f_{P2_EA}, at f_{Z_ESR} yields:

$$R2 = \frac{C_O \times ESR}{C3}$$

Set the third compensation pole at 1/2 of the switching frequency (500kHz) to gain phase margin. Calculate C2 as follows:

$$C2 = \frac{1}{\pi \times R1 \times f_S}$$

The above equations provide accurate compensation when the zero-cross frequency is significantly higher than the double-pole frequency. When the zero-cross frequency is near the double-pole frequency, the actual zero-cross frequency is higher than the calculated frequency. In this case, lowering the value of R1 reduces the zero-cross frequency. Also, set the third pole of the type III compensation close to the switching frequency (1MHz) if the zero-cross frequency is above 200kHz to boost the phase margin. The recommended range for R3 is 2kΩ to 10kΩ. Note that the loop compensation remains unchanged if only R4's resistance is altered to set different outputs.

Soft-Starting into a Prebiased Output

The MAX15040 soft-starts into a prebiased output without discharging the output capacitor. In safe prebiased startup, both low-side and high-side switches remain off to avoid discharging the prebiased output. PWM operation starts when the voltage on REFIN/SS crosses the voltage on FB. The PWM activity starts with the low-side switch turning on first to build the bootstrap capacitor charge. Power-good (PWRGD) asserts 48 clock cycles after FB crosses 92.5% of the final regulation set point. After 4096 clock cycles, the device switches from prebiased safe startup mode to forced PWM mode.

The MAX15040 is capable of starting into a prebias voltage higher than the nominal set point without abruptly discharging the output. This is achieved by using the sink current control of the low-side MOSFET, which has four internally set sinking current-limit thresholds. An internal 4-bit DAC steps through these thresholds, starting from the lowest current limit to the highest, in 128 clock cycles on every power-up.

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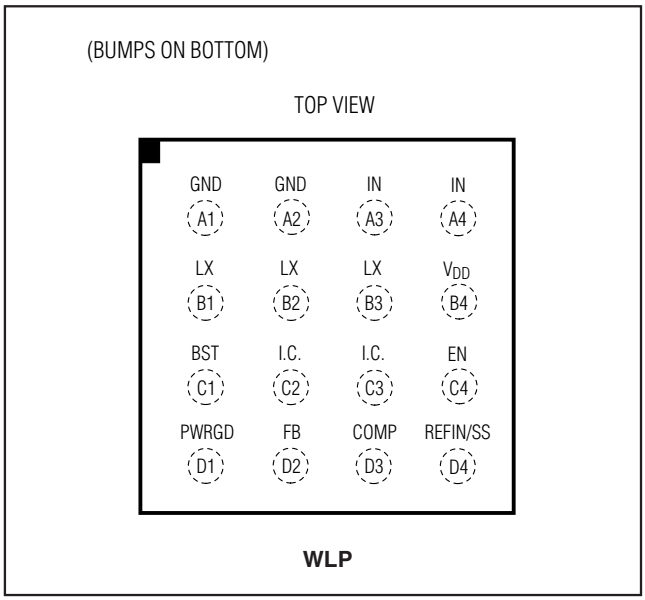
PCB Layout Considerations and Thermal Performance

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX15040 evaluation kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
2) Place capacitors on V_{DD}, IN, and REFIN/SS as close as possible to the device and the corresponding bump using direct traces. Keep power ground plane and signal ground plane separate.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect IN, LX, and GND separately to a large copper area to help cool the device to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short. Place the feedback resistors and compensation components as close to the device as possible.
6) Route high-speed switching nodes, such as LX and BST, away from sensitive analog areas (FB, COMP).

Pin Configuration



WLP

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W162B2+1	21-0200	—

High-Efficiency, 4A, Step-Down Regulator with Integrated Switches in 2mm x 2mm Package

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/09	Initial release	—
1	5/10	Revised the *Absolute Maximum Ratings* and *Electrical Characteristics*.	1–4
2	7/10	Revised the *Absolute Maximum Ratings*.	2