Single-Supply, Low-Power, Serial 8-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6.0V
CH0 to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Output to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Input to GND .....-0.3V to +6.0V
Maximum Current into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C).....714mW

Operating Temperature Range
MAX111_EKA .....-40°C to + 85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX1115), V_{DD} = +4.5V to +5.5V (MAX1116), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				8			Bits
Relative Accuracy	INL	(Note 1)				±1	LSB
Differential Nonlinearity	DNL					±1	LSB
Offset Error						0.5	LSB
Gain Error						±5	%FSR
Gain Temperature Coefficient					90		ppm/°C
V_{DD}/2 Sampling Error					±2	±7	%
DYNAMIC PERFORMANCE (25kHz sine-wave input, V_{IN} = V_{REF} (P-P), f_{SCLK} = 5MHz, f_{SAMPLE} = 100ksps, R_{IN} = 100Ω)							
Signal-to-Noise Plus Distortion	SINAD				48		dB
Total Harmonic Distortion (up to the 5th Harmonic)	THD				-69		dB
Spurious-Free Dynamic Range	SFDR				66		dB
Small-Signal Bandwidth	f_{-3dB}				4		MHz
ANALOG INPUT							
Input Voltage Range				0		V_{REF}	V
Input Leakage Current		V_{CH} = 0 or V_{DD}			±0.7	±10	µA
Input Capacitance	C_{IN}				18		pF
INTERNAL REFERENCE							
Voltage	V_{REF}	MAX1115			2.048		V
		MAX1116			4.096		
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	MAX1115		2.7		5.5	V
		MAX1116		4.5		5.5	
Supply Current (Note 2)	I_{DD}	MAX1115	f_{SAMPLE} = 10ksps		14	21	µA
			f_{SAMPLE} = 100ksps		135	190	
		MAX1116	f_{SAMPLE} = 10ksps		19	25	
			f_{SAMPLE} = 100ksps		182	230	
		Shutdown			0.8	10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX1115), V_{DD} = +4.5V to +5.5V (MAX1116), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Rejection Ratio	PSRR	Full-scale or zero input		±0.5	±1	LSB/V
DIGITAL INPUTS (CNVST AND SCLK)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}			0.2		V
Input Current High	I_{IH}				±10	µA
Input Current Low	I_{IL}				±10	µA
Input Capacitance	C_{IN}			2		pF
DIGITAL OUTPUT (DOUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.4	V
		I_{SINK} = 4mA			0.8	
Three-State Leakage Current	I_L			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}			4		pF
TIMING CHARACTERISTICS (Figures 6a–6d)						
CNVST High Time	t_{csh}		100			ns
CNVST Low Time	t_{csl}		100			ns
Conversion Time	t_{conv}				7.5	µs
Serial Clock High Time	t_{ch}		75			ns
Serial Clock Low Time	t_{cl}		75			ns
Serial Clock Period	t_{cp}		200			ns
Falling of CNVST to DOUT Active	t_{csd}	C_{LOAD} = 100pF, Figure 1			100	ns
Serial Clock Falling Edge to DOUT	t_{cd}	C_{LOAD} = 100pF	10		100	ns
Serial Clock Rising Edge To DOUT High-Z	t_{chz}	C_{LOAD} = 100pF, Figure 2	100		500	ns
Last Serial Clock to Next CNVST (successive conversions on CH0)	t_{ccs}		50			ns

Note 1: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offset have been calibrated.

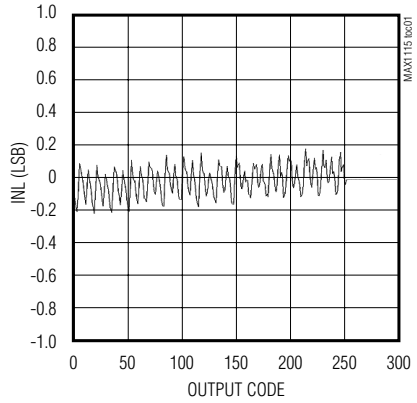
Note 2: Input = 0, with logic input levels of 0 and V_{DD}.

Single-Supply, Low-Power, Serial 8-Bit ADCs

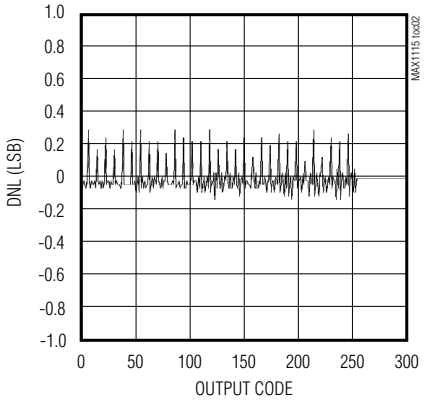
Typical Operating Characteristics

(V_{DD} = +3V (MAX1115), V_{DD} = +5V (MAX1116), f_{SCU} = 5MHz, f_{SAMPLE} = 100ksps, C_{LOAD} = 100pF, T_A = +25°C, unless otherwise noted.)

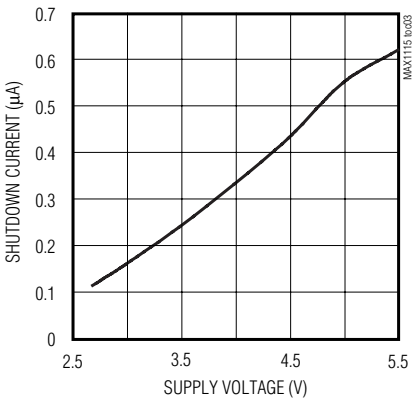
INTEGRAL NONLINEARITY vs. OUTPUT CODE



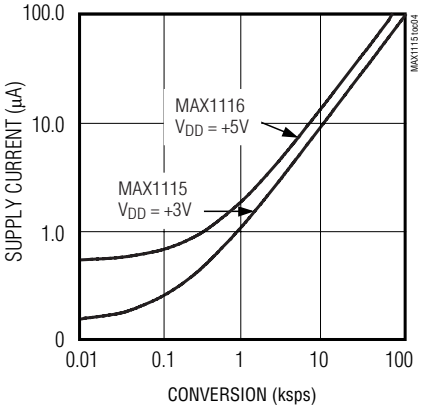
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



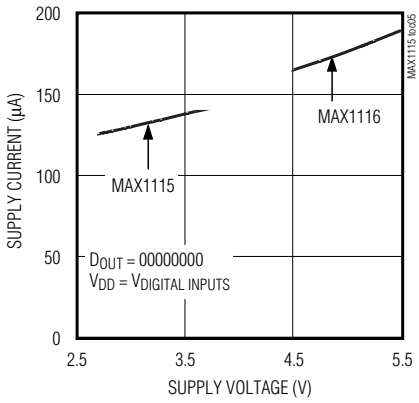
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



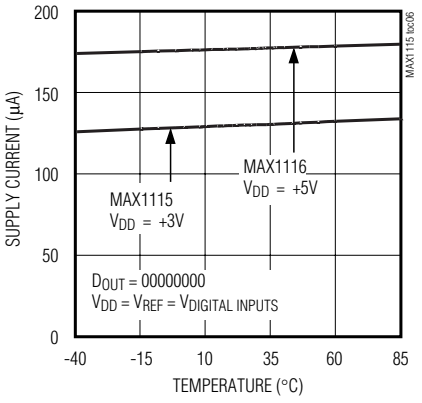
SUPPLY CURRENT vs. CONVERSION RATE



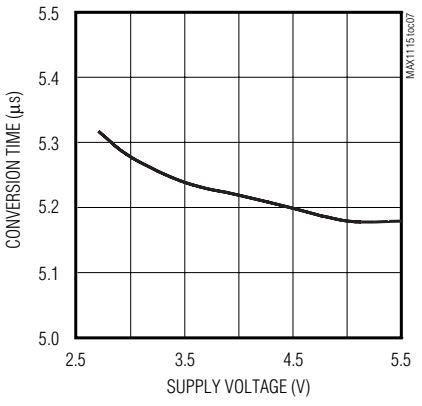
SUPPLY CURRENT vs. SUPPLY VOLTAGE



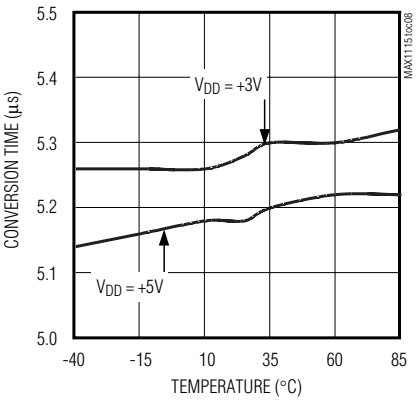
SUPPLY CURRENT vs. TEMPERATURE



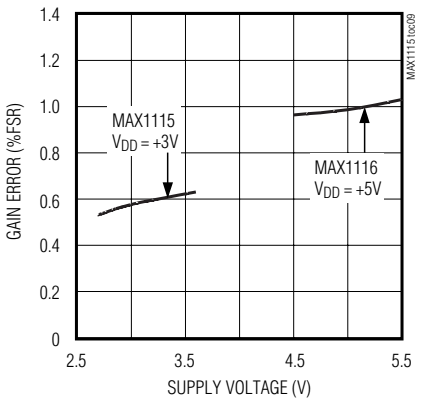
CONVERSION TIME vs. SUPPLY VOLTAGE



CONVERSION TIME vs. TEMPERATURE



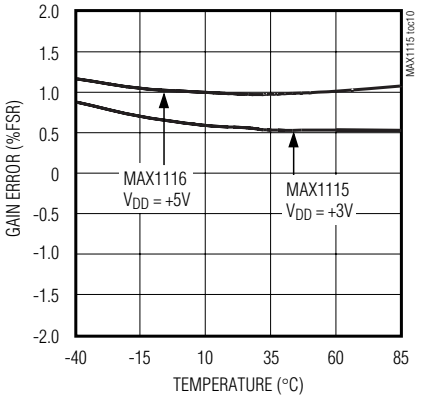
GAIN ERROR vs. SUPPLY VOLTAGE



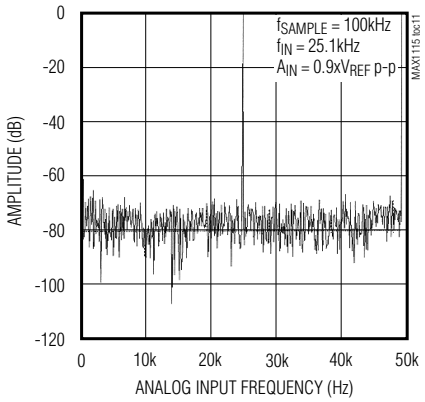
Typical Operating Characteristics (continued)

(V_{DD} = +3V (MAX1115), V_{DD} = +5V (MAX1116), f_{SCU} = 5MHz, f_{SAMPLE} = 100ksps, C_{LOAD} = 100pF, T_A = +25°C, unless otherwise noted.)

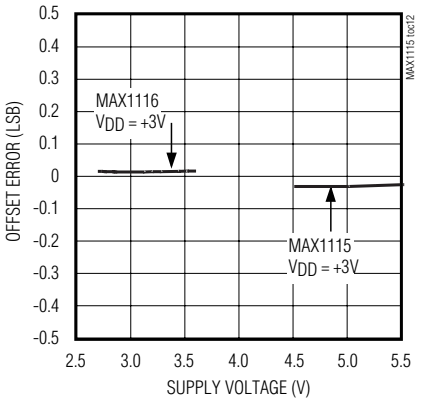
GAIN ERROR vs. TEMPERATURE



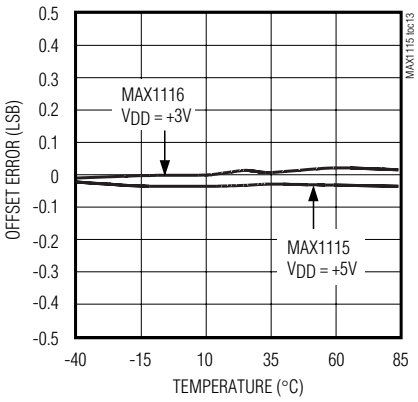
FFT PLOT



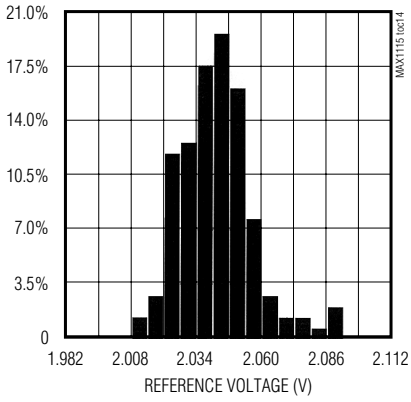
OFFSET ERROR vs. SUPPLY VOLTAGE



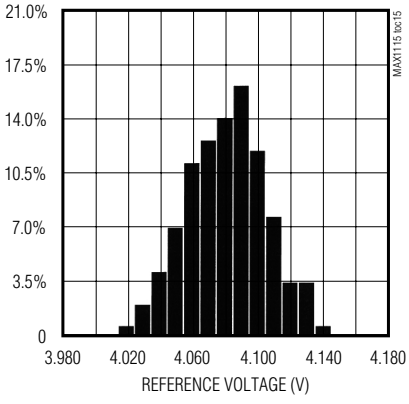
OFFSET ERROR vs. TEMPERATURE



MAX1115 REFERENCE VOLTAGE vs. NUMBER OF PIECES



MAX1116 REFERENCE VOLTAGE vs. NUMBER OF PIECES



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage
2	CH0	Analog Voltage Input
3, 5	I.C.	Internally Connected. Connect to ground.
4	GND	Ground
6	CNVST	Convert/Start Input. CNVST initiates a power-up and starts a conversion on its falling edge.
7	DOUT	Serial Data Output. Data is clocked out on the falling edge of SCLK. DOUT goes low at the start of a conversion and presents the MSB at the completion of a conversion. DOUT goes high impedance once data has been fully clocked out.
8	SCLK	Serial Clock. Used for clocking out data on DOUT.

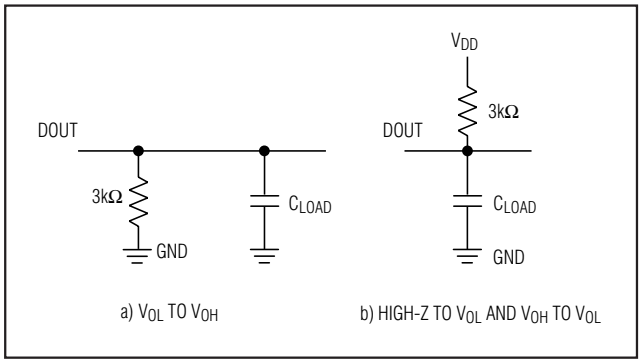


Figure 1. Load Circuits for Enable Time

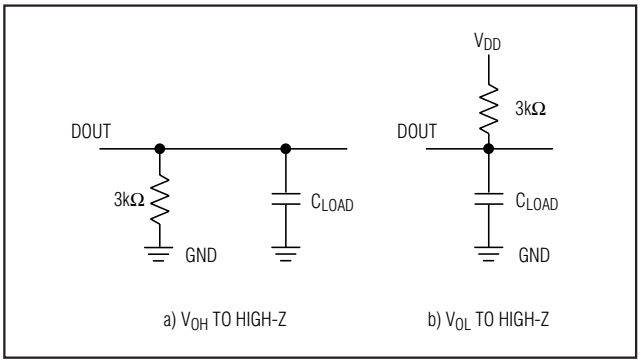


Figure 2. Load Circuits for Disable Time

Detailed Description

The MAX1115/MAX1116 ADCs use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to an 8-bit digital output. The SPI/QSPI/MICROWIRE-compatible interface directly connects to microprocessors (µPs) without additional circuitry (Figure 3).

Track/Hold

The input architecture of the ADC is illustrated in the equivalent-input circuit shown in Figure 4 and is composed of the T/H, input multiplexer, input comparator, switched capacitor DAC, and auto-zero rail.

The acquisition interval begins with the falling edge of CNVST. During the acquisition interval, the analog input (CH0) is connected to the hold capacitor (C_{HOLD}). Once the acquisition is complete, the T/H switch opens and C_{HOLD} is connected to GND, which retains the charge on C_{HOLD} as a sample of the signal at the analog input.

Sufficiently low source impedance is required to ensure an accurate sample. A source impedance of <1.5kΩ is recommended for accurate sample settling. A 100pF capacitor at the ADC inputs also improves the accuracy of an input sample.

Conversion Process

The MAX1115/MAX1116 conversion process is internally timed. The total acquisition and conversion process takes <7.5µs. Once an input sample has been acquired, the comparator's negative input is then connected to an auto-zero supply. Since the device requires only a single supply, the negative input of the comparator is set to equal $V_{DD}/2$. The capacitive DAC restores the positive input to $V_{DD}/2$ within the limits of 8-bit resolution. This action is equivalent to transferring a charge $Q_{IN} = 16pF \times V_{IN}$ from C_{HOLD} to the binary-weighted capacitive DAC, which forms a digital representation of the analog-input signal.

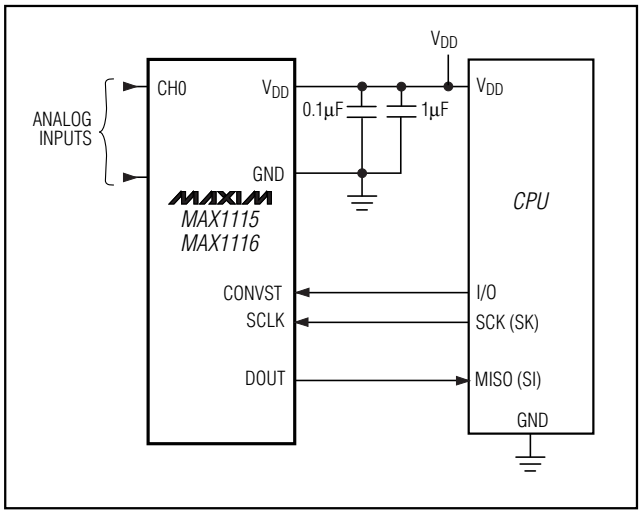


Figure 3. Typical Operating Circuit

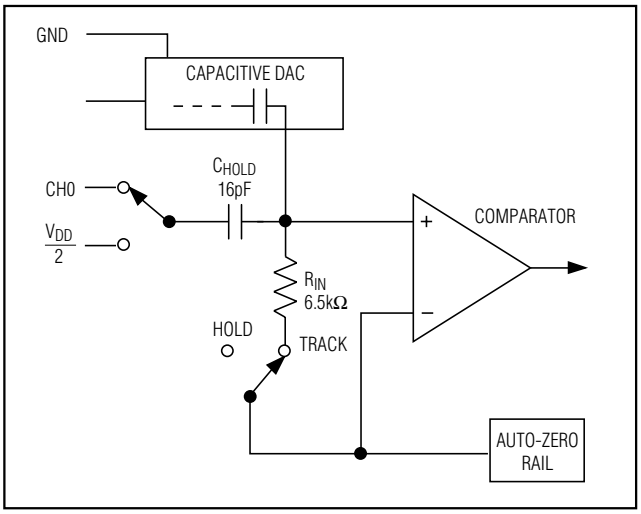


Figure 4. Equivalent Input Circuit

Input Voltage Range

Internal protection diodes that clamp the analog input to V_{DD} and GND allow the input pin (CH0) to swing from (GND - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions, the inputs must not exceed (V_{DD} + 50mV) or be less than (GND - 50mV).

Input Bandwidth

The ADC's input tracking circuitry has a 4MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Anti-alias filtering is recommended to avoid high-frequency signals being aliased into the frequency band of interest.

Serial Interface

The MAX1115/MAX1116 have a 3-wire serial interface. The CNVST and SCLK inputs are used to control the device, while the three-state DOUT pin is used to access the conversion results.

The serial interface provides connection to microcontrollers (µCs) with SPI, QSPI, and MICROWIRE serial interfaces at clock rates up to 5MHz. The interface supports either an idle high or low SCLK format. For SPI and QSPI, set CPOL = CPHA = 0 or CPOL = CPHA = 1 in the SPI control registers of the µC. Figure 5 shows the MAX1115/MAX1116 common serial-interface connections. See Figures 6a–6d for details on the serial-interface timing and protocol.

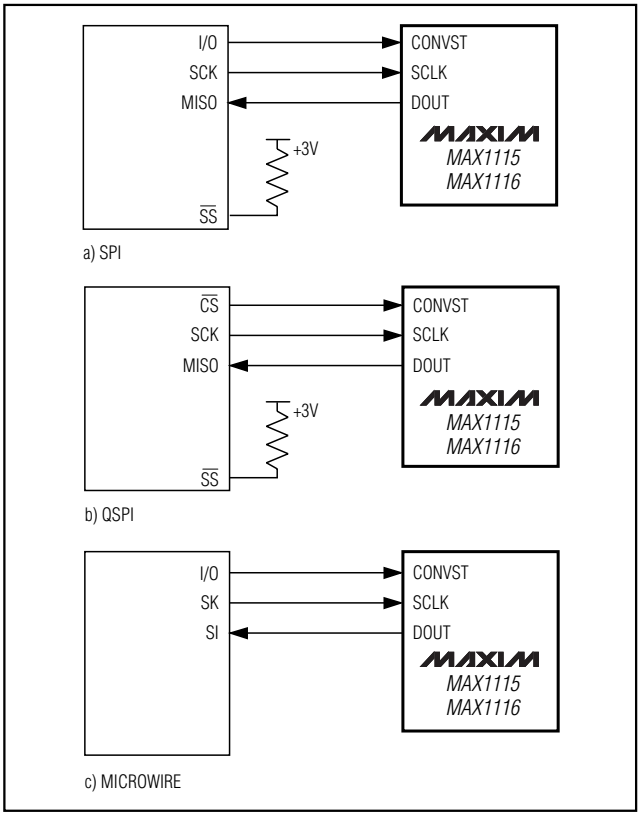


Figure 5. Common Serial-Interface Connections

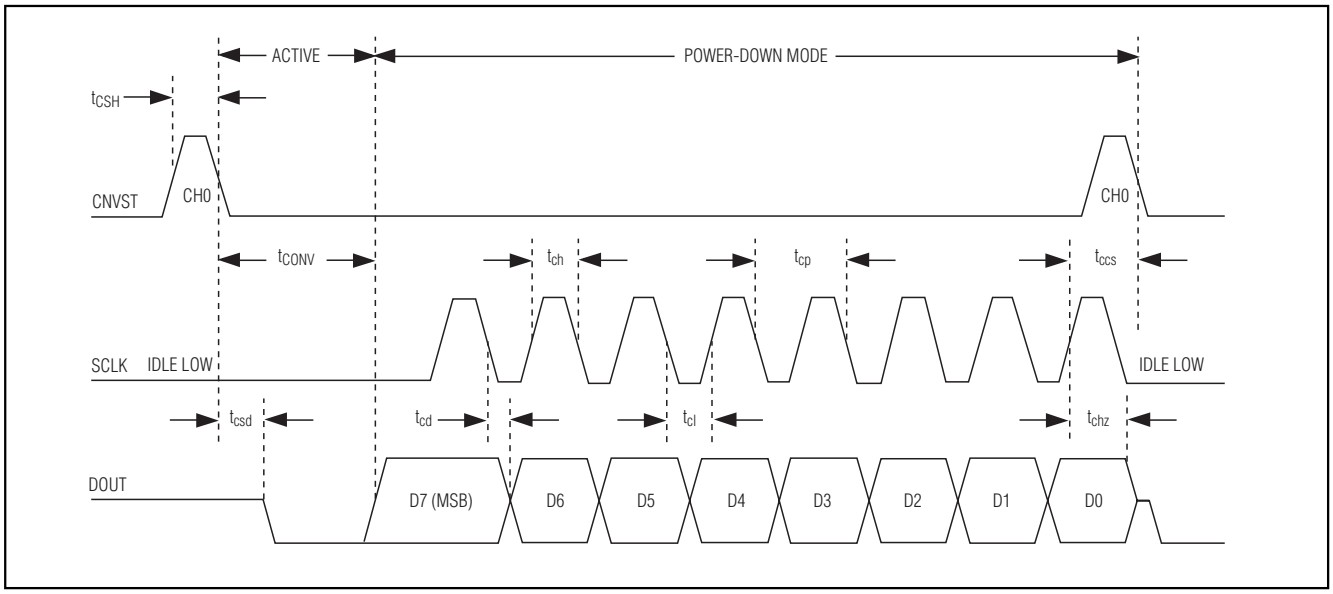


Figure 6a. Conversion and Interface Timing, Conversion on CH0 with SCLK Idle Low

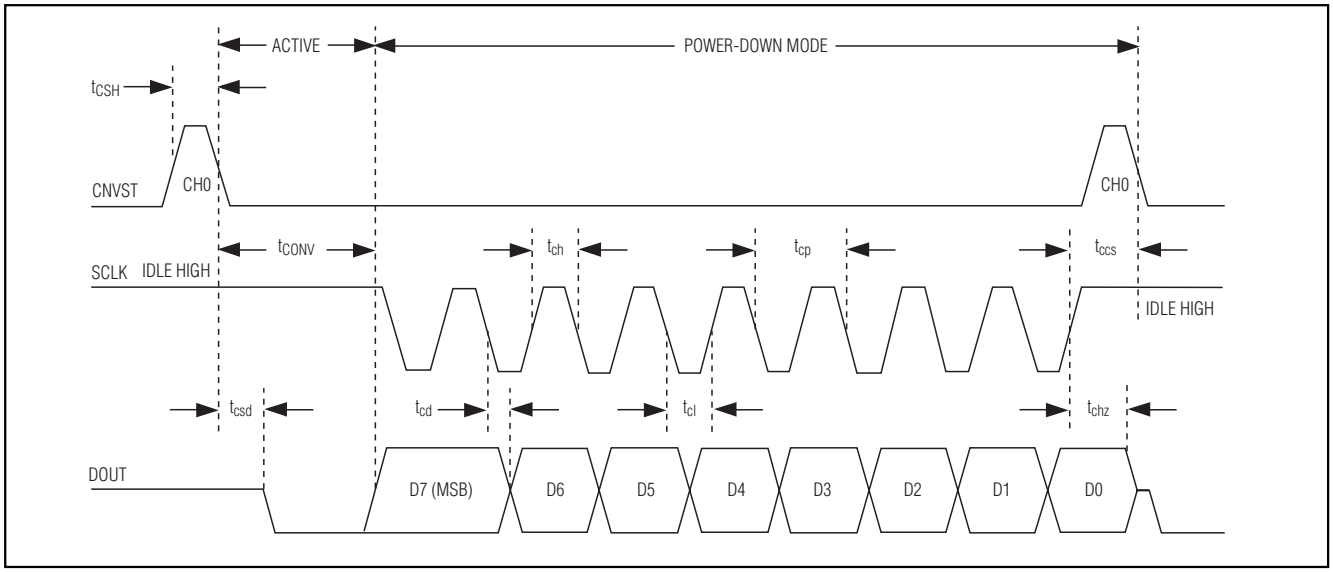


Figure 6b. Conversion and Interface Timing, Conversion on CH0 with SCLK Idle High

Digital Inputs and Outputs

The MAX1115/MAX1116 perform conversions by using an internal clock. This frees the µP from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the µP's convenience at any clock rate up to 5MHz.

The acquisition interval begins with the falling edge of CNVST. CNVST can idle between conversions in either a high or low state. If idled in a low state, CNVST must be brought high for at least 50ns, then brought low to initiate a conversion. To select $V_{DD}/2$ for conversion, the CNVST pin must be brought high and low for a second time (Figures 6c and 6d).

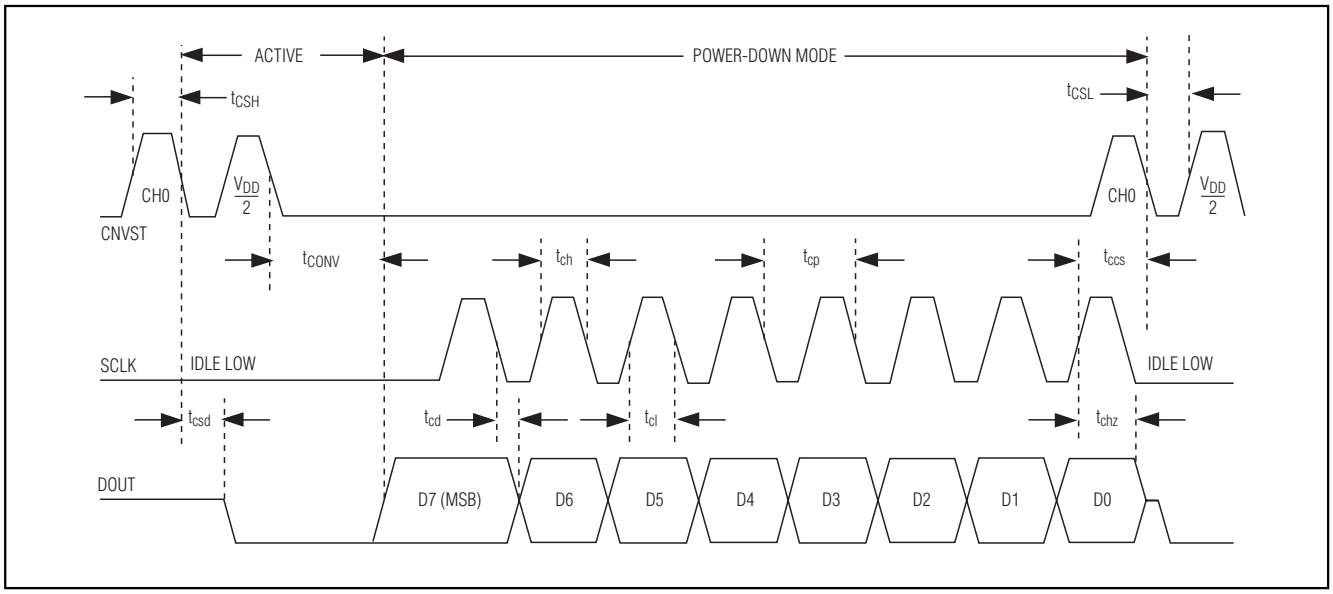


Figure 6c. Conversion and Interface Timing, Conversion on V_{DD} / 2 with SCLK Idle Low

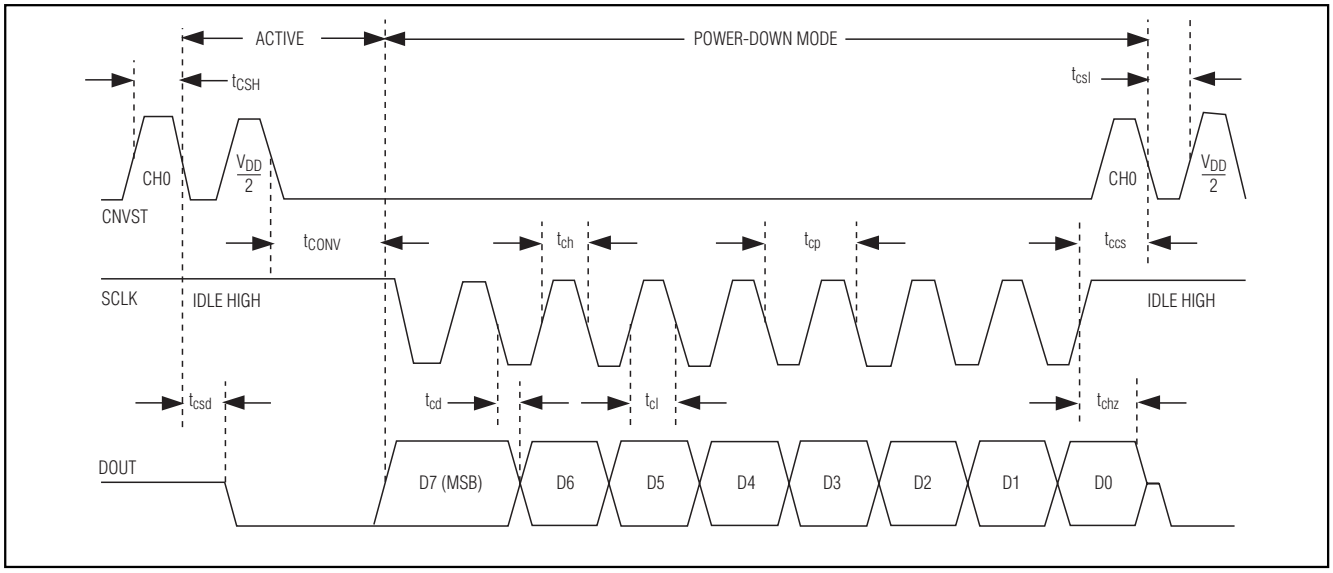


Figure 6d. Conversion and Interface Timing, Conversion on V_{DD} / 2 with SCLK Idle High

After CNVST is brought low, allow 7.5µs for the conversion to be completed. While the internal conversion is in progress, DOUT is low. The MSB is present at the DOUT pin immediately after conversion is completed. The conversion result is clocked out at the DOUT pin and is coded in straight binary (Figure 7). Data is clocked out at SCLK's falling edge in MSB-first format at rates up to 5MHz. Once all data bits are clocked out, DOUT goes high impedance (100ns to 500ns after the rising edge) of the eighth SCLK pulse.

SCLK is ignored during the conversion process. Only after a conversion is complete will SCLK cause serial data to be output. Falling edges on CNVST during an

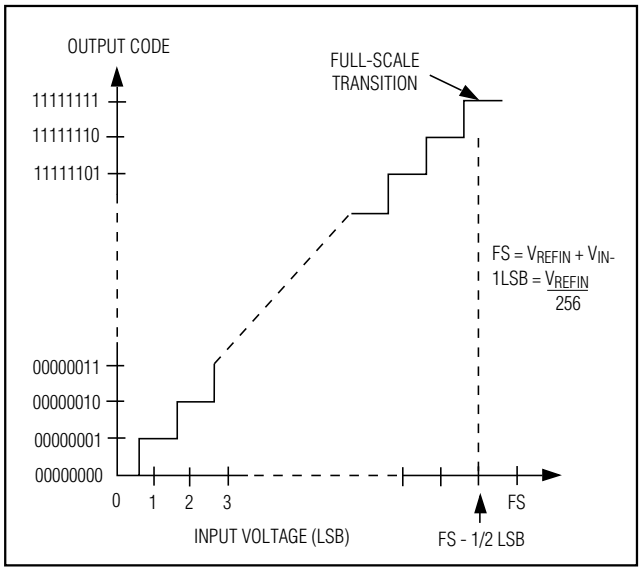


Figure 7. Input/Output Transfer Function

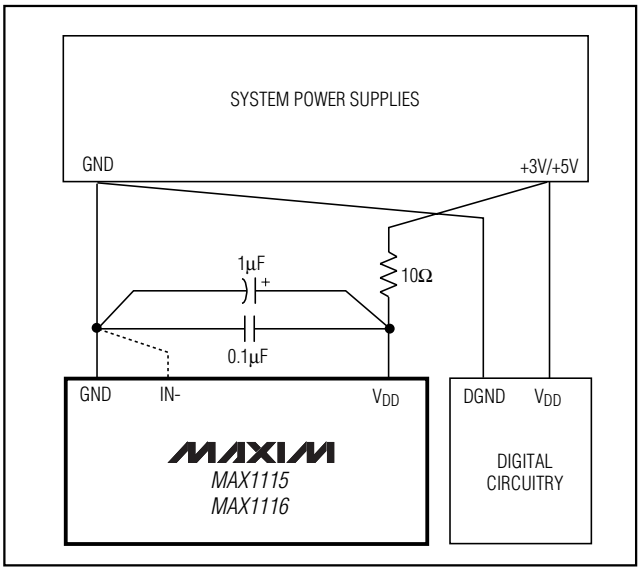


Figure 8. Power-Supply Connections

active conversion process interrupt the current conversion and cause the input multiplexer to switch to $V_{DD}/2$. To reinitiate a conversion on CH0, it is necessary to allow for a conversion to be complete and all of the data to be read out. Once a conversion has been completed, the MAX1115/MAX1116 goes into Autoshutdown mode (typically <1µA) until the next conversion is initiated.

Applications Information

Power-On Reset

When power is first applied, the MAX1115/MAX1116 are in AutoShutdown (typically <1µA). A conversion can be started by toggling CNVST high to low. Powering up the MAX1115/MAX1116 with CNVST low does not start a conversion.

AutoShutdown and Supply Current Requirements

The MAX1115/MAX1116 are designed to automatically shutdown once a conversion is complete, without any external control. An input sample and conversion process typically takes 5µs to complete, during which time the supply current to the analog sections of the device are fully on. All analog circuitry is shutdown after a conversion completes, which results in a supply current of <1µA (see *Shutdown Current vs. Supply Voltage* plot in the *Typical Operating Characteristics* section). The digital conversion result is maintained in a static register and is available for access through the serial interface at any time.

The power consumption consequence of this architecture is dramatic when relatively slow conversion rates are needed. For example, at a conversion rate of 10ksps, the average supply current for the MAX1115 is 15µA, while at 1ksps it drops to 15µA. At 0.1ksps it is just 0.3µA, or a miniscule 1µW of power consumption (see *Average Supply Current vs. Conversion Rate* plot in the *Typical Operating Characteristics* sections).

Transfer Function

Figure 7 depicts the input/output transfer function. Output coding is binary with a +2.048V reference, 1LSB = 8mV(V_{REF}/256).

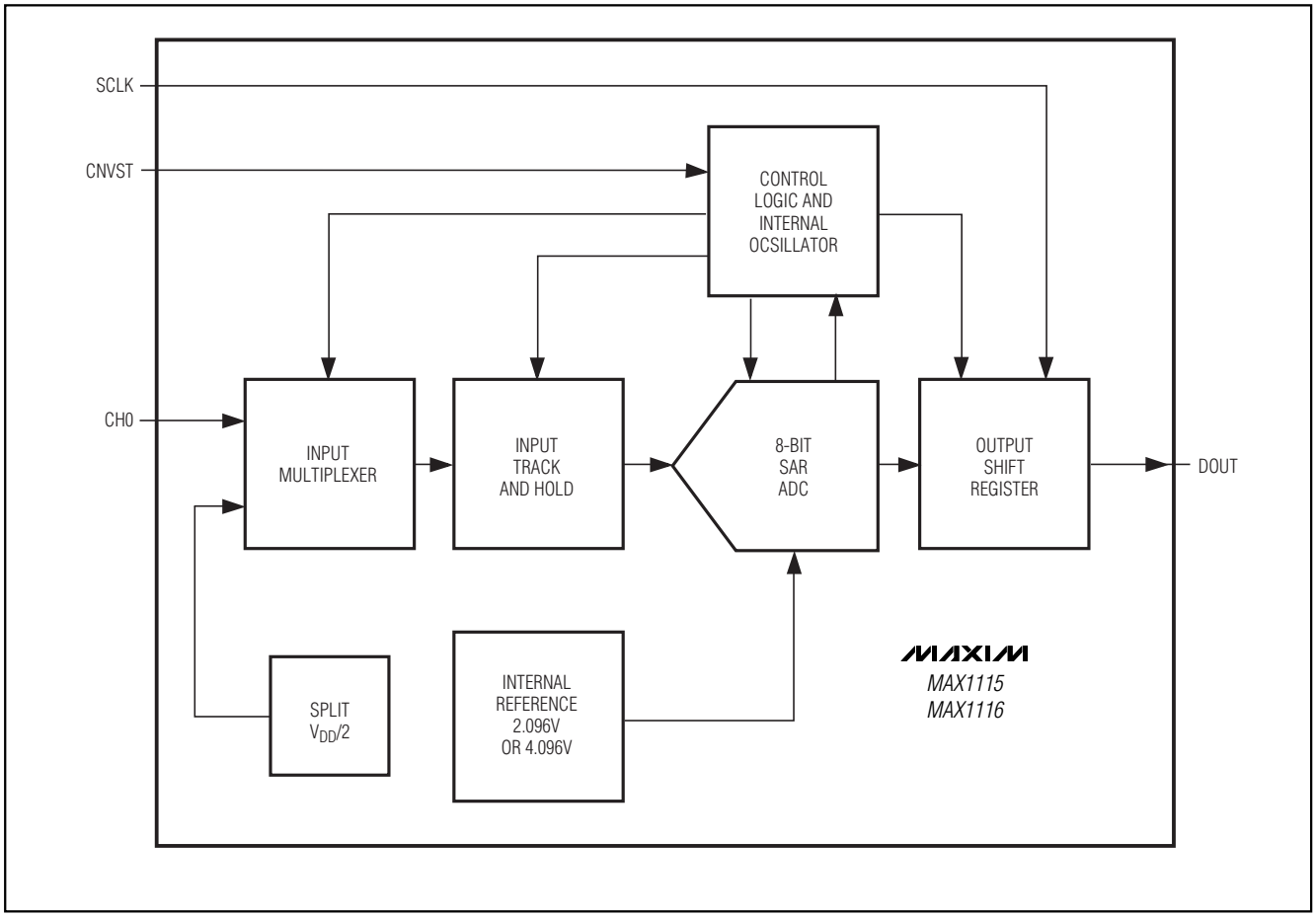
Layout, Grounding, and Bypassing

For best performance, board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or run digital lines underneath the ADC package.

Figure 8 shows the recommended system-ground connections. A single-point analog ground (star-ground point) should be established at the ADC ground. Connect all analog grounds to the star-ground. The ground-return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply can affect the comparator in the ADC. Bypass the supply to the star ground with a 0.1µF capacitor close to the V_{DD} pin of the MAX1115/MAX1116. Minimize capacitor lead

Functional Diagram



lengths for best supply-noise rejection. If the power supply is noisy, a 0.1µF capacitor in conjunction with a 10Ω series resistor can be connected to form a low-pass filter.

Chip Information

TRANSISTOR COUNT: 2000

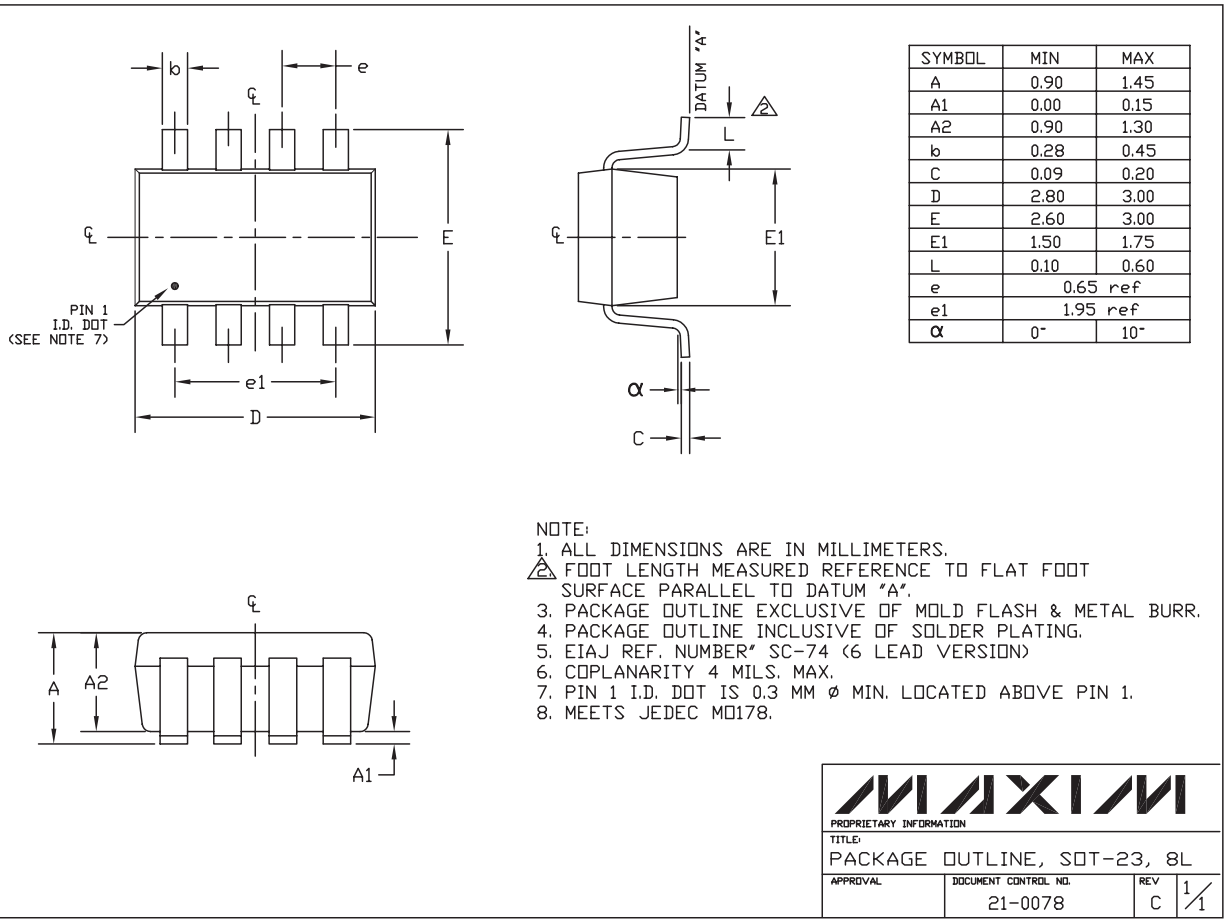
PROCESS: BiCMOS

Single-Supply, Low-Power, Serial 8-Bit ADCs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOT23, 8L.EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
8. MEETS JEDEC MO178.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SOT-23, 8L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0078	C	1/1