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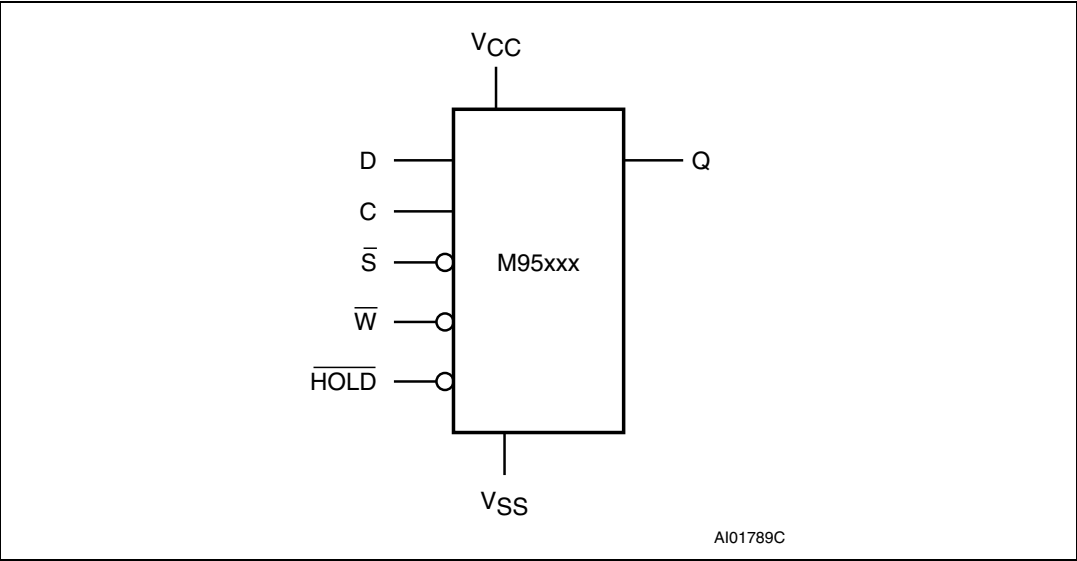
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# 1 Description

The M95640 devices are Electrically Erasable PROgrammable Memories (EEPROMs) organized as 8192 x 8 bits, accessed through the SPI bus.

The M95640 devices can operate with a supply range from 2.5 V up to 5.5 V, and are guaranteed over the -40 °C/+125 °C temperature range. They are compliant with the Automotive standard AEC-Q100 Grade 1.

Figure 1. Logic diagram

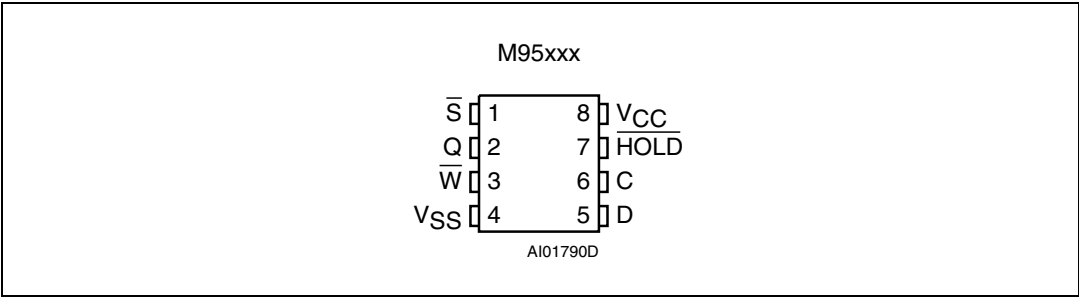


The SPI bus signals are C, D and Q, as shown in [Figure 1](#) and [Table 1](#). The device is selected when Chip Select ( $\overline{S}$ ) is driven low. Communications with the device can be interrupted when the  $\overline{HOLD}$  is driven low.

Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data Input	Input
Q	Serial Data Output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V <sub>CC</sub>	Supply voltage	
V <sub>SS</sub>	Ground	

Figure 2. 8-pin package connections (top view)

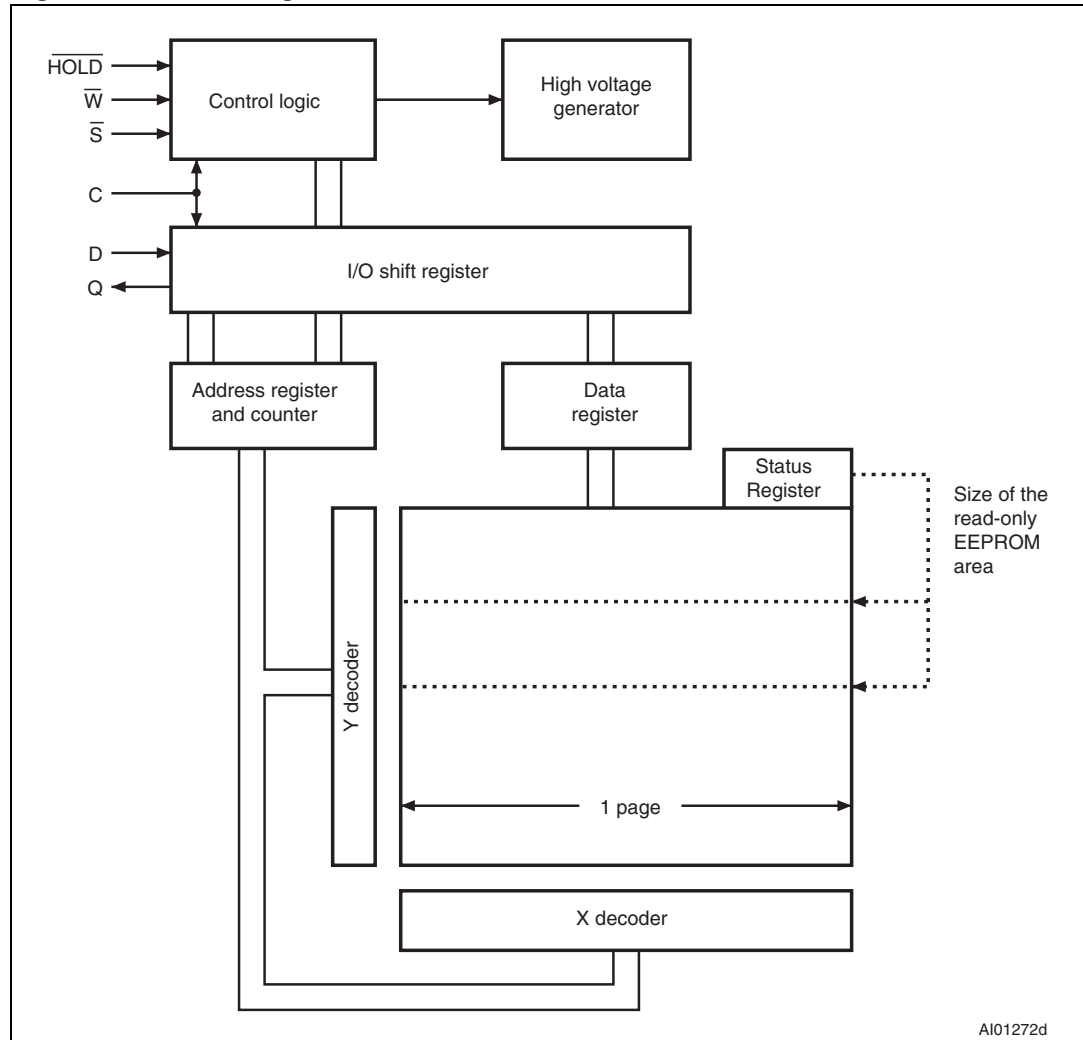


1. See [Section 10: Package mechanical data](#) section for package dimensions, and how to identify pin 1.

## 2 Memory organization

The memory is organized as shown in the following figure.

**Figure 3. Block diagram**



## 3 Signal description

During all operations,  $V_{CC}$  must be held stable and within the specified valid range:  $V_{CC}(\min)$  to  $V_{CC}(\max)$ .

All of the input and output signals must be held high or low (according to voltages of  $V_{IH}$ ,  $V_{OH}$ ,  $V_{IL}$  or  $V_{OL}$ , as specified in [Section 9: DC and AC parameters](#)). These signals are described next.

### 3.1 Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

### 3.2 Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

### 3.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) change from the falling edge of Serial Clock (C).

### 3.4 Chip Select ( $\overline{S}$ )

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. The device is in the Standby Power mode, unless an internal Write cycle is in progress. Driving Chip Select ( $\overline{S}$ ) low selects the device, placing it in the Active Power mode.

After power-up, a falling edge on Chip Select ( $\overline{S}$ ) is required prior to the start of any instruction.

### 3.5 Hold ( $\overline{HOLD}$ )

The Hold ( $\overline{HOLD}$ ) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ( $\overline{S}$ ) driven low.



### 3.6 Write Protect ( $\overline{W}$ )

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all Write instructions.

### 3.7 $V_{CC}$ supply voltage

$V_{CC}$  is the supply voltage.

### 3.8 $V_{SS}$ ground

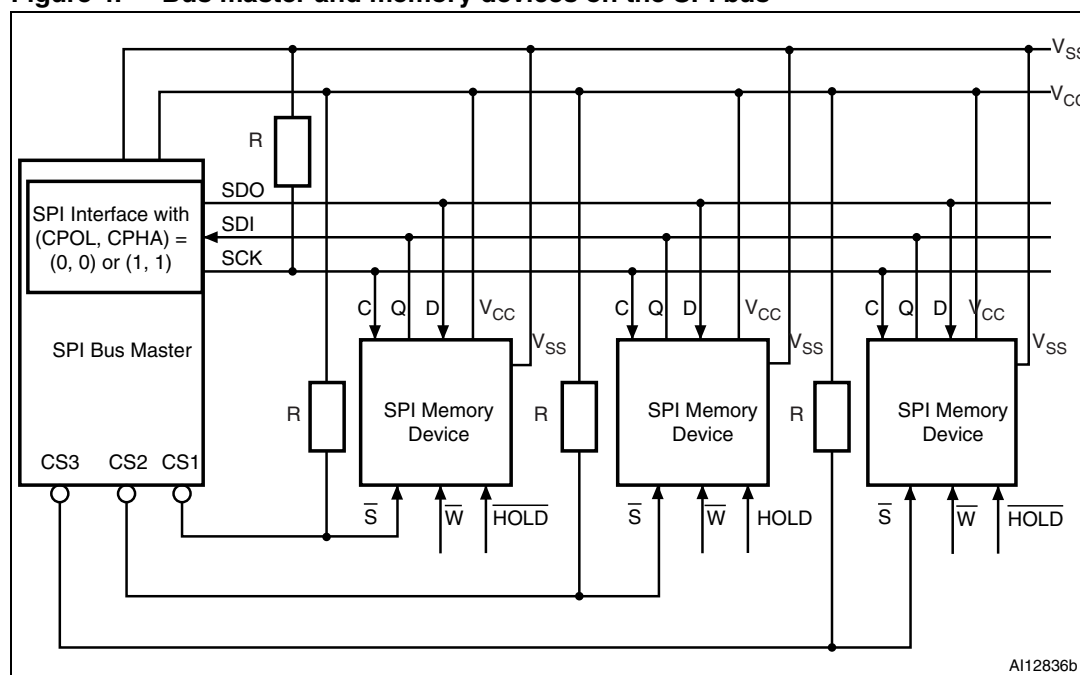
$V_{SS}$  is the reference for all signals, including the  $V_{CC}$  supply voltage.

## 4 Connecting to the SPI bus

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ( $\overline{S}$ ) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

**Figure 4. Bus master and memory devices on the SPI bus**



1. The Write Protect ( $\overline{W}$ ) and Hold ( $\overline{HOLD}$ ) signals should be driven, high or low as appropriate.

*Figure 4* shows an example of three memory devices connected to an SPI bus master. Only one memory device is selected at a time, so only one memory device drives the Serial Data Output (Q) line at a time. The other memory devices are high impedance.

The pull-up resistor R (represented in *Figure 4*) ensures that a device is not selected if the Bus Master leaves the  $\overline{S}$  line in the high impedance state.

In applications where the Bus Master may leave all SPI bus lines in high impedance at the same time (for example, if the Bus Master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the  $\overline{S}$  line is pulled high): this ensures that  $\overline{S}$  and C do not become high at the same time, and so, that the  $t_{SHCH}$  requirement is met. The typical value of R is 100 k $\Omega$ .

## 4.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

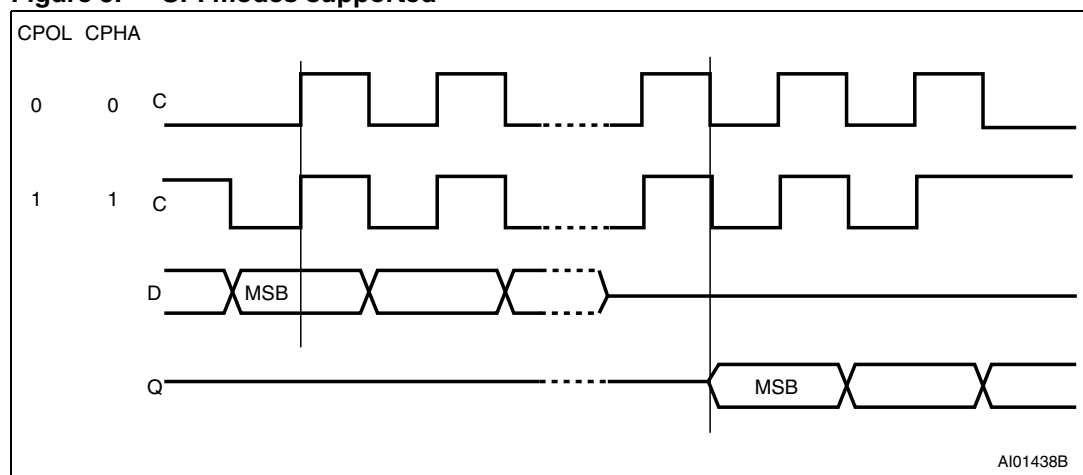
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in [Figure 5](#), is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

**Figure 5. SPI modes supported**



## 5 Operating features

### 5.1 Supply voltage ( $V_{CC}$ )

#### 5.1.1 Operating supply voltage $V_{CC}$

Prior to selecting the memory and issuing instructions to it, a valid and stable  $V_{CC}$  voltage within the specified [ $V_{CC}(\min)$ ,  $V_{CC}(\max)$ ] range must be applied (see Operating conditions in [Section 9: DC and AC parameters](#)). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle ( $t_W$ ). In order to secure a stable DC supply voltage, it is recommended to decouple the  $V_{CC}$  line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the  $V_{CC}/V_{SS}$  device pins.

#### 5.1.2 Device reset

In order to prevent erroneous instruction decoding and inadvertent Write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until  $V_{CC}$  reaches the POR threshold voltage. This threshold is lower than the minimum  $V_{CC}$  operating voltage (see Operating conditions in [Section 9: DC and AC parameters](#)).

At power-up, when  $V_{CC}$  passes over the POR threshold, the device is reset and is in the following state:

- in Standby Power mode,
- deselected,
- Status Register values:
  - The Write Enable Latch (WEL) bit is reset to 0.
  - The Write In Progress (WIP) bit is reset to 0.
  - The SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).

It is important to note that the device must not be accessed until  $V_{CC}$  reaches a valid and stable level within the specified [ $V_{CC}(\min)$ ,  $V_{CC}(\max)$ ] range, as defined under Operating conditions in [Section 9: DC and AC parameters](#).

#### 5.1.3 Power-up conditions

When the power supply is turned on,  $V_{CC}$  rises continuously from  $V_{SS}$  to  $V_{CC}$ . During this time, the Chip Select ( $\overline{S}$ ) line is not allowed to float but should follow the  $V_{CC}$  voltage. It is therefore recommended to connect the  $\overline{S}$  line to  $V_{CC}$  via a suitable pull-up resistor (see [Figure 4](#)).

In addition, the Chip Select ( $\overline{S}$ ) input offers a built-in safety feature, as the  $\overline{S}$  input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ( $\overline{S}$ ). This ensures that Chip Select ( $\overline{S}$ ) must have been high, prior to going low to start the first operation.

The  $V_{CC}$  voltage has to rise continuously from 0 V up to the minimum  $V_{CC}$  operating voltage defined under Operating conditions in [Section 9: DC and AC parameters](#), and the rise time must not vary faster than 1 V/ $\mu$ s.

### 5.1.4 Power-down

During power-down (continuous decrease of the  $V_{CC}$  supply voltage below the minimum  $V_{CC}$  operating voltage defined under Operating conditions in [Section 9: DC and AC parameters](#)), the device must be:

- deselected (Chip Select  $\overline{S}$  should be allowed to follow the voltage applied on  $V_{CC}$ ),
- in Standby Power mode (there should not be any internal write cycle in progress).

## 5.2 Active Power and Standby Power modes

When Chip Select ( $\overline{S}$ ) is low, the device is selected, and in the Active Power mode. The device consumes  $I_{CC}$ .

When Chip Select ( $\overline{S}$ ) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes into the Standby Power mode, and the device consumption drops to  $I_{CC1}$ , as specified in DC characteristics (see [Section 9: DC and AC parameters](#)).

## 5.3 Hold condition

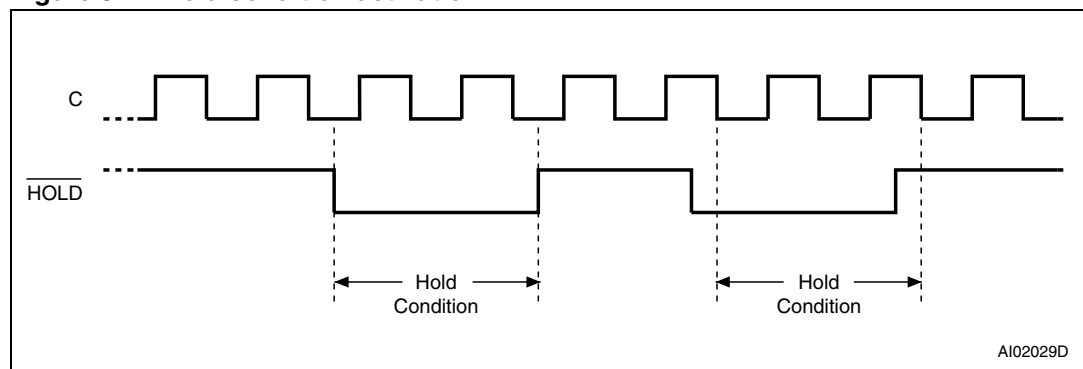
The Hold ( $\overline{HOLD}$ ) signal is used to pause any serial communications with the device without resetting the clocking sequence.

To enter the Hold condition, the device must be selected, with Chip Select ( $\overline{S}$ ) low.

During the Hold condition, the Serial Data Output (Q) is high impedance, and the Serial Data Input (D) and the Serial Clock (C) are Don't Care.

Normally, the device is kept selected for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition has the effect of resetting the state of the device, and this mechanism can be used if required to reset any processes that had been in progress.<sup>(a)(b)</sup>

**Figure 6. Hold condition activation**



The Hold condition starts when the Hold (HOLD) signal is driven low when Serial Clock (C) is already low (as shown in [Figure 6](#)).

- This resets the internal logic, except the WEL and WIP bits of the Status Register.
- In the specific case where the device has shifted in a Write command (Inst + Address + data bytes, each data byte being exactly 8 bits), deselecting the device also triggers the Write cycle of this decoded command.

The Hold condition ends when the Hold (HOLD) signal is driven high when Serial Clock (C) is already low.

[Figure 6](#) also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

## 5.4 Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See [Section 6.3: Read Status Register \(RDSR\)](#) for a detailed description of the Status Register bits.

## 5.5 Data protection and protocol control

The device features the following data protection mechanisms:

- Before accepting the execution of the Write and Write Status Register instructions, the device checks whether the number of clock pulses comprised in the instructions is a multiple of eight.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit.
- The Block Protect (BP1, BP0) bits in the Status Register are used to configure part of the memory as read-only.
- The Write Protect ( $\overline{WP}$ ) signal is used to protect the Block Protect (BP1, BP0) bits in the Status Register.

For any instruction to be accepted, and executed, Chip Select ( $\overline{CS}$ ) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points should be noted in the previous sentence:

- The “last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The “next rising edge of Serial Clock (C)” might (or might not) be the next bus transaction for some other device on the SPI bus.

**Table 2. Write-protected block size**

Status Register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	none	none
0	1	Upper quarter	1800h - 1FFFh
1	0	Upper half	1000h - 1FFFh
1	1	Whole memory	0000h - 1FFFh

# 6 Instructions

Each instruction starts with a single-byte code, as summarized in [Table 3](#).  
If an invalid instruction is sent (one not contained in [Table 3](#)), the device automatically deselects itself.

Table 3. Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

Table 4. Address range bits

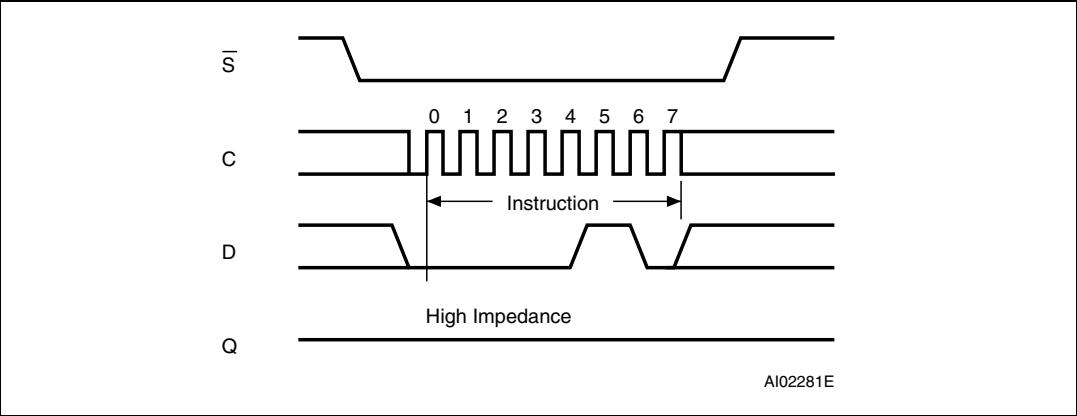
Address significant bits	A12-A0 <sup>(1)</sup>
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1. Upper MSBs are Don't Care.

## 6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.  
As shown in [Figure 7](#), to send this instruction to the device, Chip Select ( $\overline{S}$ ) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for the device to be deselected, by Chip Select ( $\overline{S}$ ) being driven high.

Figure 7. Write Enable (WREN) sequence



## 6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

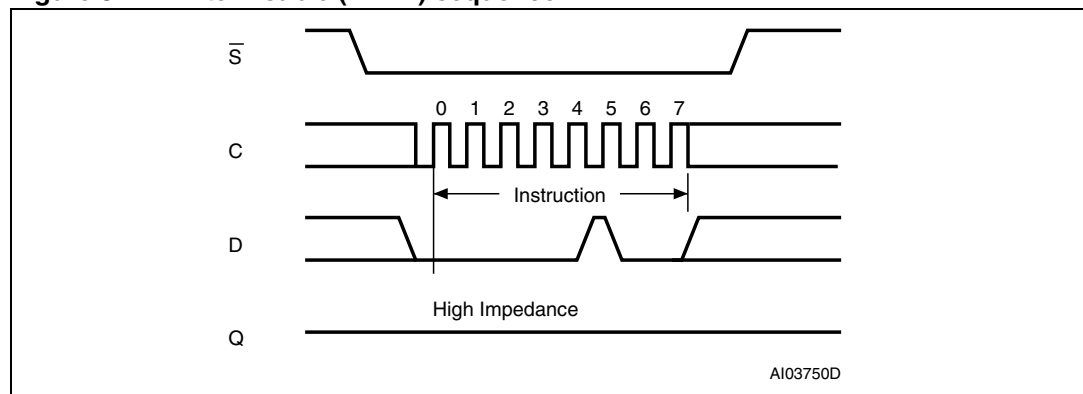
As shown in [Figure 8](#), to send this instruction to the device, Chip Select ( $\overline{S}$ ) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for the device to be deselected, by Chip Select ( $\overline{S}$ ) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

**Figure 8. Write Disable (WRDI) sequence**

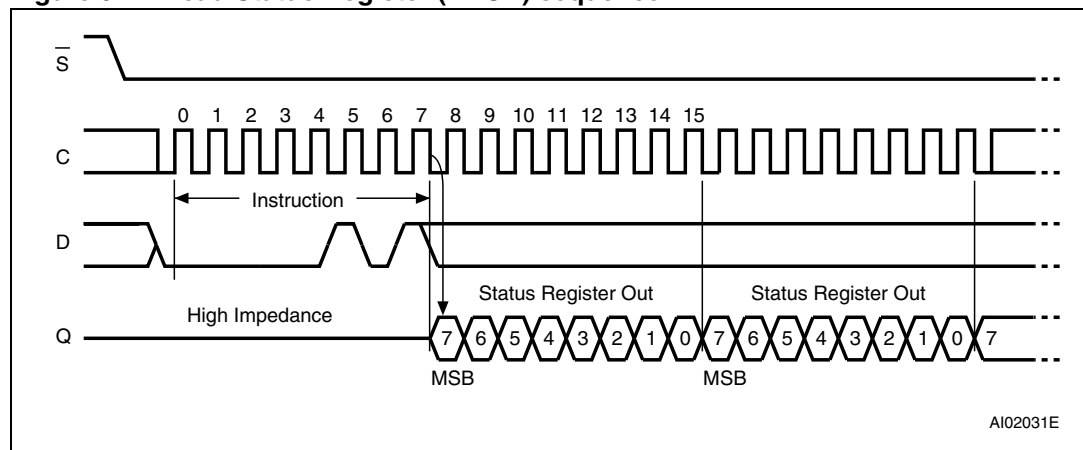




### 6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction is used to read the Status Register. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in [Figure 9](#).

**Figure 9. Read Status Register (RDSR) sequence**



The status and control bits of the Status Register are as follows:

#### 6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0, no such cycle is in progress.

#### 6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set. When set to 0, the internal Write Enable Latch is reset, and no Write or Write Status Register instruction is accepted.

The WEL bit is returned to its reset state by the following events:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Write (WRITE) instruction completion

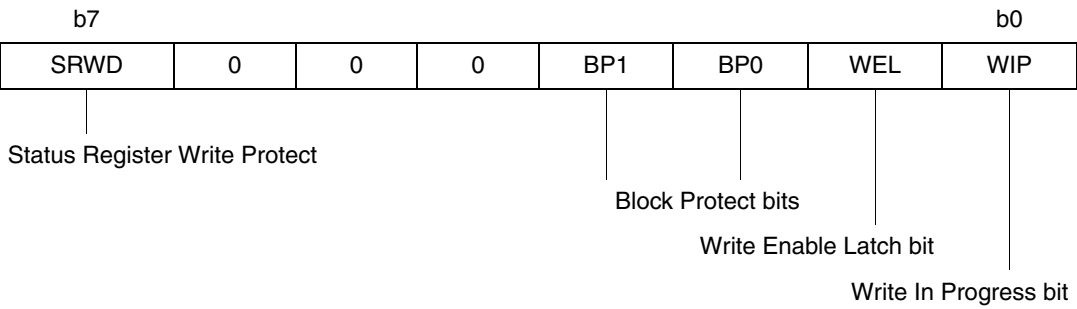
#### 6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non volatile. They define the size of the area to be software-protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in [Table 5](#)) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ( $\overline{W}$ ) signal. The Status Register Write Disable (SRWD) bit and Write Protect ( $\overline{W}$ ) signal enable the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ( $\overline{W}$ ) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 5. Status Register format



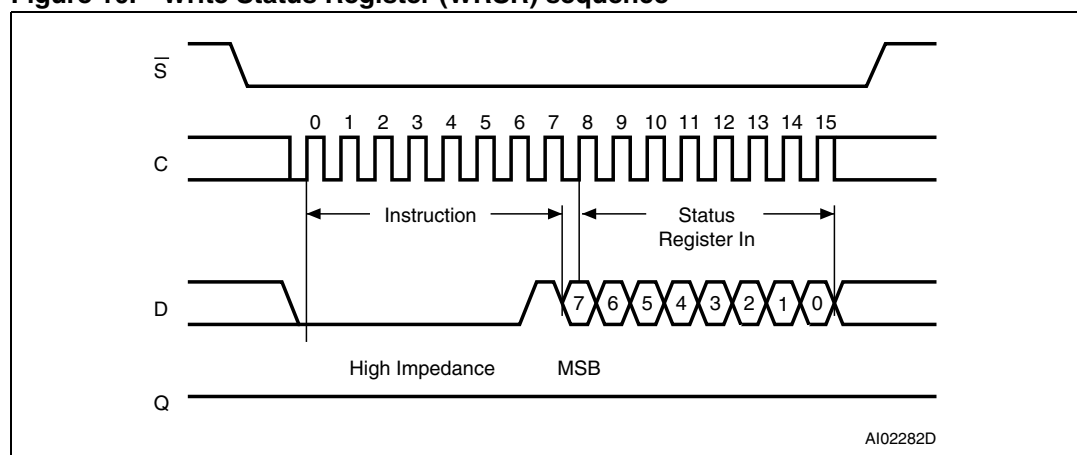
## 6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction is used to write new values to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must have been previously executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ( $\overline{S}$ ) low, followed by the instruction code, the data byte on Serial Data input (D) and Chip Select ( $\overline{S}$ ) driven high. Chip Select ( $\overline{S}$ ) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed.

The instruction sequence is shown in [Figure 10](#).

**Figure 10. Write Status Register (WRSR) sequence**



Driving the Chip Select ( $\overline{S}$ ) signal high at a byte boundary of the input data triggers the self-timed Write cycle that takes  $t_{WV}$  to complete (as specified in AC tables under [Section 9: DC and AC parameters](#)).

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed Write cycle  $t_{WV}$ , and 0 when the Write cycle is complete. The WEL bit (Write Enable Latch) is also reset at the end of the Write cycle  $t_{WV}$ .

The Write Status Register (WRSR) instruction enables the user to change the values of the BP1, BP0 and SRWD bits:

- The Block Protect (BP1, BP0) bits define the size of the area that is to be treated as read-only, as defined in [Table 2](#).
- The SRWD (Status Register Write Disable) bit, in accordance with the signal read on the Write Protect pin ( $\overline{W}$ ), enables the user to set or reset the Write protection mode of the Status Register itself, as defined in [Table 6](#). When in Write-protected mode, the Write Status Register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the  $t_{WV}$  Write cycle.

The Write Status Register (WRSR) instruction has no effect on the b6, b5, b4, b1, b0 bits in the Status Register. Bits b6, b5, b4 are always read as 0.

**Table 6. Protection modes**

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area <sup>(1)</sup>	Unprotected area <sup>(1)</sup>
1	0	Software-protected (SPM)	Status Register is writable (if the WREN instruction has set the WEL bit). The values in the BP1 and BP0 bits can be changed.	Write-protected	Ready to accept Write instructions
0	0				
1	1	Hardware-protected (HPM)	Status Register is Hardware write-protected. The values in the BP1 and BP0 bits cannot be changed.	Write-protected	Ready to accept Write instructions
0	1				

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register. See [Table 2](#).

The protection features of the device are summarized in [Table 6](#).

When the Status Register Write Disable (SRWD) bit in the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction), regardless of the logic level applied on the Write Protect ( $\overline{W}$ ) input pin.

When the Status Register Write Disable (SRWD) bit in the Status Register is set to 1, two cases should be considered, depending on the state of the Write Protect ( $\overline{W}$ ) input pin:

- If Write Protect ( $\overline{W}$ ) is driven high, it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction).
- If Write Protect ( $\overline{W}$ ) is driven low, it is not possible to write to the Status Register even if the WEL bit has previously been set by a WREN instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area, which are Software-protected (SPM) by the Block Protect (BP1, BP0) bits in the Status Register, are also hardware-protected against data modification.

Regardless of the order of the two events, the Hardware-protected mode (HPM) can be entered by:

- either setting the SRWD bit after driving the Write Protect ( $\overline{W}$ ) input pin low,
- or driving the Write Protect ( $\overline{W}$ ) input pin low after setting the SRWD bit.

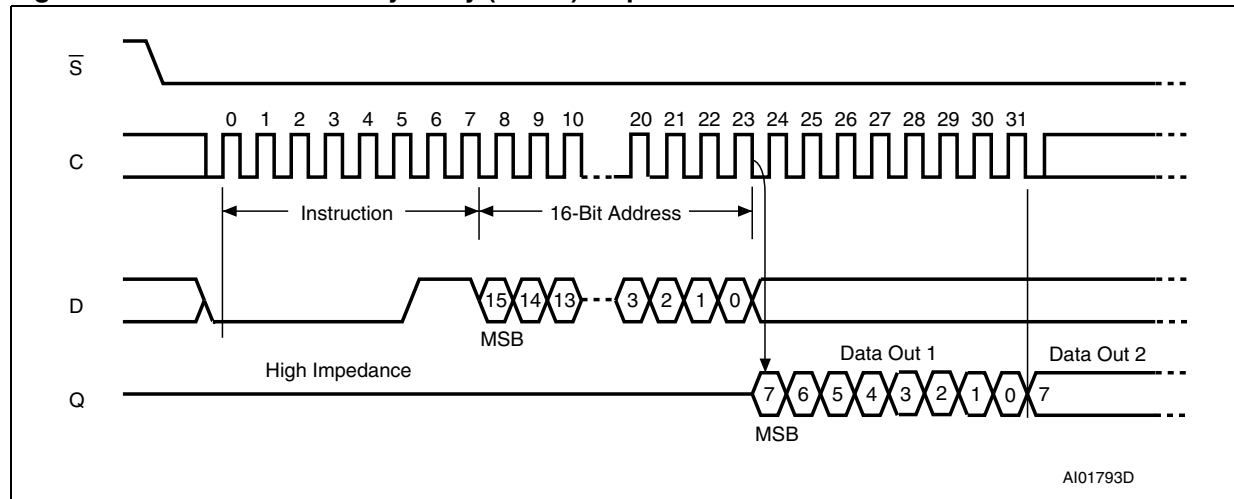
Once the Hardware-protected mode (HPM) has been entered, the only way of exiting it is to pull high the Write Protect ( $\overline{W}$ ) input pin.

If the Write Protect ( $\overline{W}$ ) input pin is permanently tied high, the Hardware-protected mode (HPM) can never be activated, and only the Software-protected mode (SPM), using the Block Protect (BP1, BP0) bits in the Status Register, can be used.

## 6.5 Read from Memory Array (READ)

As shown in [Figure 11](#), to send this instruction to the device, Chip Select ( $\overline{S}$ ) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

**Figure 11. Read from Memory Array (READ) sequence**



1. Depending on the memory size, as shown in [Table 4](#), the most significant address bits are Don't Care.

If Chip Select ( $\overline{S}$ ) continues to be driven low, the internal address register is incremented automatically, and the byte of data at the new address is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ( $\overline{S}$ ) high. The rising edge of the Chip Select ( $\overline{S}$ ) signal can occur at any time during the cycle.

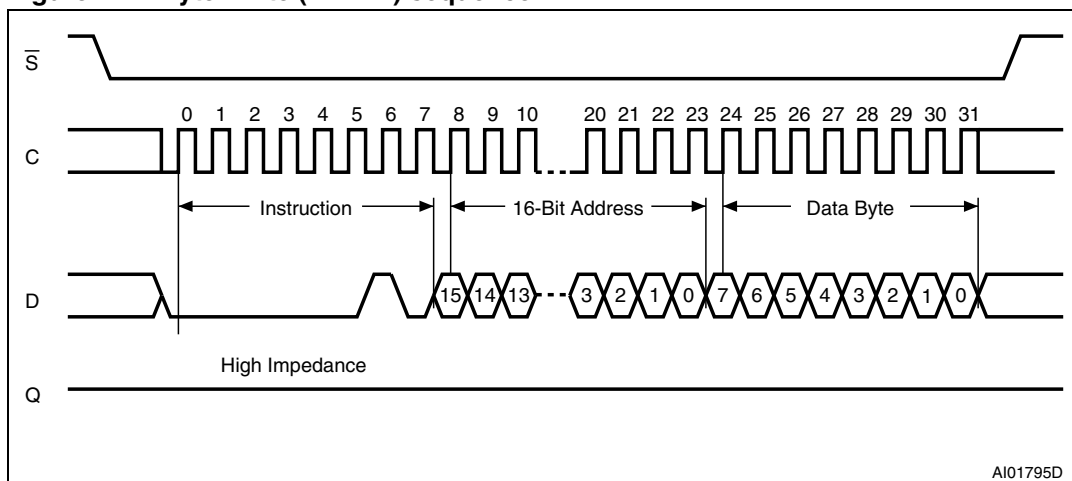
The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

## 6.6 Write to Memory Array (WRITE)

As shown in [Figure 12](#), to send this instruction to the device, Chip Select ( $\overline{S}$ ) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ( $\overline{S}$ ) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the Chip Select ( $\overline{S}$ ) rising edge, continues for a period  $t_W$  (as specified in AC characteristics in [Section 9: DC and AC parameters](#)), at the end of which the Write in Progress (WIP) bit is reset to 0.

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in [Table 4](#), the most significant address bits are Don't Care.

In the case of [Figure 12](#), Chip Select ( $\overline{S}$ ) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. However, if Chip Select ( $\overline{S}$ ) continues to be driven low, as shown in [Figure 13](#), the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

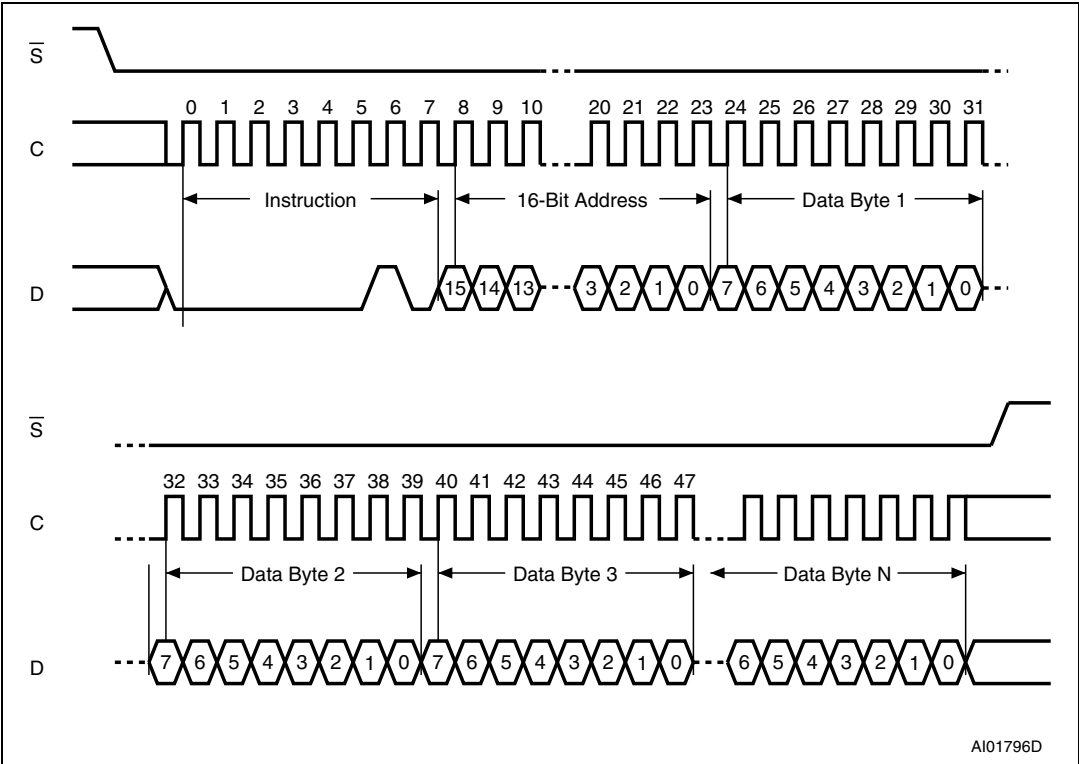
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 32 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before),
- if a Write cycle is already in progress,
- if the device has not been deselected, by driving high Chip Select ( $\overline{S}$ ), at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in),
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

**Note:** The self-timed write cycle  $t_{W}$  is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in [Table 4](#), the most significant address bits are Don't Care.

## 7 Power-up and delivery state

### 7.1 Power-up state

After power-up, the device is in the following state:

- Standby power mode,
- deselected (after power-up, a falling edge is required on Chip Select ( $\overline{S}$ ) before any instructions can be started),
- not in the Hold condition,
- the Write Enable Latch (WEL) is reset to 0,
- Write In Progress (WIP) is reset to 0.

The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

### 7.2 Initial delivery state

The device is delivered with the memory array set to all 1s (each byte = FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.



## 8 Maximum rating

Stressing the device outside the ratings listed in [Table 7](#) may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute maximum ratings**

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	−40	130	°C
T <sub>STG</sub>	Storage temperature	−65	150	°C
T <sub>LEAD</sub>	Lead temperature during soldering	See note <sup>(1)</sup>		°C
V <sub>O</sub>	Output voltage	−0.50	V <sub>CC</sub> +0.6	V
V <sub>I</sub>	Input voltage	−0.50	6.5	V
V <sub>CC</sub>	Supply voltage	−0.50	6.5	V
I <sub>OL</sub>	DC output current (Q = 0)		5	mA
I <sub>OH</sub>	DC output current (Q = 1)		5	mA
V <sub>ESD</sub>	Electrostatic discharge voltage (human body model) <sup>(2)</sup>		4000	V

1. Compliant with JEDEC Std J-STD-020 (for small body, Sn-Pb or Pb assembly), with the ST ECOPACK® 7191395 specification, and with the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. Positive and negative pulses applied on pin pairs, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω).

## 9 DC and AC parameters

This section summarizes the operating conditions and the DC/AC characteristics of the device.

**Table 8. Operating conditions (M95640, device grade 3)**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply voltage	4.5	5.5	V
$T_A$	Ambient operating temperature	-40	125	°C

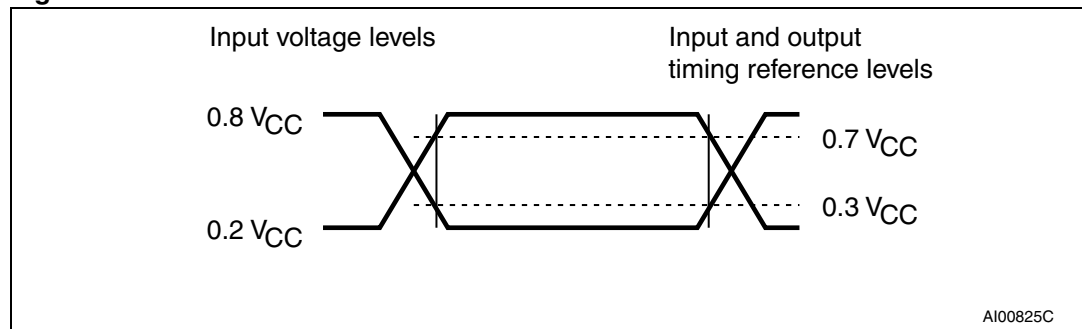
**Table 9. Operating conditions (M95640-W, device grade 3)**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply voltage	2.5	5.5	V
$T_A$	Ambient operating temperature	-40	125	°C

**Table 10. AC measurement conditions**

Symbol	Parameter	Min.	Max.	Unit
$C_L$	Load capacitance	30		pF
	Input rise and fall times		25	ns
	Input pulse voltages	0.2 $V_{CC}$ to 0.8 $V_{CC}$		V
	Input and output timing reference voltages	0.3 $V_{CC}$ to 0.7 $V_{CC}$		V

**Figure 14. AC measurement I/O waveform**



**Table 11. Capacitance**

Symbol	Parameter	Test condition <sup>(1)</sup>	Min.	Max.	Unit
$C_{OUT}$	Output capacitance (Q)	$V_{OUT} = 0$ V		8	pF
$C_{IN}$	Input capacitance (D)	$V_{IN} = 0$ V		8	pF
	Input capacitance (other pins)	$V_{IN} = 0$ V		6	pF

1. Sampled only, not 100% tested, at  $T_A = 25$  °C and a frequency of 5 MHz.

**Table 12. DC characteristics (M95640, device grade 3)**

Symbol	Parameter	Test conditions	Min.	Max.	Unit
$I_{LI}$	Input leakage current	$V_{IN} = V_{SS}$ or $V_{CC}$		$\pm 2$	$\mu A$
$I_{LO}$	Output leakage current	$\overline{S} = V_{CC}$ , $V_{OUT} = V_{SS}$ or $V_{CC}$		$\pm 2$	$\mu A$
$I_{CC}$	Supply current	$C = 0.1 V_{CC}/0.9 V_{CC}$ at 5 MHz, $V_{CC} = 5 V$ , $Q = \text{open}$		4	mA
		$C = 0.1 V_{CC}/0.9 V_{CC}$ at 10 MHz, $V_{CC} = 5 V$ , $Q = \text{open}$		8	
$I_{CC1}$	Supply current (Standby)	$\overline{S} = V_{CC}$ , $V_{CC} = 5 V$ , $V_{IN} = V_{SS}$ or $V_{CC}$		5	$\mu A$
$V_{IL}$	Input low voltage		-0.45	$0.3 V_{CC}$	V
$V_{IH}$	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
$V_{OL}^{(1)}$	Output low voltage	$I_{OL} = 2 \text{ mA}$ , $V_{CC} = 5 V$		0.4	V
$V_{OH}^{(1)}$	Output high voltage	$I_{OH} = -2 \text{ mA}$ , $V_{CC} = 5 V$	$0.8 V_{CC}$		V
$V_{RES}^{(2)}$	Internal reset threshold voltage		2.5	4.0	V

1. For all 5 V range devices, the device meets the output requirements for both TTL and CMOS standards.

2. Characterized only, not tested in production.

**Table 13. DC characteristics (M95640-W, device grade 3)**

Symbol	Parameter	Test conditions	Min.	Max.	Unit
$I_{LI}$	Input leakage current	$V_{IN} = V_{SS}$ or $V_{CC}$		$\pm 2$	$\mu A$
$I_{LO}$	Output leakage current	$\overline{S} = V_{CC}$ , $V_{OUT} = V_{SS}$ or $V_{CC}$		$\pm 2$	$\mu A$
$I_{CC}$	Supply current (Read)	$f_C = 5 \text{ MHz}$ , $V_{CC} = 2.5 \text{ V}$ , $C = 0.1 V_{CC}/0.9 V_{CC}$ , $Q = \text{open}$		3	mA
		$f_C = 10 \text{ MHz}$ , $V_{CC} = 2.5 \text{ V}$ , $C = 0.1 V_{CC}/0.9 V_{CC}$ , $Q = \text{open}$		6	
$I_{CC0}$	Supply current (Write)	During $t_W$ , $\overline{S} = V_{CC}$ , $2.5 \text{ V} < V_{CC} < 5.5 \text{ V}$		6	mA
$I_{CC1}$	Supply current (Standby)	$\overline{S} = V_{CC}$ , $V_{CC} = 2.5 \text{ V}$ , $V_{IN} = V_{SS}$ or $V_{CC}$		2	$\mu A$
$V_{IL}$	Input low voltage		-0.45 V	$0.3 V_{CC}$	V
$V_{IH}$	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
$V_{OL}$	Output low voltage	$I_{OL} = 1.5 \text{ mA}$ , $V_{CC} = 2.5 \text{ V}$		0.4	V
$V_{OH}$	Output high voltage	$I_{OH} = -0.4 \text{ mA}$ , $V_{CC} = 2.5 \text{ V}$	$0.8 V_{CC}$		V
$V_{RES}^{(1)}$	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not tested in production.

Table 14. AC characteristics (M95640, device grade 3)

Test conditions specified in <a href="#">Table 8</a> and <a href="#">Table 10</a>							
Symbol	Alt.	Parameter	Min. <sup>(1)</sup>	Max. <sup>(1)</sup>	Min. <sup>(2)</sup>	Max. <sup>(2)</sup>	Unit
$f_C$	$f_{SCK}$	Clock frequency	D.C.	5	D.C.	10	MHz
$t_{SLCH}$	$t_{CSS1}$	$\overline{S}$ active setup time	90		30		ns
$t_{SHCH}$	$t_{CSS2}$	$\overline{S}$ not active setup time	90		30		ns
$t_{SHSL}$	$t_{CS}$	$\overline{S}$ deselect time	100		40		ns
$t_{CHSH}$	$t_{CSH}$	$\overline{S}$ active hold time	90		30		ns
$t_{CHSL}$		$\overline{S}$ not active hold time	90		30		ns
$t_{CH}^{(3)}$	$t_{CLH}$	Clock high time	90		42		ns
$t_{CL}^{(3)}$	$t_{CLL}$	Clock low time	90		40		ns
$t_{CLCH}^{(4)}$	$t_{RC}$	Clock rise time		1		2	$\mu$ s
$t_{CHCL}^{(4)}$	$t_{FC}$	Clock fall time		1		2	$\mu$ s
$t_{DVCH}$	$t_{DSU}$	Data in setup time	20		10		ns
$t_{CHDX}$	$t_{DH}$	Data in hold time	30		10		ns
$t_{HHCH}$		Clock low hold time after $\overline{HOLD}$ not active	70		30		ns
$t_{HLCH}$		Clock low hold time after $\overline{HOLD}$ active	40		30		ns
$t_{CLHL}$		Clock low set-up time before $\overline{HOLD}$ active	0		0		ns
$t_{CLHH}$		Clock low set-up time before $\overline{HOLD}$ not active	0		0		ns
$t_{SHQZ}^{(4)}$	$t_{DIS}$	Output disable time		100		40	ns
$t_{CLQV}^{(5)}$	$t_V$	Clock low to output valid		60		40	ns
$t_{CLQX}$	$t_{HO}$	Output hold time	0		0		ns
$t_{QLQH}^{(4)}$	$t_{RO}$	Output rise time		50		40	ns
$t_{QHQL}^{(4)}$	$t_{FO}$	Output fall time		50		40	ns
$t_{HHQV}$	$t_{LZ}$	$\overline{HOLD}$ high to output valid		50		40	ns
$t_{HLQZ}^{(4)}$	$t_{HZ}$	$\overline{HOLD}$ low to output high-Z		100		40	ns
$t_W$	$t_{WC}$	Write time		5		5	ms

1. These timings are offered with grade 3 devices referenced with “/P” process letters only (see the last digits in [Part numbering](#)).
2. These timings are offered with grade 3 devices referenced with “/PC” process letters only (see the last digits in [Part numbering](#)).
3.  $t_{CH} + t_{CL}$  must never be lower than the shortest possible clock period,  $1/f_C(\text{max})$ .
4. Characterized only, not tested in production.
5.  $t_{CLQV}$  must be compatible with  $t_{CL}$  (clock low time): if the SPI bus master offers a Read setup time  $t_{SU} = 0$  ns,  $t_{CL}$  can be equal to (or greater than)  $t_{CLQV}$ ; in all other cases,  $t_{CL}$  must be equal to (or greater than)  $t_{CLQV} + t_{SU}$ .

Table 15. AC characteristics (M95640-W, device grade 3)

Test conditions specified in <i>Table 9</i> and <i>Table 10</i>							
Symbol	Alt.	Parameter	Min.	Max.	Min.	Max.	Unit
			2.5 V to 5.5 V <sup>(1)</sup>		3.0 V to 5.5 V <sup>(2)</sup>		
f <sub>C</sub>	f <sub>SCK</sub>	Clock frequency	D.C.	5	D.C.	10	MHz
t <sub>SLCH</sub>	t <sub>CSS1</sub>	$\overline{S}$ active setup time	90		30		ns
t <sub>SHCH</sub>	t <sub>CSS2</sub>	$\overline{S}$ not active setup time	90		30		ns
t <sub>SHSL</sub>	t <sub>CS</sub>	$\overline{S}$ deselect time	100		40		ns
t <sub>CHSH</sub>	t <sub>CSH</sub>	$\overline{S}$ active hold time	90		30		ns
t <sub>CHSL</sub>		$\overline{S}$ not active hold time	90		30		ns
t <sub>CH</sub> <sup>(3)</sup>	t <sub>CLH</sub>	Clock high time	90		42		ns
t <sub>CL</sub> <sup>(3)</sup>	t <sub>CLL</sub>	Clock low time	90		40		ns
t <sub>CLCH</sub> <sup>(4)</sup>	t <sub>RC</sub>	Clock rise time		1		2	μs
t <sub>CHCL</sub> <sup>(4)</sup>	t <sub>FC</sub>	Clock fall time		1		2	μs
t <sub>DVCH</sub>	t <sub>DSU</sub>	Data in setup time	20		10		ns
t <sub>CHDX</sub>	t <sub>DH</sub>	Data in hold time	30		10		ns
t <sub>HHCH</sub>		Clock low hold time after $\overline{HOLD}$ not active	70		30		ns
t <sub>HLCH</sub>		Clock low hold time after $\overline{HOLD}$ active	40		30		ns
t <sub>CLHL</sub>		Clock low set-up time before $\overline{HOLD}$ active	0		0		ns
t <sub>CLHH</sub>		Clock low set-up time before $\overline{HOLD}$ not active	0		0		ns
t <sub>SHQZ</sub> <sup>(4)</sup>	t <sub>DIS</sub>	Output disable time		100		40	ns
t <sub>CLQV</sub> <sup>(5)</sup>	t <sub>V</sub>	Clock low to output valid		60		40	ns
t <sub>CLQX</sub>	t <sub>HO</sub>	Output hold time	0		0		ns
t <sub>QLQH</sub> <sup>(4)</sup>	t <sub>RO</sub>	Output rise time		50		40	ns
t <sub>QHQL</sub> <sup>(4)</sup>	t <sub>FO</sub>	Output fall time		50		40	ns
t <sub>HHQV</sub>	t <sub>LZ</sub>	$\overline{HOLD}$ high to output valid		50		40	ns
t <sub>HLQZ</sub> <sup>(4)</sup>	t <sub>HZ</sub>	$\overline{HOLD}$ low to output high-Z		100		40	ns
t <sub>W</sub>	t <sub>WC</sub>	Write time		5		5	ms

1. These timings are offered with grade 3 devices referenced with “/P” process letters only (see the last digits in [Part numbering](#)).
2. These timings are offered with grade 3 devices referenced with “/PC” process letters only (see the last digits in [Part numbering](#)).
3.  $t_{CH} + t_{CL}$  must never be lower than the shortest possible clock period,  $1/f_C(\text{max})$ .
4. Value guaranteed by characterization, not 100% tested in production.
5.  $t_{CLQV}$  must be compatible with  $t_{CL}$  (clock low time): if the SPI bus master offers a Read setup time  $t_{SU} = 0$  ns,  $t_{CL}$  can be equal to (or greater than)  $t_{CLQV}$ ; in all other cases,  $t_{CL}$  must be equal to (or greater than)  $t_{CLQV} + t_{SU}$ .

Figure 15. Serial input timing

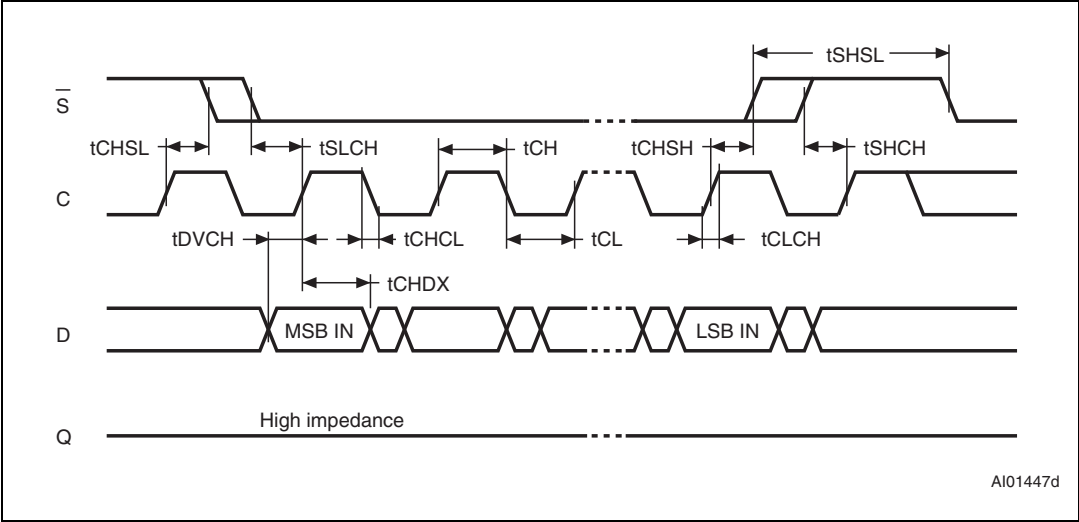


Figure 16. Hold timing

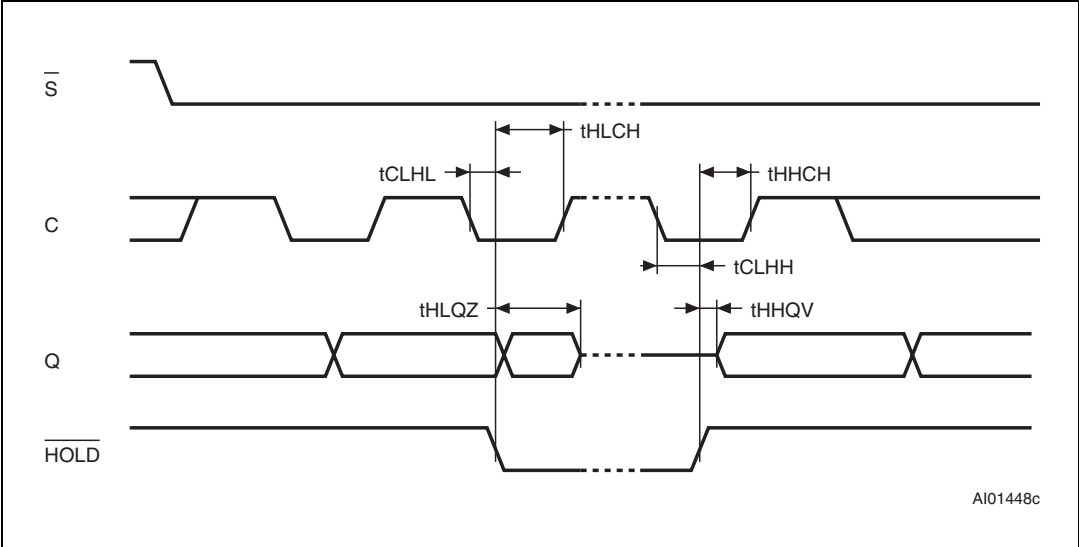
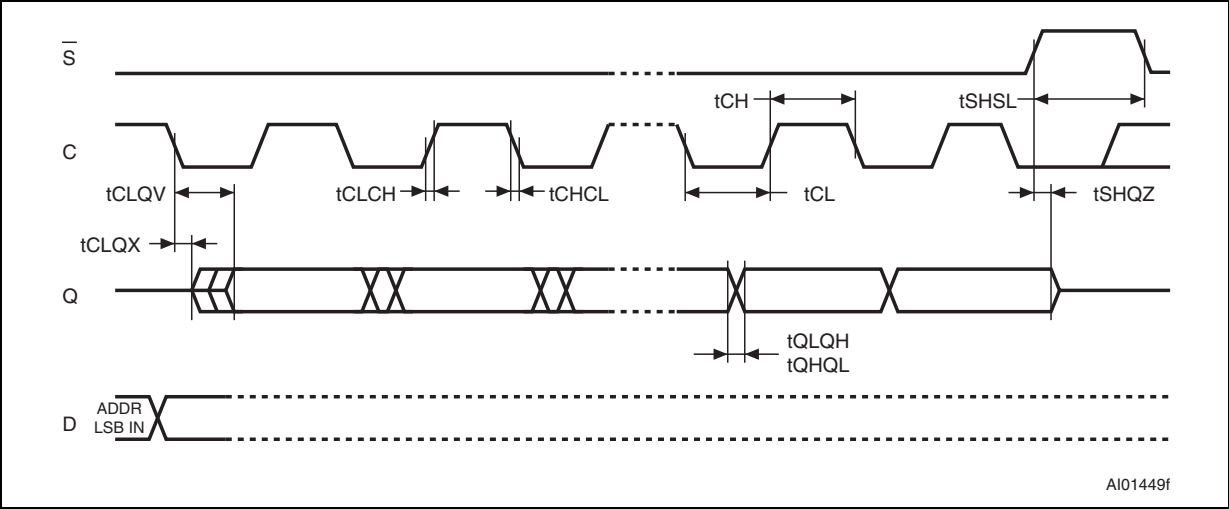


Figure 17. Serial output timing

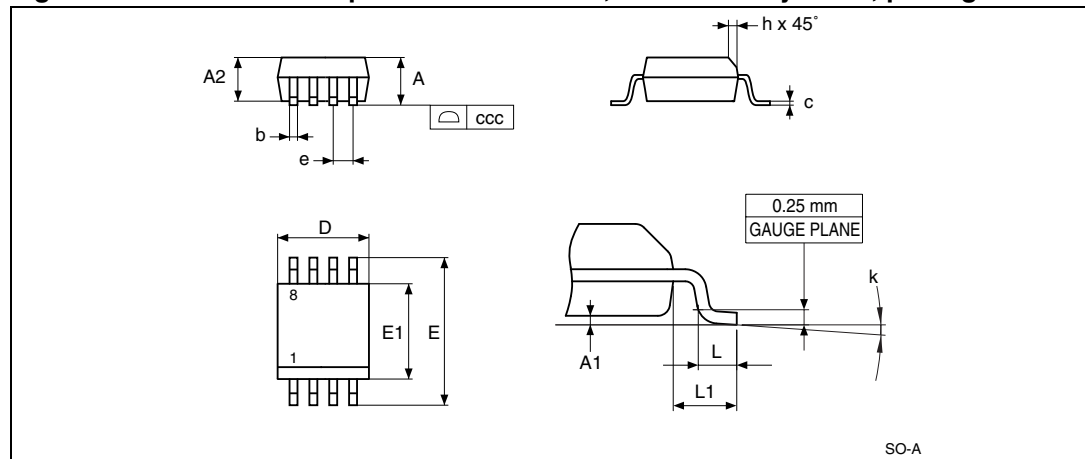




## 10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Figure 18. SO8N – 8-lead plastic small outline, 150 mils body width, package outline**



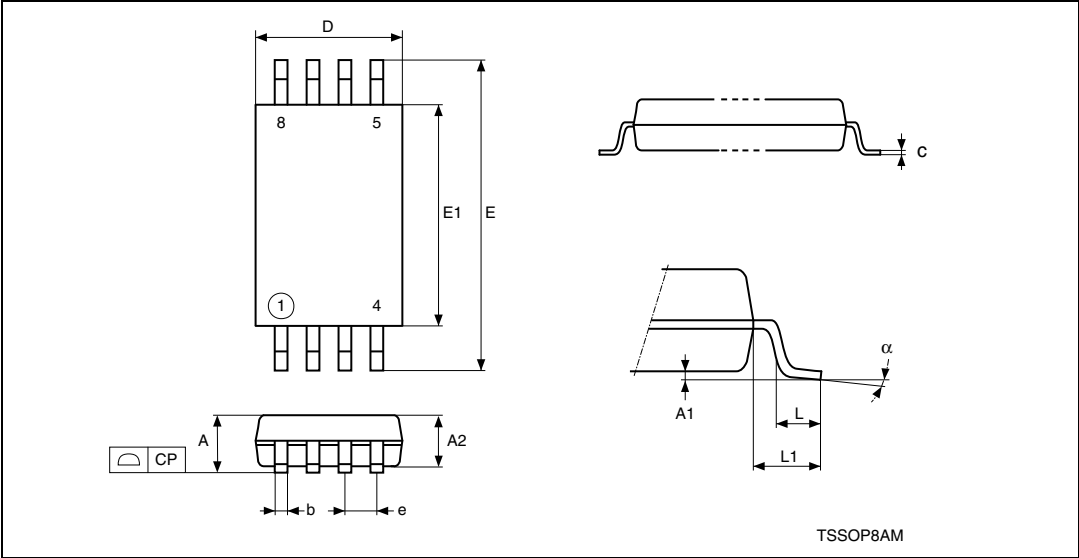
1. Drawing is not to scale.

**Table 16. SO8N – 8-lead plastic small outline, 150 mils body width, mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Typ	Min	Max	Typ	Min	Max
A			1.750			0.0689
A1		0.100	0.250		0.0039	0.0098
A2		1.250			0.0492	
b		0.280	0.480		0.0110	0.0189
c		0.170	0.230		0.0067	0.0091
ccc			0.100			0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270	-	-	0.0500	-	-
h		0.250	0.500		0.0098	0.0197
k		0°	8°		0°	8°
L		0.400	1.270		0.0157	0.0500
L1	1.040			0.0409		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 19. TSSOP8 – 8-lead thin shrink small outline, package outline



1. Drawing is not to scale.

Table 17. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
$\alpha$		0°	8°		0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to four decimal digits.

11 Part numbering

Table 18. Ordering information scheme

Example:	M95640	–	W	MN	3	T	P	/P
<b>Device type</b>								
M95 = SPI serial access EEPROM								
<b>Device function</b>								
640 = 64 Kbit (8192 x 8)								
<b>Operating voltage</b>								
blank = V <sub>CC</sub> = 4.5 to 5.5 V								
W = V <sub>CC</sub> = 2.5 to 5.5 V								
<b>Package</b>								
MN = SO8 (150 mil width)								
DW = TSSOP8 (169 mil width)								
<b>Device grade</b>								
3 = Device tested with high reliability certified flow.								
Automotive temperature range (–40 to 125 °C)								
<b>Option</b>								
blank = Standard packing								
T = Tape and reel packing								
<b>Plating technology</b>								
P = RoHS compliant and halogen-free (ECOPACK®)								
<b>Process</b>								
/P or /PC = Manufacturing technology code								

# 12      Revision history

Table 19.    Document revision history

Date	Revision	Changes
06-Jan-2012	1	Initial release.



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