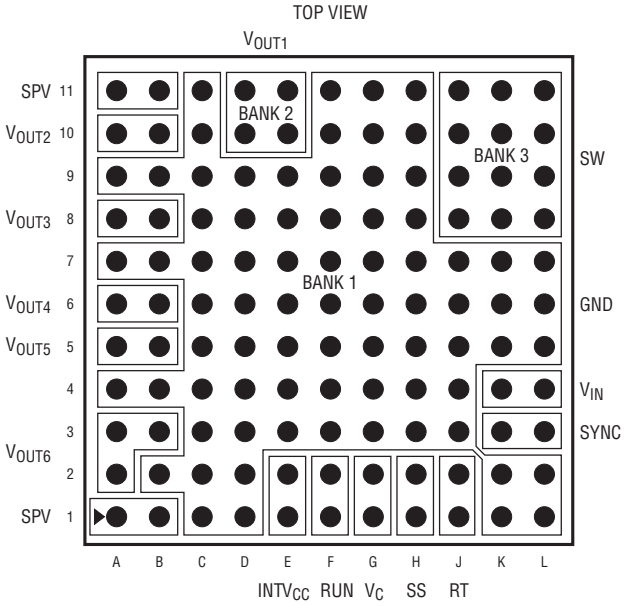
## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$, SW ..... 80V
RUN ..... $INTV_{CC}$
SYNC, SPV, $INTV_{CC}$ ..... 8V
$V_C$, SS ..... 3V
RT ..... 1.5V
$V_{OUT1,2,3,4,5,6}$ Relative to SPV ..... ±20
Operating Internal Temperature
(Note 2) ..... –40°C to 150°C
Storage Temperature Range ..... –55°C to 150°C
Maximum Solder Temperature ..... 245°C

## PIN CONFIGURATION




LGA PACKAGE
121-LEAD (15mm × 15mm × 2.82mm)
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 9.6°C/W, $\theta_{JCtop}$ = 12.2°C/W,
$\theta_{JCbottom}$ = 0.5°C/W, $\theta_{JCboard}$ = 1.6°C/W
VALUES DETERMINED PER JESD51-9, MAX OUTPUT POWER
WEIGHT = 1.4 GRAMS

## ORDER INFORMATION

| LEAD FREE FINISH | TRAY | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTM8008HV#PBF | LTM8008HV#PBF | LTM8008V | 121-Lead (15mm × 15mm × 2.82mm) LGA | –40°C to 150°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications that apply over the full operating temperature range, $V_{IN}$ = 14V, RUN = 14V, otherwise specifications are at $T_A$ = 25°C (Note 2)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Minimum $V_{IN}$ Operating Voltage | | ● | | | 3 | V |
| Minimum $V_{IN}$ Start Voltage | $V_{IN}$ Rising | ● | | | 6 | V |
| $V_{IN}$ Shutdown $I_Q$ | RUN = 0V | | | 70 | | µA |
| $V_{IN}$ Operating $I_Q$ | $V_C$ = 0.3V, $R_T$ = 41.2k | | | 1.6 | 2.2 | mA |
| SPV Regulation Voltage | | | | 5.6 | | V |
| SPV Overvoltage Threshold | | | | 6.1 | | V |
| $V_C$ Source Current | SPV = 0V, $V_C$ = 1.5V | | | –15 | | µA |
| $V_C$ Sink Current | SPV = 6V, $V_C$ = 1.5V | | | 12 | | µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications that apply over the full operating temperature range, $V_{IN}$ = 14V, RUN = 14V, otherwise specifications are at $T_A$ = 25°C (Note 2)**

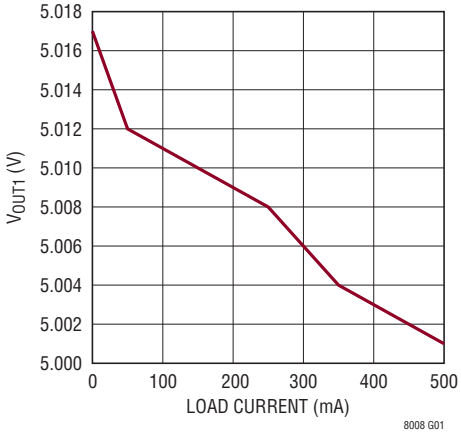
| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Switching Frequency | $R_T$ = 140k to GND<br>$R_T$ = 10.5k to GND | | | 100<br>1 | | kHz<br>MHz |
| Minimum Off Time | | | | 220 | | ns |
| Minimum On Time | | | | 220 | | ns |
| SYNC Input Low | | | | | 0.4 | V |
| SYNC Input High | | | 1.5 | | | V |
| SS Sourcing Current | SS = 0V | | | –10 | | µA |
| SS Sink Current Under Fault | SS = 1V | | | 0.7 | | mA |
| RUN Threshold to Stop Switching | | ● | 1.15 | 1.21 | 1.26 | V |
| RUN Bias Current Low | | | | 2 | | µA |
| RUN Bias Current High | RUN = 1.3V | | | | 0.1 | µA |
| SW Current Limit | | ● | 7.4 | 8.2 | 9.0 | A |
| SW $R_{DS(ON)}$ | | | | 35 | | mΩ |
| $V_{OUT1}$ Output Voltage | 1mA < $I_{LOAD}$ < 500mA | <br>● | 4.95<br>4.9 | 5 | 5.05<br>5.1 | V<br>V |
| $V_{OUT1}$ Load Regulation | $\Delta I_{LOAD}$ = 1mA to 500mA | <br>● | | 12 | 25<br>50 | mV<br>mV |
| $V_{OUT1}$ RMS Output Noise | $R_T$ = 41.2k, $I_{LOAD}$ = 500mA, BW = 100Hz to 100kHz | | | 20 | | $\mu V_{RMS}$ |
| $V_{OUT1}$ Current Limit | | ● | 520 | | | mA |
| $V_{OUT1}$ Reverse Output Current | SPV = 0, $V_{OUT1}$ = 5V | | | 10 | | µA |
| $V_{OUT2,3,4,5}$ Output Voltage | 1mA < $I_{LOAD}$ < 150mA | <br>● | 4.95<br>4.9 | 5 | 5.05<br>5.1 | V<br>V |
| $V_{OUT2,3,4,5}$ Load Regulation | $\Delta I_{LOAD}$ = 1mA to 150mA | <br>● | | 9 | 25<br>50 | mV<br>mV |
| $V_{OUT2,3,4,5}$ RMS Output Noise | $R_T$ = 41.2k, $I_{LOAD}$ = 150mA, BW = 100Hz to 100kHz | | | 20 | | $\mu V_{RMS}$ |
| $V_{OUT2,3,4,5}$ Current Limit | | ● | 160 | | | mA |
| $V_{OUT2,3,4,5}$ Reverse Output Current | SPV = 0, $V_{OUT2,3,4,5}$ = 5V | | | 10 | 20 | µA |
| $V_{OUT6}$ Output Voltage | 1mA < $I_{LOAD}$ < 300mA | <br>● | 3.267<br>3.234 | 3.3 | 3.333<br>3.366 | V<br>V |
| $V_{OUT6}$ Load Regulation | $\Delta I_{LOAD}$ = 1mA to 300mA | ● | | 7 | 15<br>33 | mV<br>mV |
| $V_{OUT6}$ RMS Output Noise | $R_T$ = 41.2k, $I_{LOAD}$ = 300mA, BW = 100Hz to 100kHz | | | 20 | | $\mu V_{RMS}$ |
| $V_{OUT6}$ Current Limit | | ● | 320 | | | mA |
| $V_{OUT6}$ Reverse Output Current | SPV = 0, $V_{OUT1}$ = 5V | | | 10 | 20 | µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

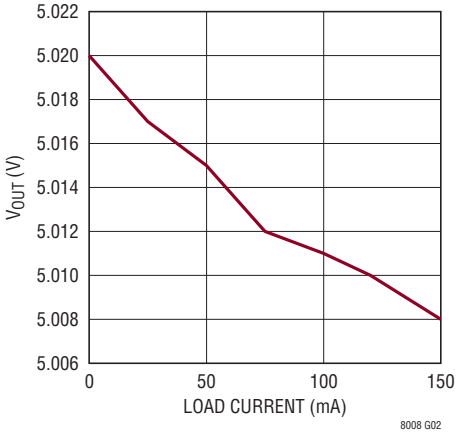
**Note 2:** The LTM8008HV is guaranteed to meet performance specifications from –40°C to 150°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

## TYPICAL PERFORMANCE CHARACTERISTICS

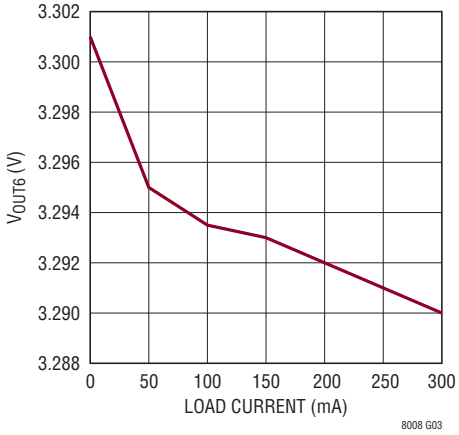
**$V_{OUT1}$ vs Load**



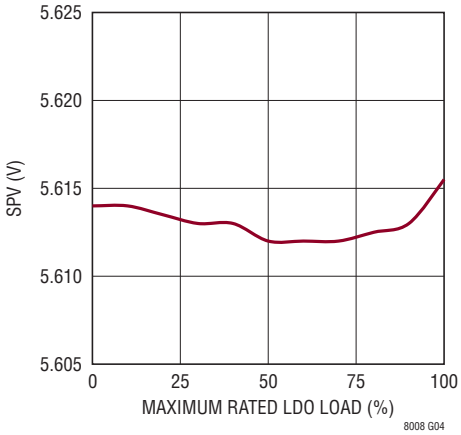

**$V_{OUT2,3,4,5}$ vs Load**



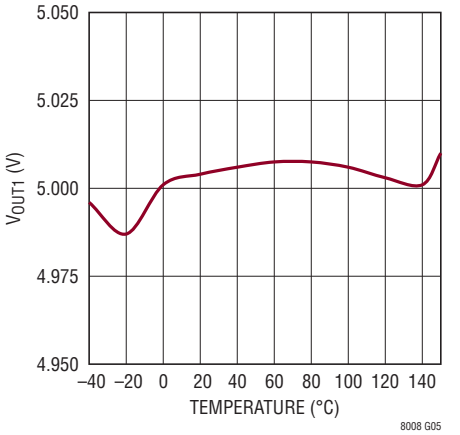

**$V_{OUT6}$ vs Load**



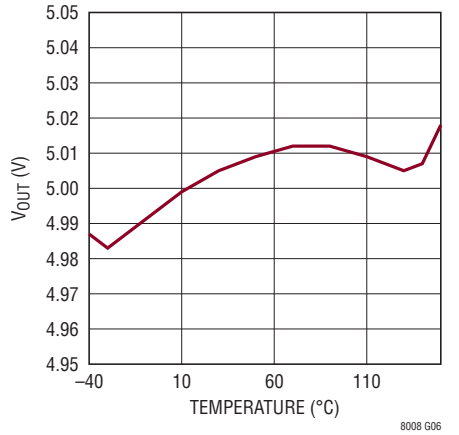

**SPV vs Percentage of LDO Load**



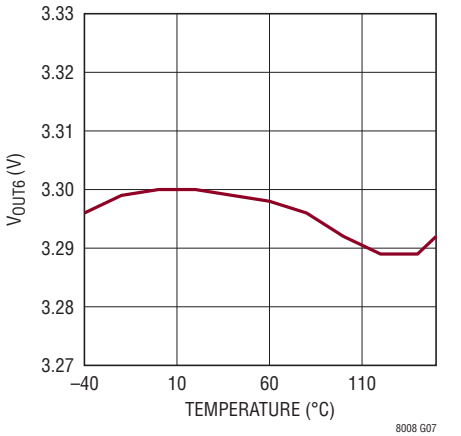

**$V_{OUT1}$ vs Temperature Full Load**



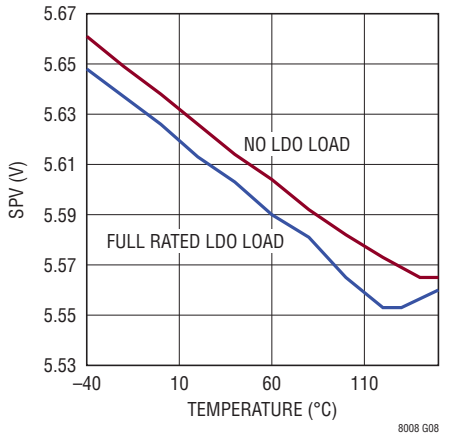

**$V_{OUT2,3,4,5}$ vs Temperature Full Load**



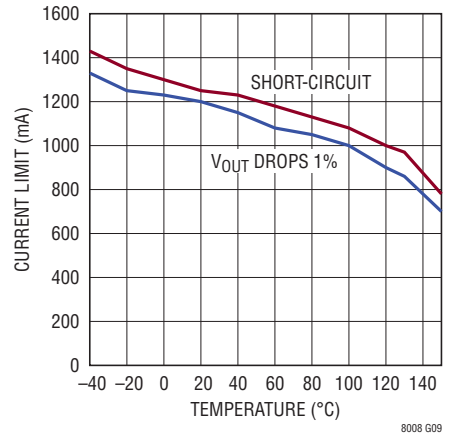

**$V_{OUT6}$ vs Temperature Full Load**




**SPV vs Temperature (Front Page Schematic)**

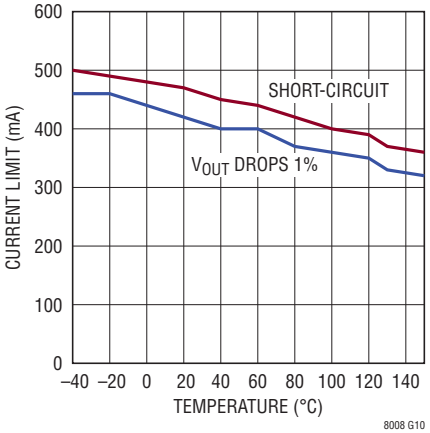



**$V_{OUT1}$ Current Limit vs Temperature**

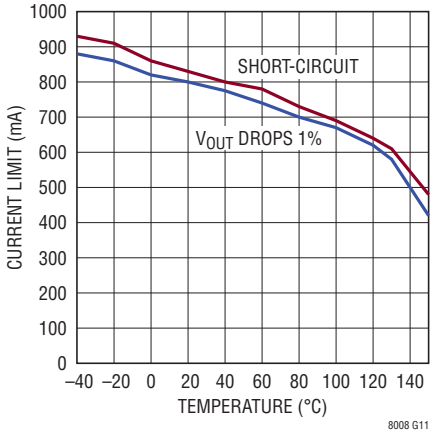


# TYPICAL PERFORMANCE CHARACTERISTICS

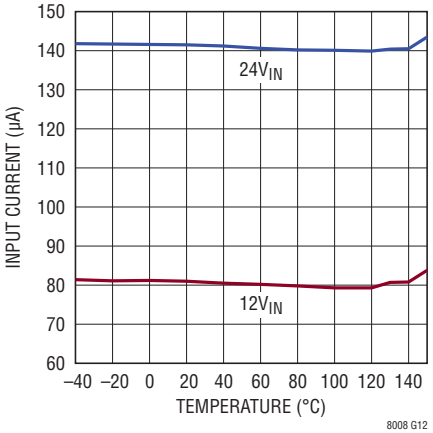
**$V_{OUT2,3,4,5}$ Current Limit vs Temperature**



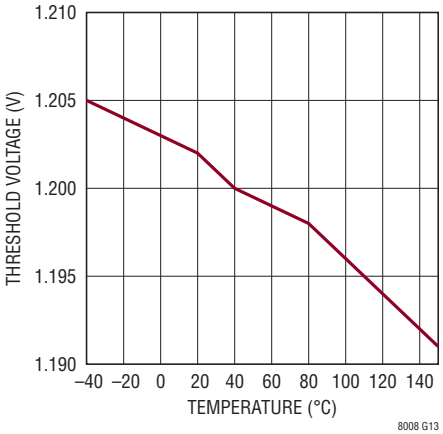

**$V_{OUT6}$ Current Limit vs Temperature**



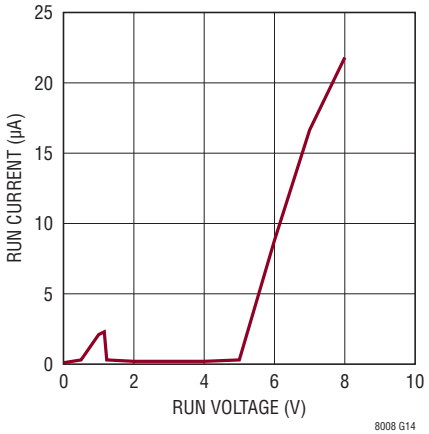

**$V_{IN}$ Pin Current vs Temperature (No Load)**



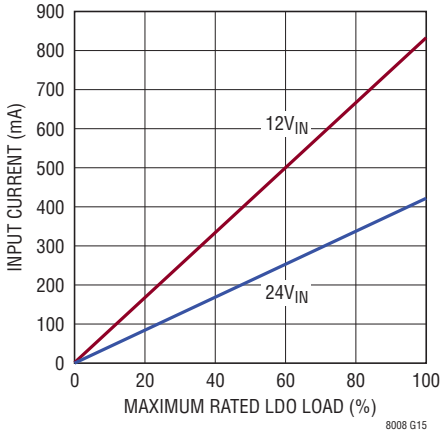

**RUN Threshold vs Temperature**



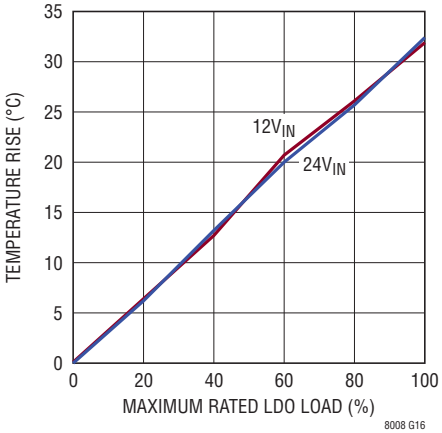

**Run Current vs Run Voltage**




**Input Current vs Percentage of LDO Load (Front Page Schematic)**




**Temperature Rise vs Percentage of LDO Load (Front Page Schematic, Measured on DC1630A Demo Board)**



## PIN FUNCTIONS

**$V_{IN}$ (K4, L4):** Input Supply Pin. Must be locally bypassed with a 0.22µF or larger capacitor placed close to the pin.

**RUN (F1, F2):** Shutdown and Undervoltage Detect Pin. An accurate 1.21V (nominal) falling threshold with externally programmable hysteresis detects when power is okay to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 2µA pull-down current. An undervoltage condition resets soft-start. Tie to 0.4V or less to disable the device and reduce $V_{IN}$ quiescent current below 70µA. Tie to $INTV_{CC}$ if this function is not used.

**GND (Bank 1):** Ground. Tie these GND pins to a local ground plane under the LTM8008 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8008 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details.

**SYNC (K3, L3):** Frequency Synchronization Pin. It is used to synchronize the switching frequency to an external clock. If this feature is used, an $R_T$ resistor should be chosen to program a switching frequency 20% lower than the SYNC pulse frequency. Tie the SYNC pin to GND if this feature is not used. See the Synchronization section in Applications Information.

**RT (J1, J2):** The RT pin is used to program the switching frequency of the LTM8008 by connecting a resistor from this pin to ground. Table 1 gives the resistor values that correspond to the resultant switching frequency. Minimize the capacitance at this pin.

**SS (H1, H2):** Soft-Start Pin. This pin modulates the compensation pin voltage ($V_C$) clamp. The soft-start interval is set with an external capacitor. The pin has a 10µA (typical) pull-up current source to an internal 2.5V rail. The soft-start pin is reset to GND by an undervoltage condition at RUN, an $INTV_{CC}$ undervoltage or overvoltage condition or an internal thermal lockout.

**$V_C$ (G1, G2):** Error Amplifier Compensation Pin. This is used to stabilize the voltage loop with an external RC network.

**$INTV_{CC}$ (E1, E2):** Regulated Supply for Internal Loads. This is derived from $V_{IN}$ and SPV; it must be bypassed with at least a 4.7µF capacitor placed close to the pin.

**SPV (A1, B1, A11, B11):** SEPIC Output Voltage. This is connected to the internal SEPIC feedback network and is used to power the six post regulators. It must be locally bypassed by at least 22µF. Apply a bypass capacitor at each set of pins.

**$V_{OUT1}$ (Bank 2):** Output of the 5V, 500mA Linear Post Regulator. It must be locally bypassed with at least 22µF.

**$V_{OUT2}$ (A10, B10):** Output of One of the Four 5V, 150mA Linear Post Regulators. It must be bypassed with at least 10µF.

**$V_{OUT3}$ (A8, B8):** Output of One of the Four 5V, 150mA Linear Post Regulators. It must be bypassed with at least 10µF.

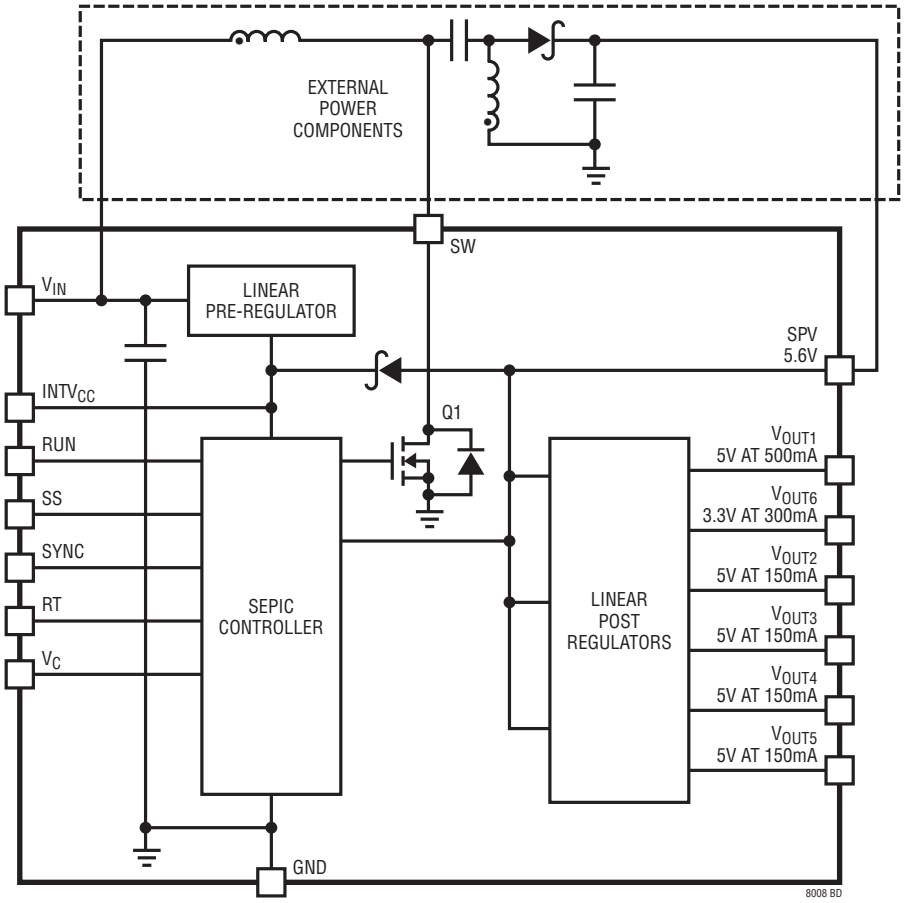
**$V_{OUT4}$ (A6, B6):** Output of One of the Four 5V, 150mA Linear Post Regulators. It must be bypassed with at least 10µF.

**$V_{OUT5}$ (A5, B5):** Output of One of the Four 5V, 150mA Linear Post Regulators. It must be bypassed with at least 10µF.

**$V_{OUT6}$ (A2, A3, B2):** Output of the 3.3V, 300mA Linear Post Regulator. It must be bypassed by at least 10µF.

**SW (Bank 3):** SEPIC Converter Switch. This is the drain of the internal power switching MOSFET.

## SIMPLIFIED BLOCK DIAGRAM




## OPERATION

The LTM8008 is a SEPIC equipped with six high performance linear post regulators. The device contains the SEPIC power MOSFET, controller, linear regulators and optimized support circuitry. The current limit for the SEPIC converter is internally set to 8.2A. The output of the SEPIC converter is internally set to 5.6V, which is the optimal voltage for running the six post regulators at the best combination of efficiency, ripple rejection and thermal performance.

The SEPIC converter is equipped with several control pins. These include RUN for enabling and sequencing, SS for soft-start control, SYNC for frequency synchronization, RT for setting the operating frequency and $V_C$ for frequency compensation. There are also power ports, $V_{IN}$, $INTV_{CC}$, SPV and the six post regulator outputs, $V_{OUT1,2,3,4,5,6}$, as well as the SEPIC converter switch node, SW.

Of the six linear post regulators, one produces 5V at 500mA, a second produces 3.3V at 300mA and the remaining four provide 5V at 150mA each. Each one is individually equipped with overcurrent, reverse voltage and thermal protection.

## APPLICATIONS INFORMATION

### Running Input Voltage Versus Start Voltage

In normal operation the LTM8008 SEPIC Converter output SPV is used to run the $INTV_{CC}$ internal biasing through a rectifying diode (see the Block Diagram). This allows the internal MOSFET driver Q1 and other circuitry to be properly biased even when the input voltage falls as low as 3V. At start-up, however, the SPV voltage is low and $INTV_{CC}$ is derived from $V_{IN}$ through a linear regulator. In order to properly bias the LTM8008 internal circuitry at start-up, $V_{IN}$ must rise to at least 6V.

### Main Control Loop

The LTM8008 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. At the start of each oscillator cycle, a latch turns on the internal power MOSFET switch. The switch current flows through an internal current sensing resistor and generates a voltage proportional to the switch current. This current sense voltage is added to a stabilizing slope compensation ramp and the resulting sum is compared with the voltage on the $V_C$ pin. When the stabilized current sense voltage exceeds the level of the $V_C$ pin, the internal latch is reset, turning off the power switch. The level at the $V_C$ pin is an amplified version of the difference between the feedback voltage and the reference voltage. In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation. The LTM8008 is also equipped with a switch current limit function. If the detected current is higher than 8.2A, typical, the internal circuitry will turn off Q1 for the rest of the switching cycle.

The LTM8008 has overvoltage protection functions to protect the converter from excessive output voltage overshoot during start-up or recovery from a short-circuit condition. If the output voltage exceeds the targeted set point by 8%, internal circuitry will actively inhibit switching for the duration of an output overvoltage condition.

### Programming Turn-On and Turn-Off Thresholds with the RUN Pin

The RUN pin controls whether the LTM8008 is enabled or shut down. Low power circuitry allows the user to accurately program the supply voltage at which the SEPIC converter turns on and off. The falling value can be accurately set by the resistor divider network composed of R3 and R4 shown in Figure 1.

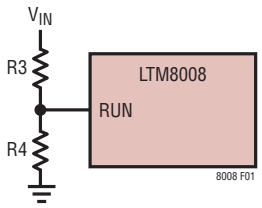



**Figure 1. The LTM8008 Turn-On and Turn-Off Thresholds Are Set by a Simple Resistor Network**

If RUN is above 1.21V, the LTM8008 is running. Below 1.21V and above 0.7V, the LTM8008 is off and the RUN pin sinks a hysteresis current (typically 2µA). Below 0.7V, the LTM8008 is not switching and is in a low power state, drawing less than 70µA at $V_{IN}$. The typical falling threshold voltage and rising threshold voltage can be calculated by the following equations:

$$V_{VIN,FALLING} = 1.21 \bullet \frac{(R3 + R4)}{R4}$$

$$V_{VIN,RISING} = 2\mu A \bullet R3 + V_{IN,FALLING}$$

For applications where the RUN pin is not used, the RUN pin can be connected directly to the input voltage $INTV_{CC}$ for always-on operation.

### $INTV_{CC}$ Regulator Bypassing and Operation

An internal, low dropout (LDO) voltage regulator produces the $INTV_{CC}$ supply which powers the internal circuitry during start-up or whenever SPV is low. The LTM8008 contains an undervoltage lockout comparator and an overvoltage lockout comparator for the $INTV_{CC}$ supply. The $INTV_{CC}$ undervoltage (UV) function protects the internal circuitry from attempting to operate in a brown-out condition, while the overvoltage (OV) function protects the gate of the power MOSFET and excessive power dissipation within the LTM8008 in the case of a fault. When $INTV_{CC}$ is below the UV threshold, or above the OV threshold, switching stops and the soft-start operation will be triggered.

The $INTV_{CC}$ regulator must be bypassed to ground immediately adjacent to the LTM8008 pins with a minimum of a 4.7µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

## APPLICATIONS INFORMATION

In an actual application, most of the $INTV_{CC}$ supply current is used to drive the gate capacitance of the power MOSFET. The power dissipation can be a significant concern when the internal MOSFET is being driven at a high frequency and the $V_{IN}$ voltage is high. It is important to limit the power dissipation of the MOSFET and/or adjust the operating frequency so the LTM8008 does not exceed its maximum junction temperature rating.

### Operating Frequency and Synchronization

The choice of operating frequency may be determined by on-chip power dissipation, otherwise it is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing gate drive current and MOSFET and diode switching losses. However, lower frequency operation requires a physically larger inductor. Switching frequency also has implications for loop compensation. The LTM8008 uses a constant-frequency architecture that can be programmed over a 100kHz to 1MHz range with a single external resistor from the RT pin to GND. The RT pin must have an external resistor to GND for proper operation of the LTM8008. A table for selecting the value of $R_T$ for a given operating frequency is shown in Table 1.

**Table 1. Timing Resistor ($R_T$) Value**

| OSCILLATOR FREQUENCY (kHz) | $R_T$ (kΩ) |
|---|---|
| 100 | 140 |
| 200 | 63.4 |
| 300 | 41.2 |
| 400 | 30.9 |
| 500 | 24.3 |
| 600 | 19.6 |
| 700 | 16.5 |
| 800 | 14 |
| 900 | 12.1 |
| 1000 | 10.5 |

The operating frequency of the LTM8008 can be synchronized to an external clock source. By providing a digital clock signal into the SYNC pin, the LTM8008 will operate at the SYNC clock frequency. If this feature is used, an $R_T$ resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. The SYNC pulse should have a minimum pulse width of 200ns. Tie the SYNC pin to GND if this feature is not used.

### Duty Cycle Considerations

Switching duty cycle is a key variable defining converter operation. As such, its limits must be considered. Minimum on-time is the smallest time duration that the LTM8008 is capable of turning on the power MOSFET. This time is generally about 220ns (typical) (see Minimum On-Time in the Electrical Characteristics table). In each switching cycle, the LTM8008 keeps the power switch off for at least 220ns (typical) (see Minimum Off-Time in the Electrical Characteristics table).

### Soft-Start

The LTM8008 contains several features to limit peak switch currents and output voltage ($V_{OUT}$) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load. High peak switch currents during start-up may occur in switching regulators. Since $V_{OUT}$ is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

The LTM8008 addresses this mechanism with the SS pin. The SS circuit reduces the power MOSFET current by pulling down the $V_C$ pin. In this way the SS allows the output capacitor to charge gradually toward its final value while limiting the start-up peak currents. The inductor current slew rate is limited by the soft-start function.

Besides start-up, soft-start can also be invoked by the following faults:

1. $INTV_{CC}$ overvoltage
2. $INTV_{CC}$ undervoltage
3. Thermal lockout

Any of these three faults will cause the LTM8008 to stop switching immediately and discharge the SS pin. When all faults are cleared and the SS pin has been discharged below 0.2V, a 10µA current source will start charging the

## APPLICATIONS INFORMATION

SS pin, initiating a soft-start operation. The soft-start interval is set by the soft-start capacitor selection according to the equation:

$$T_{SS} = C_{SS} \bullet \frac{1.25V}{10\mu A}$$

### Thermal Lockout

If LTM8008 internal temperature reaches 165°C (typical), the part will go into thermal lockout. The power switch will be turned off. A soft-start operation will be triggered. The part will be enabled again when the die temperature has dropped by 5°C (nominal).

### Loop Compensation

Loop compensation determines the stability and transient performance. The LTM8008 uses current mode control to regulate the output which simplifies loop compensation. The optimum values depend on the converter topology, the component values and the operating conditions (including the input voltage, load current, etc.). To compensate the feedback loop of the LTM8008, a series resistor-capacitor network is usually connected from the $V_C$ pin to GND.

Figure 2 shows the typical $V_C$ compensation network. For most applications, the capacitor $C_{C1}$ should be in the range of 1nF to 47nF, and the resistor $R_C$ should be in the range of 2.5k to 50k. A small capacitor $C_{C2}$ is often connected in parallel with the $R_C$ compensation network to attenuate the $V_C$ voltage ripple induced from the output voltage ripple through the internal error amplifier. The parallel capacitor usually ranges in value from 10pF to 100pF. A practical approach to design the compensation network is to start with one of the circuits in this data sheet that is similar to your application, and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature.

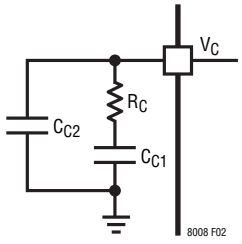



**Figure 2. A Typical Compensation Network**

### Board Layout

The high speed operation of the LTM8008 demands careful attention to board layout and component placement. The GND pads of the package are the primary heat path of the device, and are important for thermal management. Therefore, it is crucial to achieve a good electrical and thermal contact between the GND pads and the ground plane of the board. For the LTM8008 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package.

It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the LTM8008 and into a copper plane with as much area as possible. To prevent radiation and high frequency resonance problems, proper layout of the components connected to the LTM8008 is essential, especially the power paths with higher di/dt. The high di/dt loop should be kept as tight as possible to reduce inductive ringing. In the SEPIC configuration, the high di/dt loop contains the power MOSFET, sense resistor, output capacitor, Schottky diode and the coupling capacitor. Keep the circuit path among these components as short as possible.

The LTM8008 is a switching power supply, so care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heat-sinking are acceptable. Here are additional tips to follow:

1. Place the L1, $R_T$ and $V_C$ components as close as possible to their respective pins.
2. Place the $C_{IN}$, $C_{INTVCC}$, SPV and $C_{OUT}$ capacitors as close as possible to their respective pins. If more than one capacitor is required in parallel, place as many of the electrically paralleled capacitors as close as possible to their respective pin.
3. Place the $C_{IN}$ and $C_{OUT}$ capacitors such that their ground currents follow a path as short as possible.

## APPLICATIONS INFORMATION

4. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8008.

5. For good heatsinking, use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 3. The LTM8008 can benefit from the heat-sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

### Post Regulator Output Capacitance and Transient Response

The LTM8008 linear post regulators are designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. The output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the post regulators, will increase the effective output capacitor value. Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and

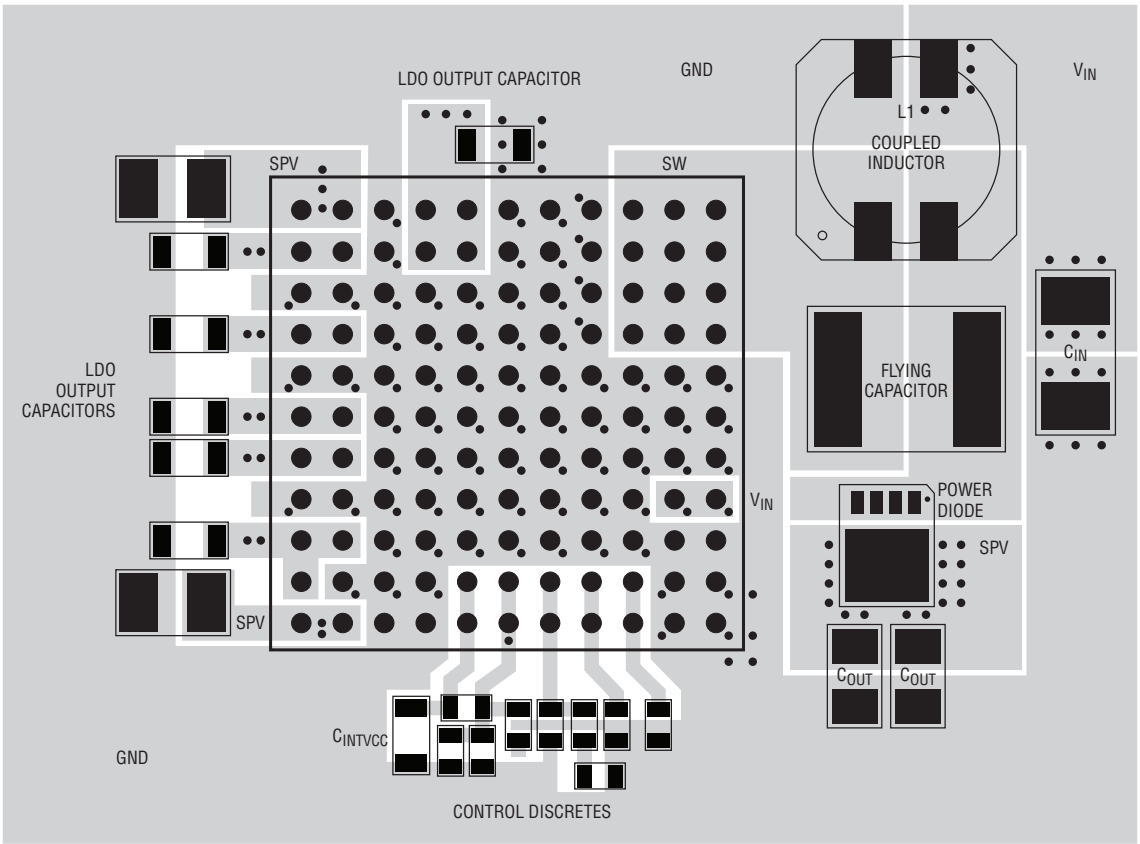



**Figure 3. Layout Showing Suggested External Components, GND Plane and Interconnect/Thermal Vias**

## APPLICATIONS INFORMATION

X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing.

### Post Regulator Thermal Considerations

The power handling capability of the post regulators will be limited by the maximum rated junction temperature (150°C). The power dissipated by each post regulator is approximately the output current multiplied by the input/output voltage differential: $(I_{OUT}) \bullet (SPV - V_{OUT})$.

The post regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 150°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction-to-ambient. Additional heat sources mounted nearby must also be considered. For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

### Protection Features

The linear post regulators incorporate several protection features. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages and reverse voltages from output to input. Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 150°C.

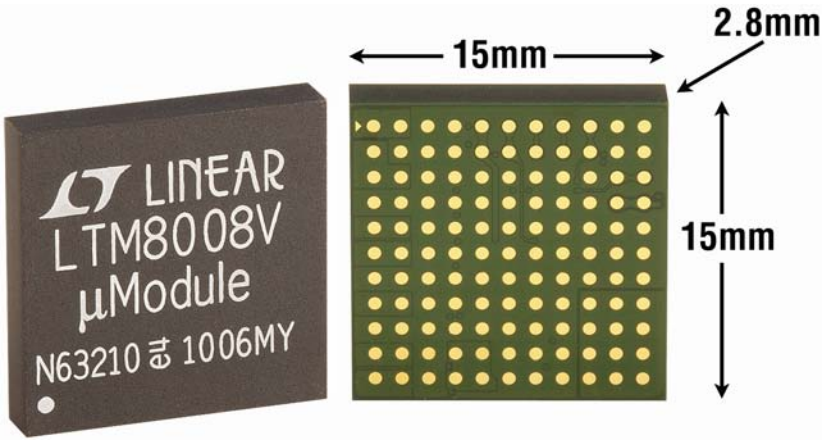
When any of the $V_{OUT}$ pins are forced above the SPV pin of the LTM8008, input current to the corresponding post regulator will typically drop to less than 2µA. The output of the linear post regulators can be pulled below ground without damaging the device. If the input is left open-circuit or grounded, the output can be pulled below ground by 20V. The outputs will act like a large resistor, typically 500k or higher, limiting current flow to less than 100µA. In the case of a short circuit, the output will source the short-circuit current of the device and will protect itself by thermal limiting.

# PACKAGE DESCRIPTION

**Pin Assignment Table**
**(Arranged by Pin Number)**

| PIN NAME | | PIN NAME | | PIN NAME | | PIN NAME | | PIN NAME | | PIN NAME | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | SPV | C1 | GND | E1 | $INTV_{CC}$ | G1 | $V_C$ | J1 | RT | L1 | GND |
| A2 | $V_{OUT6}$ | C2 | GND | E2 | $INTV_{CC}$ | G2 | $V_C$ | J2 | RT | L2 | GND |
| A3 | $V_{OUT6}$ | C3 | GND | E3 | GND | G3 | GND | J3 | GND | L3 | SYNC |
| A4 | GND | C4 | GND | E4 | GND | G4 | GND | J4 | GND | L4 | $V_{IN}$ |
| A5 | $V_{OUT5}$ | C5 | GND | E5 | GND | G5 | GND | J5 | GND | L5 | GND |
| A6 | $V_{OUT4}$ | C6 | GND | E6 | GND | G6 | GND | J6 | GND | L6 | GND |
| A7 | GND | C7 | GND | E7 | GND | G7 | GND | J7 | GND | L7 | GND |
| A8 | $V_{OUT3}$ | C8 | GND | E8 | GND | G8 | GND | J8 | SW | L8 | SW |
| A9 | GND | C9 | GND | E9 | GND | G9 | GND | J9 | SW | L9 | SW |
| A10 | $V_{OUT2}$ | C10 | GND | E10 | $V_{OUT1}$ | G10 | GND | J10 | SW | L10 | SW |
| A11 | SPV | C11 | GND | E11 | $V_{OUT1}$ | G11 | GND | J11 | SW | L11 | SW |
| B1 | SPV | D1 | GND | F1 | RUN | H1 | SS | K1 | GND | | |
| B2 | GND | D2 | GND | F2 | RUN | H2 | SS | K2 | GND | | |
| B3 | $V_{OUT6}$ | D3 | GND | F3 | GND | H3 | GND | K3 | SYNC | | |
| B4 | GND | D4 | GND | F4 | GND | H4 | GND | K4 | $V_{IN}$ | | |
| B5 | $V_{OUT5}$ | D5 | GND | F5 | GND | H5 | GND | K5 | GND | | |
| B6 | $V_{OUT4}$ | D6 | GND | F6 | GND | H6 | GND | K6 | GND | | |
| B7 | GND | D7 | GND | F7 | GND | H7 | GND | K7 | GND | | |
| B8 | $V_{OUT3}$ | D8 | GND | F8 | GND | H8 | GND | K8 | SW | | |
| B9 | GND | D9 | GND | F9 | GND | H9 | GND | K9 | SW | | |
| B10 | $V_{OUT2}$ | D10 | $V_{OUT1}$ | F10 | GND | H10 | GND | K10 | SW | | |
| B11 | SPV | D11 | $V_{OUT1}$ | F11 | GND | H11 | GND | K11 | SW | | |

# PACKAGE PHOTO



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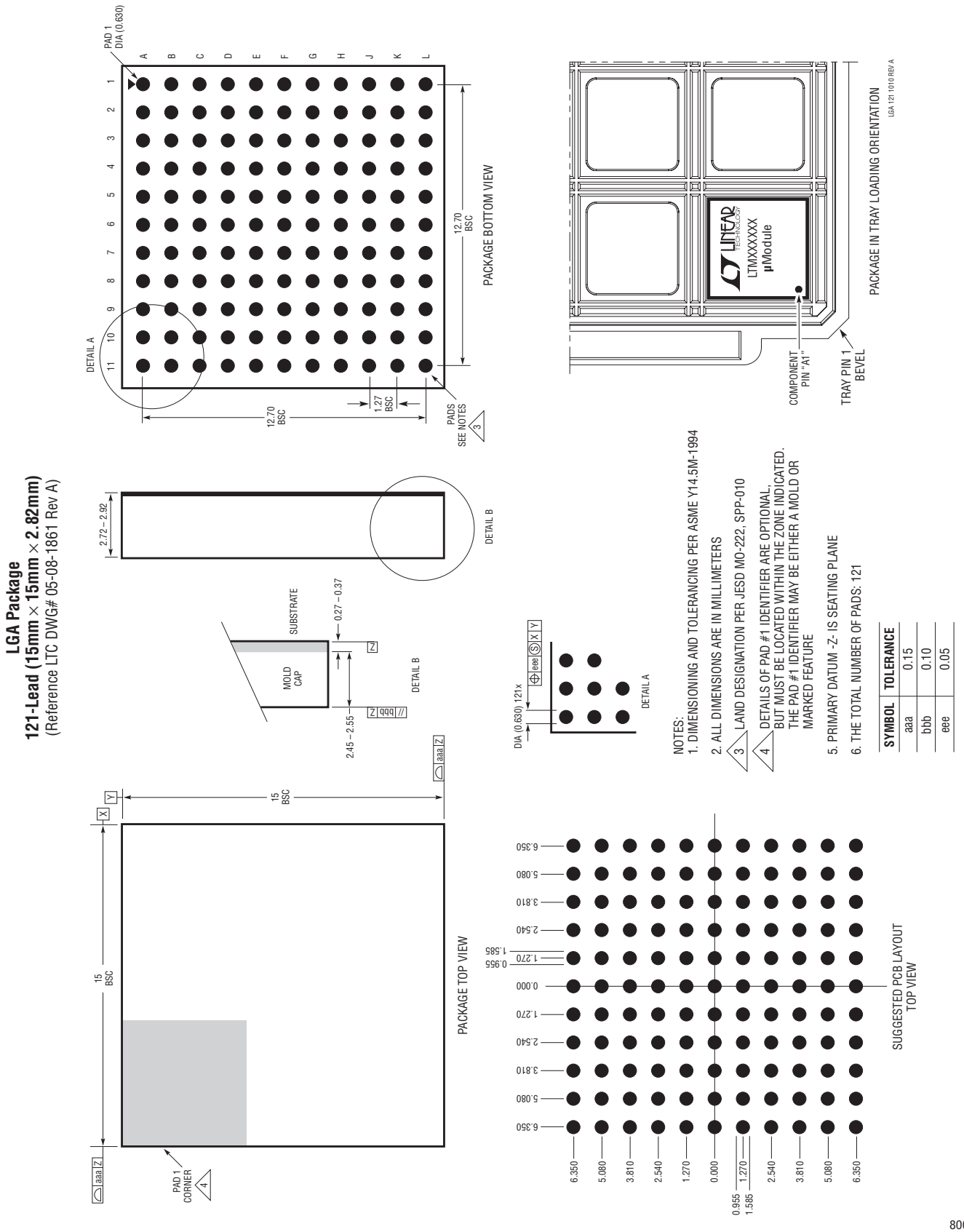
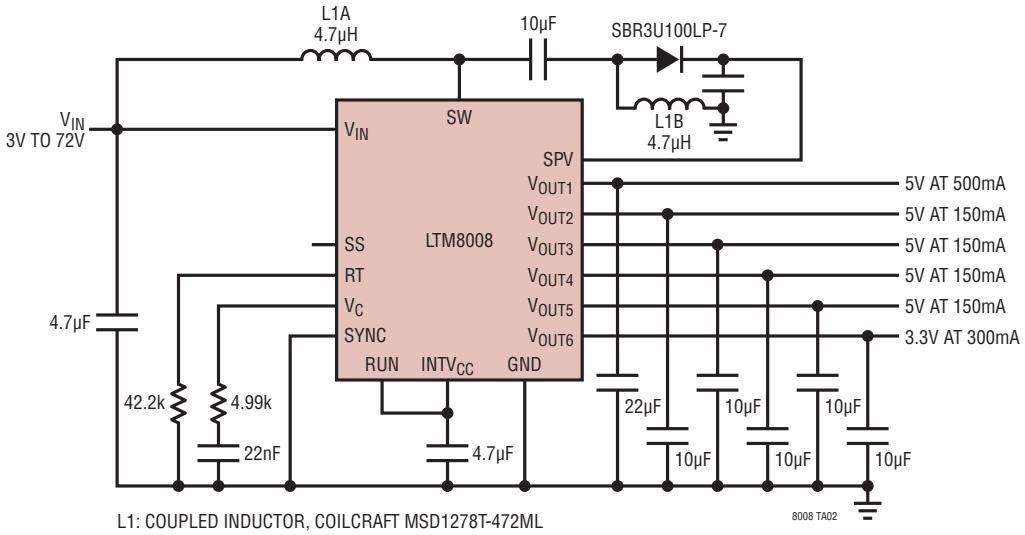


## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 2/11 | Removed “RUN Threshold to $I_Q$ to Fall Below 1µA” spec | 3 |

## TYPICAL APPLICATION

**Six Output DC/DC µModule Regulator**




L1: COUPLED INDUCTOR, COILCRAFT MSD1278T-472ML

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTM8027 | 60V, 4A DC/DC µModule Regulator | $4.5V \le V_{IN} \le 60V$, $2.5V \le V_{OUT} \le 24V$, 15mm × 15mm × 4.32mm |
| LTC3824 | 60V, 40µA $I_Q$ DC/DC Regulator | $4V \le V_{IN} \le 60V$, 100% Duty Cycle, 200kHz to 600kHz |

For an H-Grade Product Portfolio go to: http://cds.linear.com/docs/Information%20Card/LTC_H_Grade_Products_Web.pdf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