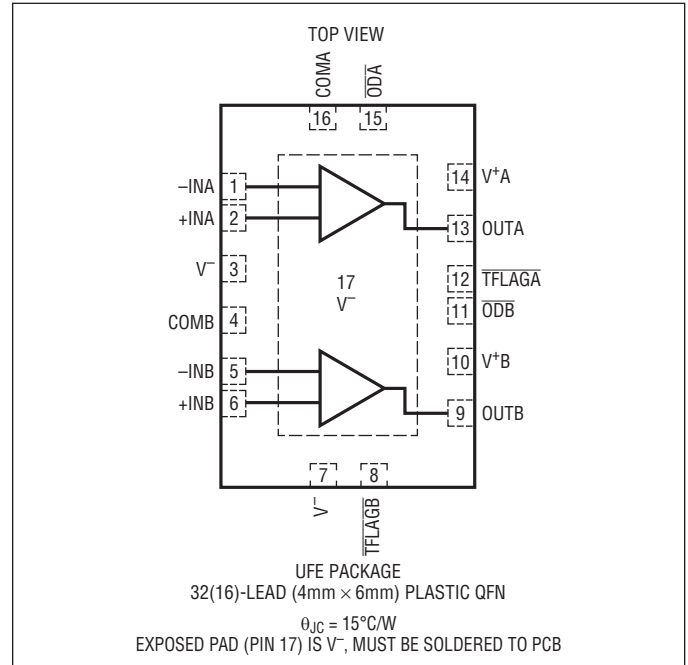


## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage ( $V^+A$ to $V^-$ , or $V^+B$ to $V^-$ )	150V
COMA	$V^-$ to $V^+A$
COMB	$V^-$ to $V^+B$
Input Voltage	
$\overline{ODA}$	$V^-$ to $V^+A + 0.3V$
$\overline{ODB}$	$V^-$ to $V^+B + 0.3V$
+INA, -INA	$V^- - 0.3V$ to $V^+A + 0.3V$
+INB, -INB	$V^- - 0.3V$ to $V^+B + 0.3V$
$\overline{ODA}$ to COMA, $\overline{ODB}$ to COMB	-3V to 7V
Input Current	
+INA, -INA, +INB, -INB	$\pm 10mA$
TFLAGA, TFLAGB Output	
TFLAGA	$V^- - 0.3V$ to $V^+A + 0.3V$
TFLAGB	$V^- - 0.3V$ to $V^+B + 0.3V$
TFLAGA to COMA	-3V to 7V
TFLAGB to COMB	-3V to 7V
Continuous Output Current	
OUTA, OUTB (Note 2)	50mA <sub>RMS</sub>
Operating Junction Temperature Range	
(Note 3)	-40°C to 125°C
Specified Junction Temperature Range (Note 4)	
LTC6091I	-40°C to 85°C
LTC6091H	-40°C to 125°C
Junction Temperature (Note 5)	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering 10sec)	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6091IUFEPBF	LTC6091IUFETRPF	6091	16-Lead Plastic QFN	-40°C to 85°C
LTC6091HUFEPBF	LTC6091HUFETRPF	6091	16-Lead Plastic QFN	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 70\text{V}$ ,  $V^- = -70\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$ ,  $V_{\text{OD}} = \text{open}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		I-SUFFIX			H-SUFFIX			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{\text{OS}}$	Input Offset Voltage		●		$\pm 330$ $\pm 330$	$\pm 1000$ $\pm 1250$		$\pm 330$ $\pm 330$	$\pm 1000$ $\pm 1250$	$\mu\text{V}$ $\mu\text{V}$
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift	$T_A = 25^\circ\text{C}$ , $\Delta T_J = 70^\circ\text{C}$		-5	$\pm 3$	5	-5	$\pm 3$	5	$\mu\text{V}/^\circ\text{C}$
$I_{\text{B}}$	Input Bias Current (Note 6)	Supply Voltage = $\pm 70\text{V}$ Supply Voltage = $\pm 15\text{V}$ Supply Voltage = $\pm 15\text{V}$	●		3 0.3			3 0.3		pA pA pA
$I_{\text{OS}}$	Input Offset Current (Note 6)	Supply Voltage = $\pm 15\text{V}$	●		0.5	30		0.5	120	pA pA
$e_{\text{n}}$	Input Noise Voltage Density	$f = 1\text{kHz}$ $f = 10\text{kHz}$			14 11			14 11		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
	Input Noise Voltage	0.1Hz to 10Hz			3.5			3.5		$\mu\text{V}_{\text{P-P}}$
$i_{\text{n}}$	Input Noise Current Density				1			1		$\text{fA}/\sqrt{\text{Hz}}$
$V_{\text{CM}}$	Input Common Mode Range	Guaranteed by CMRR	●	$V^- + 3\text{V}$	$\pm 68$	$V^+ - 3\text{V}$	$V^- + 3\text{V}$	$\pm 68$	$V^+ - 3\text{V}$	V V
$C_{\text{IN}}$	Common Mode Input Capacitance				9			9		pF
$C_{\text{DIFF}}$	Differential Input Capacitance				5			5		pF
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -67\text{V}$ to $67\text{V}$	●	130 126	$>140$		130 126	$>140$		dB dB
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = \pm 4.75\text{V}$ to $\pm 70\text{V}$	●	112 106	$>120$		112 106	$>120$		dB dB
$V_{\text{OUT}}$	Output Voltage Swing High (Referred to $V^+$ ) ( $V_{\text{OH}}$ )	No Load $I_{\text{SOURCE}} = 1\text{mA}$ $I_{\text{SOURCE}} = 10\text{mA}$	● ● ●		10 50 450	25 140 1000		10 50 450	25 140 1000	mV mV mV
	Output Voltage Swing Low (Referred to $V^-$ ) ( $V_{\text{OL}}$ )	No Load $I_{\text{SINK}} = 1\text{mA}$ $I_{\text{SINK}} = 10\text{mA}$	● ● ●		10 30 250	25 80 600		10 30 250	25 80 600	mV mV mV
$A_{\text{VOL}}$	Large-Signal Voltage Gain	$R_{\text{L}} = 10\text{k}$ $V_{\text{OUT}}$ from $-60\text{V}$ to $60\text{V}$	●	1000 1000	$>10000$		1000 1000	$>10000$		V/mV V/mV
$I_{\text{SC}}$	Output Short-Circuit Current (Source and Sink)	Supply Voltage = $\pm 70\text{V}$ Supply Voltage = $\pm 15\text{V}$	●	50	90		50	90		mA mA
SR	Slew Rate	$A_{\text{VCL}} = -4$ , $R_{\text{L}} = 10\text{k}$	●	10	21		9	21		V/ $\mu\text{s}$ V/ $\mu\text{s}$
GBW	Gain-Bandwidth Product	$f_{\text{TEST}} = 20\text{kHz}$ , $R_{\text{L}} = 10\text{k}$	●	5.5	12		5	12		MHz MHz
$\phi_{\text{M}}$	Phase Margin	$R_{\text{L}} = 10\text{k}$ , $C_{\text{L}} = 50\text{pF}$			60			60		Deg
FPBW	Full-Power Bandwidth	$V_{\text{OUT}} = 125\text{V}_{\text{P-P}}$	●	20	40		18	40		kHz kHz
$t_{\text{S}}$	Settling Time 0.1%	$V_{\text{STEP}} = 1\text{V}$ , $A_{\text{V}} = 1$ , $R_{\text{L}} = 10\text{k}$			2			2		$\mu\text{s}$
$I_{\text{S}}$	Supply Current (Per Amplifier)	No Load	●		2.8	3.9 4.3		2.8	3.9 4.3	mA mA
$V_{\text{S}}$	Supply Voltage Range	Guaranteed by the PSRR Test	●	9.5		140	9.5		140	V

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 70\text{V}$ ,  $V^- = -70\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$ ,  $V_{\text{OD}} = \text{open}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		I-SUFFIX			H-SUFFIX			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{\text{ODH}}$	$\overline{\text{OD}}$ Pin Voltage, Referenced to COM Pin	$V_{\text{IH}}$	●	COM + 1.8V			COM + 1.8V			V
$\overline{\text{ODL}}$	$\overline{\text{OD}}$ Pin Voltage, Referenced to COM Pin	$V_{\text{IL}}$	●			COM + 0.65V			COM + 0.65V	V
	Amplifier DC Output Impedance, Disabled	DC, $\overline{\text{OD}} = \text{COM}$			>10			>10		$\text{M}\Omega$
COMCM	COM Pin Voltage Range		●	$V^-$		$V^+ - 5$	$V^-$		$V^+ - 5$	V
COMV	COM Pin Open-Circuit Voltage		●	17	21	25	17	21	25	V
COMR	COM Pin Resistance		●	500	665	850	500	665	850	$\text{k}\Omega$
TEMPF	Die Temperature Where TFLAG Is Active				145			145		$^\circ\text{C}$
TEMPHYS	TFLAG Output Hysteresis				5			5		$^\circ\text{C}$
$I_{\text{TFLAG}}$	TFLAG Pull-Down Current	TFLAG Output Voltage = 0V	●	70	200	330	70	200	330	$\mu\text{A}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Either output (OUTA or OUTB) of the LTC6091 is capable of producing peak output currents in excess of 50mA. Current density limitations within the IC require the continuous RMS current supplied by either output (sourcing or sinking) over the operating lifetime of the part to be limited to under 50mA (absolute maximum). Proper heat sinking may be required to keep the junction temperature below the absolute maximum rating. Refer to the Power Dissipation and Thermal Considerations section of the data sheet for more information.

**Note 3:** The LTC6091I is guaranteed functional over the operating junction temperature range  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6091H is guaranteed functional over the operating junction temperature range  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . Specifying the junction temperature range as an operating condition is applicable for devices with potentially significant quiescent power dissipation.

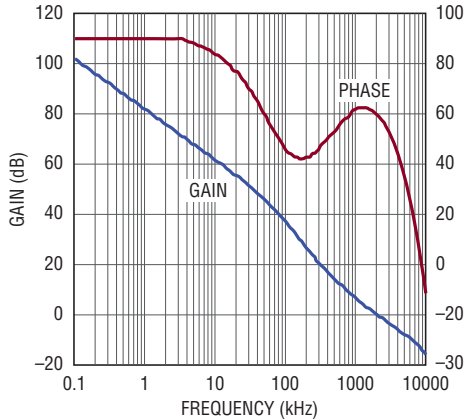
**Note 4:** The LTC6091I is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6091H is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 5:** This device includes overtemperature protection that is intended to protect the device during momentary overload conditions. Operation above the specified maximum operating junction temperature is not recommended.

**Note 6:** Input bias and offset current is production tested with  $\pm 15\text{V}$  supplies. See Typical Performance Characteristics curves of actual typical performance over full supply range.

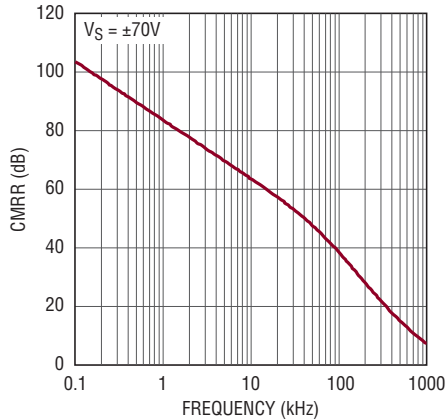
## TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Gain and Phase vs Frequency



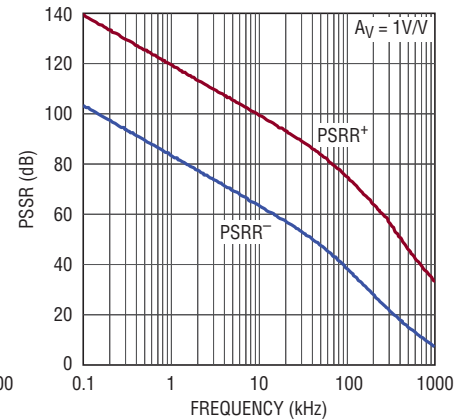
6091 G01

CMRR vs Frequency



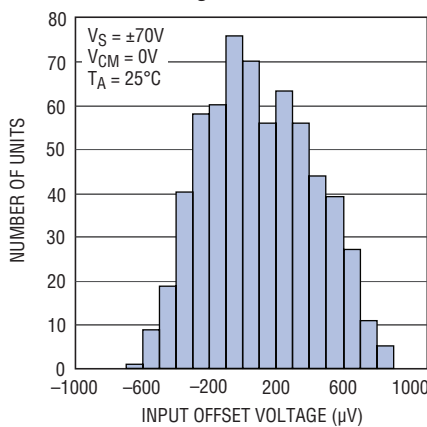
6091 G02

PSRR vs Frequency



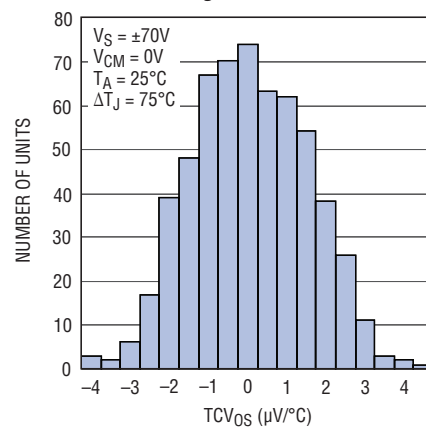
6091 G03

Offset Voltage Distribution



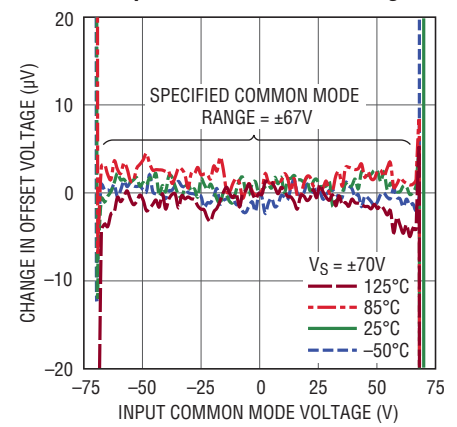
6091 G04

Offset Voltage Drift Distribution



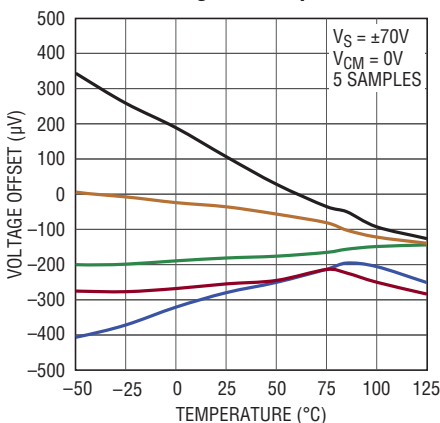
6091 G05

Change in Offset Voltage vs Input Common Mode Voltage



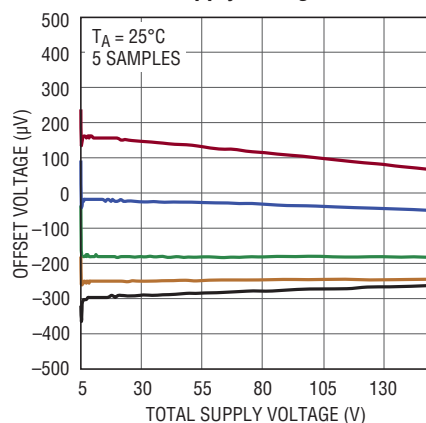
6091 G06

Offset Voltage vs Temperature



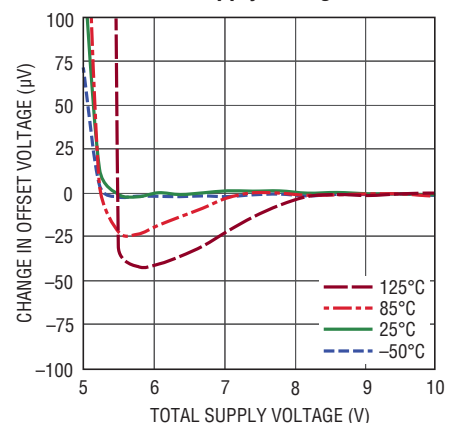
6091 G07

Offset Voltage vs Total Supply Voltage



6091 G08

Minimum Supply Voltage

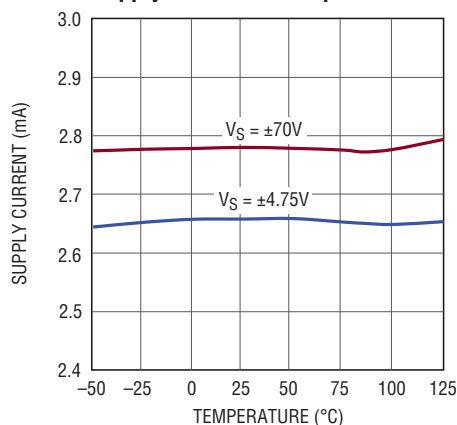


6091 G09

6091fa

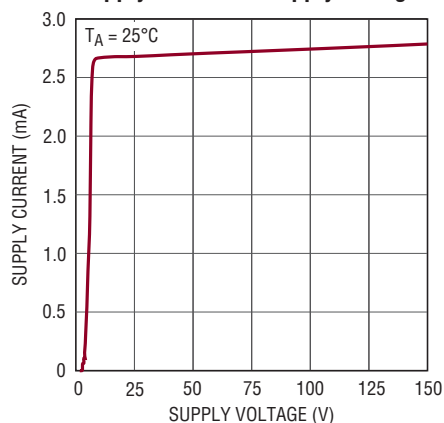
## TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



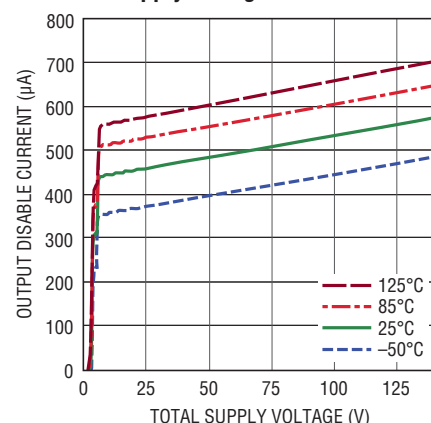
6091 G10

Supply Current vs Supply Voltage



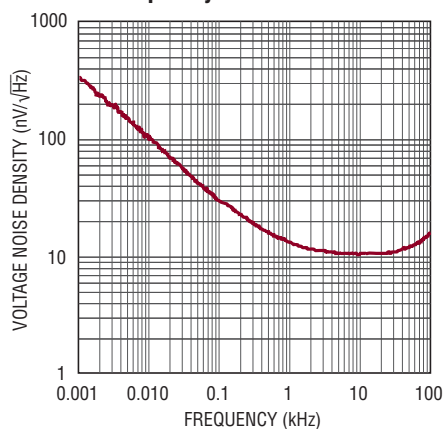
6091 G11

Output Disable Supply Current vs Supply Voltage



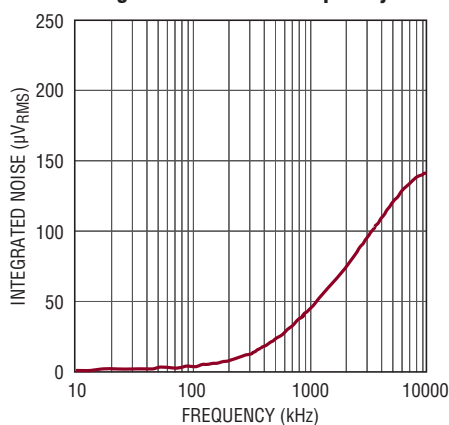
6091 G12

Voltage Noise Density vs Frequency



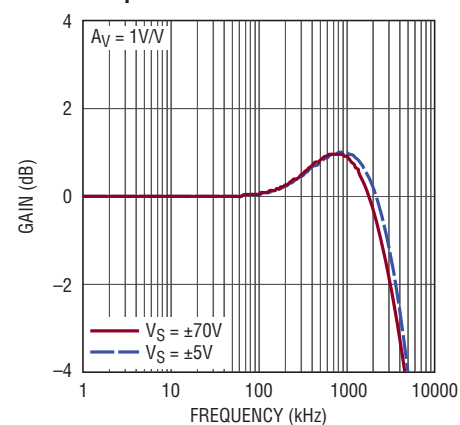
6091 G13

Integrated Noise vs Frequency



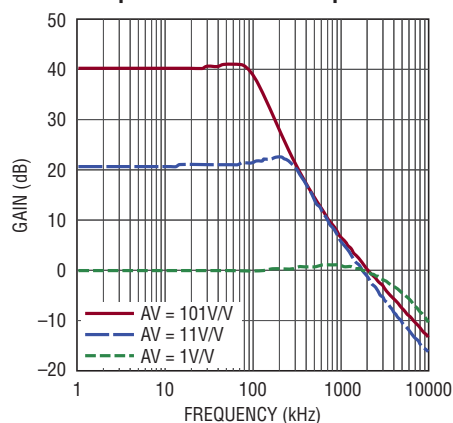
6091 G14

Small-Signal Frequency Response



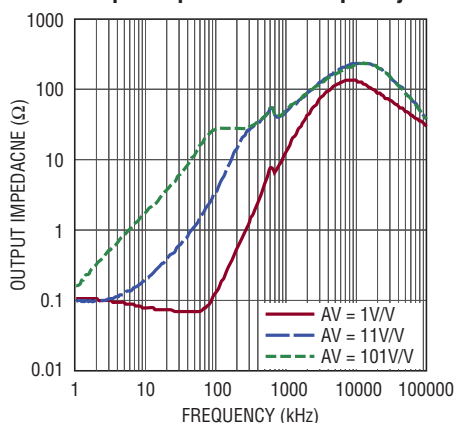
6091 G15

Small-Signal Frequency Response vs Closed-Loop Gain



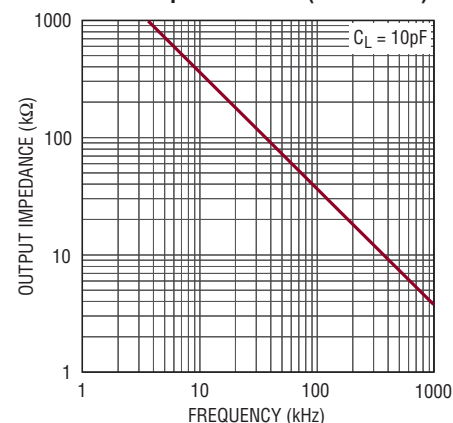
6091 G16

Output Impedance vs Frequency



6091 G17

Output Impedance vs Frequency with Output Disabled (OD = COM)

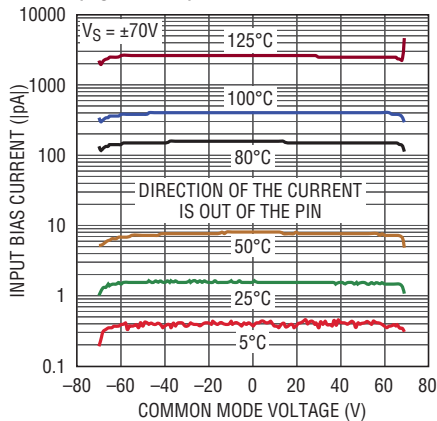


6091 G18

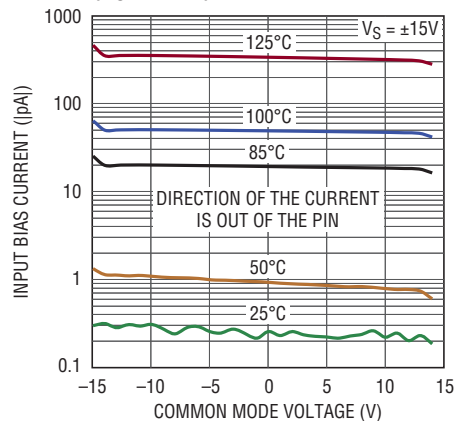
6091fa

# TYPICAL PERFORMANCE CHARACTERISTICS

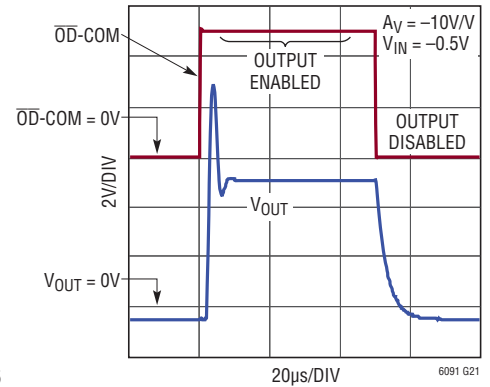
**Input Bias Current vs Common Mode Voltage and Temperature ( $V_S = \pm 70V$ )**



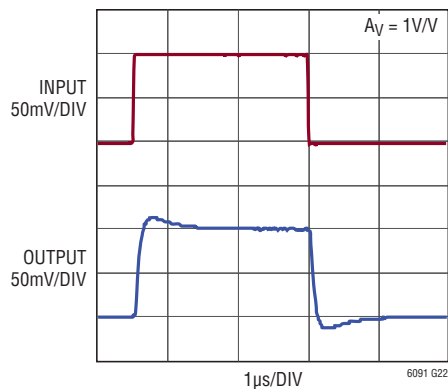
**Input Bias Current vs Common Mode Voltage and Temperature ( $V_S = \pm 15V$ )**



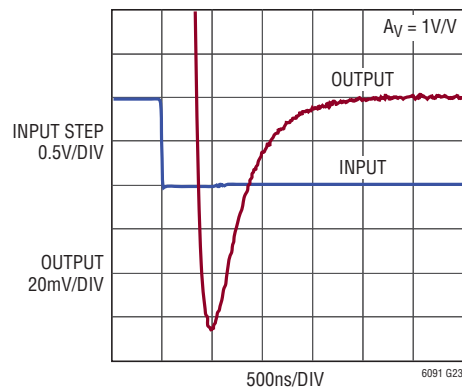
**Output Disable ( $\overline{OD}$ ) Response Time**



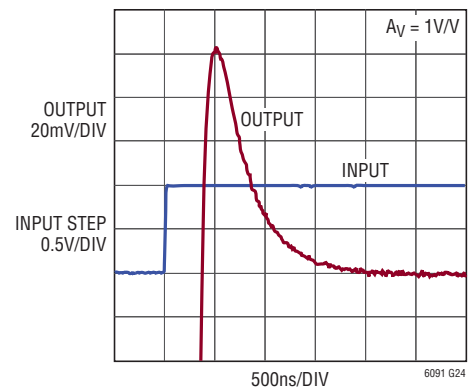
**Small-Signal Transient Response**



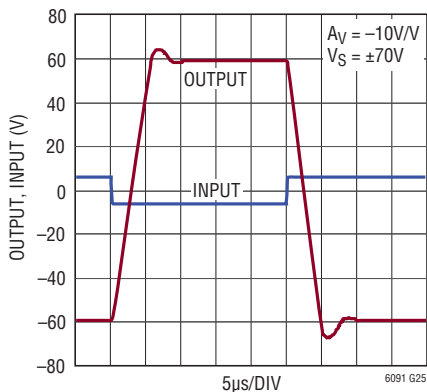
**Falling Edge Settling Time**



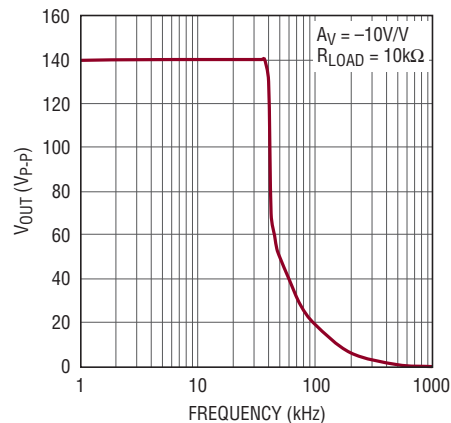
**Rising Edge Settling Time**



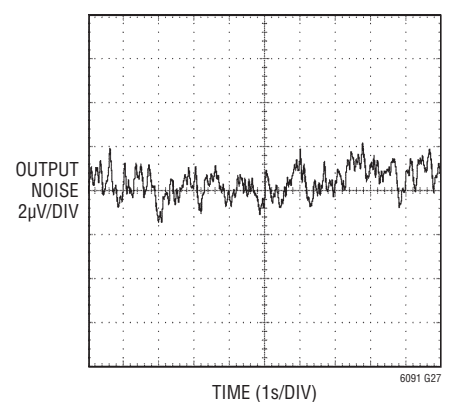
**Large-Signal Transient Response**



**Output Voltage Swing vs Frequency**

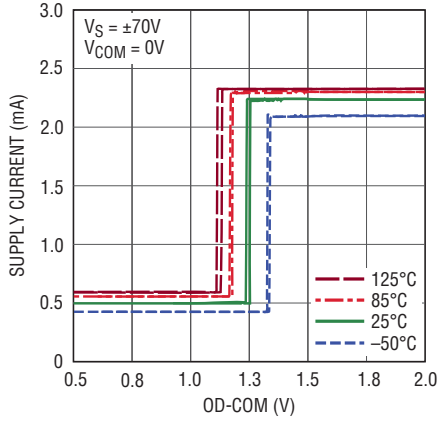


**0.1Hz to 10Hz Voltage Noise**

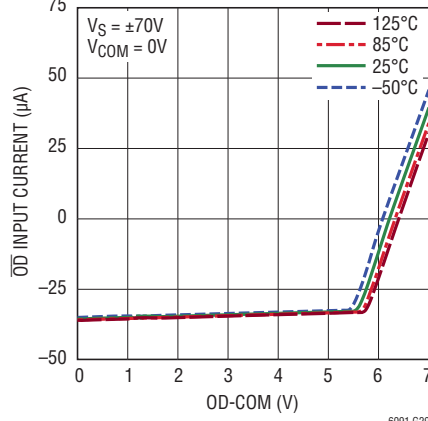


# TYPICAL PERFORMANCE CHARACTERISTICS

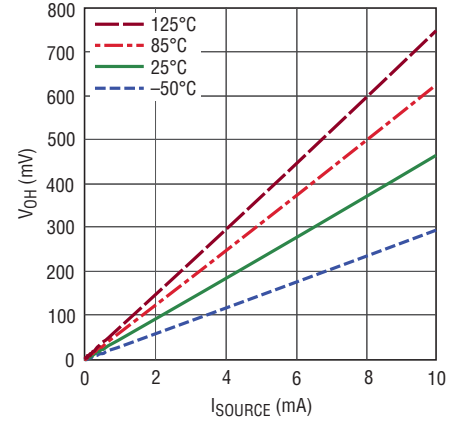
Supply Current vs  $\overline{OD}$  Pin Voltage



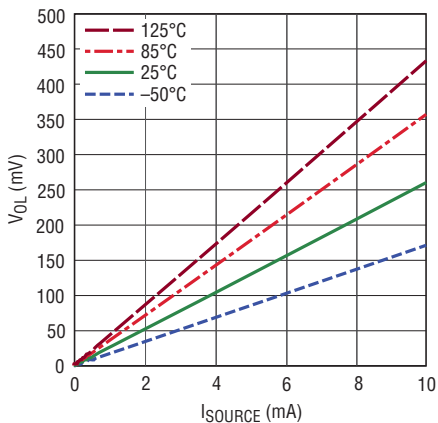
$\overline{OD}$  Pin Input Current vs  $\overline{OD}$  Pin Voltage



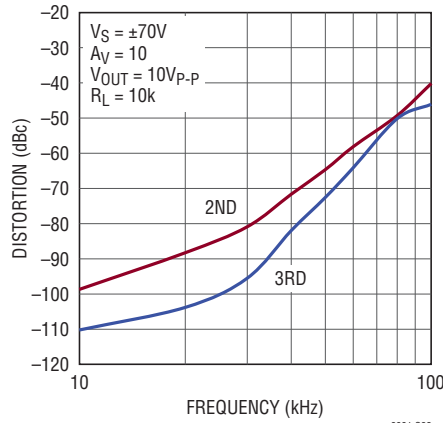
Output Voltage Swing High ( $V_{OH}$ ) vs Load Current and Temperature



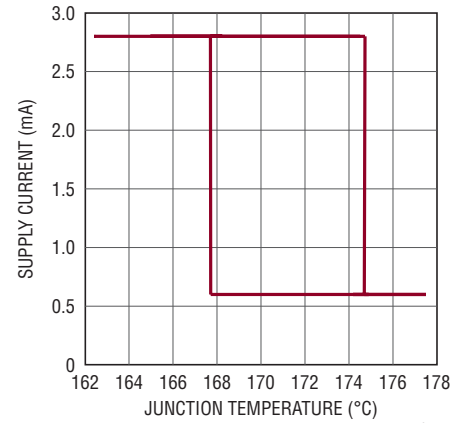
Output Voltage Swing Low ( $V_{OL}$ ) vs Load Current and Temperature



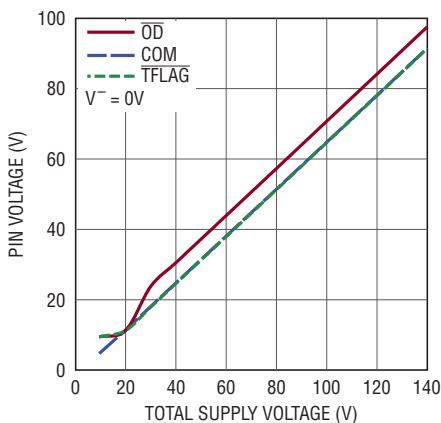
Distortion vs Frequency



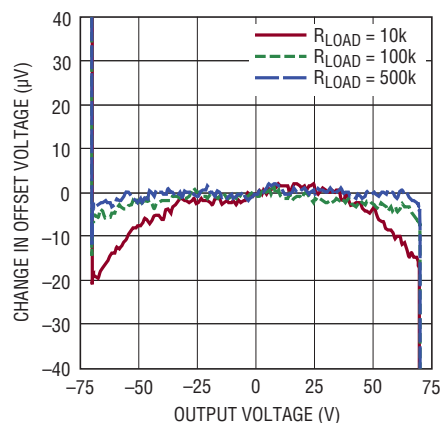
Thermal Shutdown Hysteresis



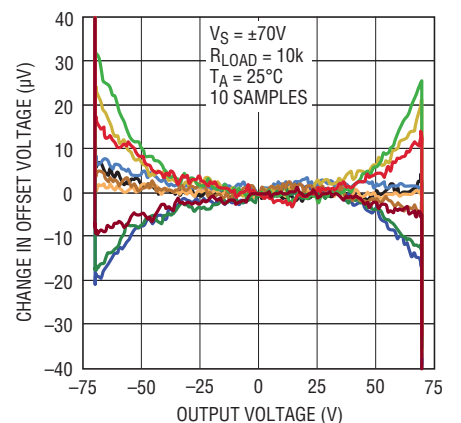
Open-Circuit Voltage of COM,  $\overline{OD}$ , TFLAG



Open-Loop Gain vs Load Resistance



Open-Loop Gain



## PIN FUNCTIONS (A Channel/B Channel)

**–INA, –INB (Pin 1/Pin 5):** Inverting Input Pin. Input common mode range is  $V^- + 3V$  to  $V^+ - 3V$ . Do not exceed absolute maximum voltage range.

**+INA, +INB (Pin 2/Pin 6):** Noninverting Input Pin. Input common mode range is  $V^- + 3V$  to  $V^+ - 3V$ . Do not exceed absolute maximum voltage range.

**$V^-$  (Pin 3, Pin 7, Exposed Pad Pin 17):** Negative Supply Pin. Connect to a single  $V^-$  only. Both amplifiers share a common substrate, and are not isolated from each other. Pins 3, and 7 must be electrically tied to the exposed pad (Pin 17). The exposed pad connection removes heat from the device. To achieve a low thermal resistance, connect the exposed pad to a  $V^-$  power plane with as much metal land as possible (see Applications Information).

**$\overline{TFLAGA}$ ,  $\overline{TFLAGB}$  (Pin 12/ Pin 8):** Temperature Flag Pin. The TFLAG pin is an open-drain output that sinks current when the die temperature exceeds 145°C.

**OUTA, OUTB (Pin 13/Pin 9):** Output Pin. If this rail-to-rail output goes below  $V^-$ , the ESD protection diode will forward bias. If OUT goes above  $V^+$ , then output device diodes will forward bias. Avoid forward biasing the diodes on the OUT pin. Excessive current can cause damage.

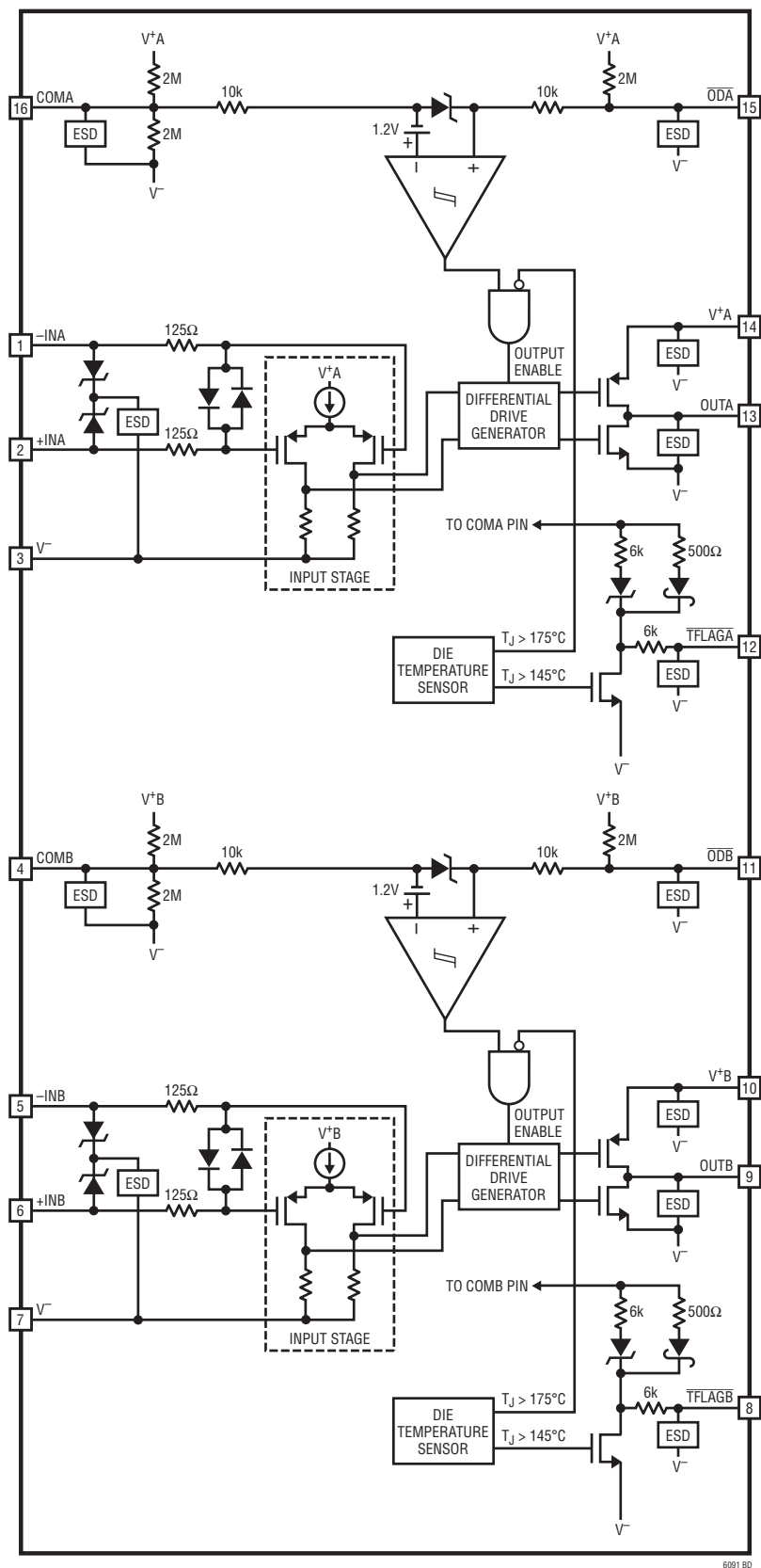
**$V^+A$ ,  $V^+B$  (Pin 14/Pin 10):** Positive Supply Pin. Each amplifier has an independent  $V^+$  supply. But since both amplifiers shares a common substrate, they must share the same  $V^-$  supply.

**$\overline{ODA}$ ,  $\overline{ODB}$  (Pin 15/Pin 11):** Output Disable Pin. Active low input disables the output stage. If left open, an internal pull-up resistor enables the amplifier. Input voltage levels are referred to the COM pin.

**COMA, COMB (Pin 16/Pin 4):** COM Pin is used to interface  $\overline{OD}$  and  $\overline{TFLAG}$  pins to voltage control circuits. Tie this pin to the low voltage ground, or let it float.



BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### General

The LTC6091 dual high voltage operational amplifier is designed in a Linear Technology proprietary CMOS process enabling a rail-to-rail output stage with a 140V supply while maintaining precision, low offset, low offset drift and low noise.

### Power Supply

The LTC6091 consists of single monolithic die containing two LTC6090 amplifiers assembled in a single exposed-pad QFN package. Since both amplifiers share the same substrate,  $V^-$  pins (Pin 3 and Pin 7) must be tied together and to the exposed pad underneath. The  $V^+A$  (Pin 14) and  $V^+B$  (Pin 10) may be supplied independently. The LTC6091 works off single or split supplies. Split supplies can be balanced or unbalanced. For example, two  $\pm 70V$  supplies can be used, or a 100V and  $-40V$  supply can be used. The  $V^+$  and  $V^-$  pins should be bypassed with high quality surface mount ceramic capacitors. See Board Layout section for recommendations. When using split supplies, supply sequencing does not cause problems.

### Input Protection

As shown in the Block Diagram, the LTC6091 has a comprehensive protection network to prevent damage to

the input devices. The current limiting resistors and back-to-back diodes are to keep the inputs from being driven apart. The voltage-current relationship is that of a resistor in series with a diode until the voltage difference between the pins reaches 12V. At that point the Zener diodes turn on. Any additional current into the pins will snap back the input differential voltage to 9V.

In the event of an ESD strike between an input and  $V^-$ , the voltage clamps and ESD device fire providing a current path to  $V^-$  protecting the input devices. The input pin protection is designed to protect against momentary ESD events. A repetitive large fast input swing ( $>5.5V$  and  $<20ns$  rise time) will cause repeated stress on the MOSFET input devices. When in such an application, anti-parallel diodes (1N4148) should be connected between the inputs to limit the swing.

### Output Disable

Each amplifier of the LTC6091 has its own output disable ( $\overline{OD}$ ) pin (Refer to Figure 1). The  $\overline{OD}$  pin is an active low disable with an internal 2M resistor that will pull up the  $\overline{OD}$  pin enabling the output stage. The  $\overline{OD}$  pin voltage is limited by an internal Zener diode tied between COM and  $\overline{OD}$ . When the  $\overline{OD}$  pin for a particular channel is asserted low with respect to its COM pin, the output stage for that

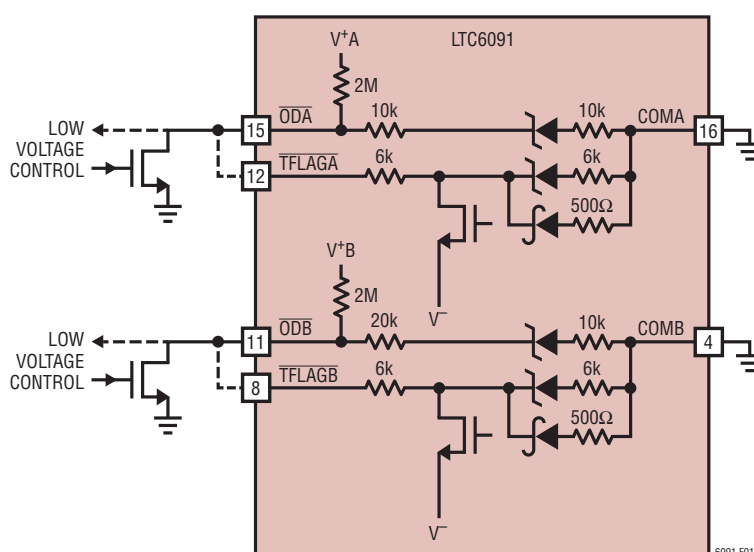


Figure 1. Low Voltage Interface Example for Output Disable

## APPLICATIONS INFORMATION

channel is disabled, leaving its bias and input circuits enabled. This results in  $580\mu\text{A}$  (typical) standby current for the disabled channel. The  $\overline{\text{OD}}$  pin can be directly connected to either an open drain NMOS device (as in Figure 1) or connected to low voltage logic circuitry.

Since the  $\overline{\text{OD}}$  pin is referenced to the COM pin, absolute maximum ratings should be observed for the COM and  $\overline{\text{OD}}$  pins. When coming out of shutdown the LTC6091 bias circuits and input stage are already powered up leaving only the output stage to turn on and drive to the proper output voltage. Figures 2 and 3 illustrate the part powering on and coming out of shutdown, respectively.

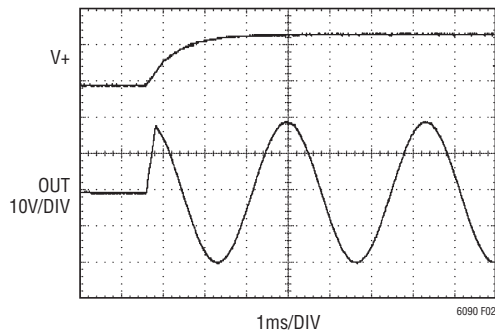


Figure 2. Starting Up

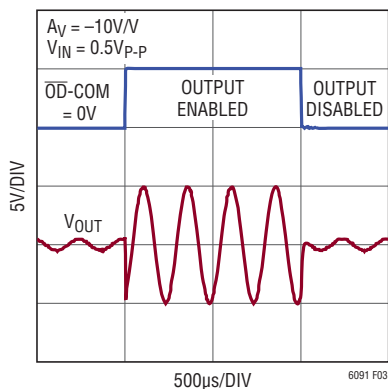


Figure 3. LTC6091 Output Disable Function

### Thermal Shutdown

Each amplifier of the LTC6091 has its own trimmed temperature sensing circuit which senses die temperature in close proximity to their respective amplifier's output stage, where most of the on-chip power dissipation occurs. When one of the amplifiers's sensing circuit senses temperatures in excess of approximately  $145^{\circ}\text{C}$ , it will assert the  $\overline{\text{TFLAG}}$  pin for that amplifier. The  $\overline{\text{TFLAG}}$  pins are open-drain output pins that sink  $200\mu\text{A}$  (typical) each when asserted. The temperature sensor itself has approximately  $5^{\circ}\text{C}$  of hysteresis requiring the part to cool to approximately  $140^{\circ}\text{C}$  before disabling  $\overline{\text{TFLAG}}$ .

For simplest operation, float both channel's COM pins (COMA and COMB), and connect  $\overline{\text{ODA}}$  to  $\overline{\text{TFLAGA}}$ , and  $\overline{\text{ODB}}$  to  $\overline{\text{TFLAGB}}$  as shown in Figure 4. Both output stages will be safely disabled should the die temperature reach approximately  $145^{\circ}\text{C}$ . Both COM pins may be tied to ground.

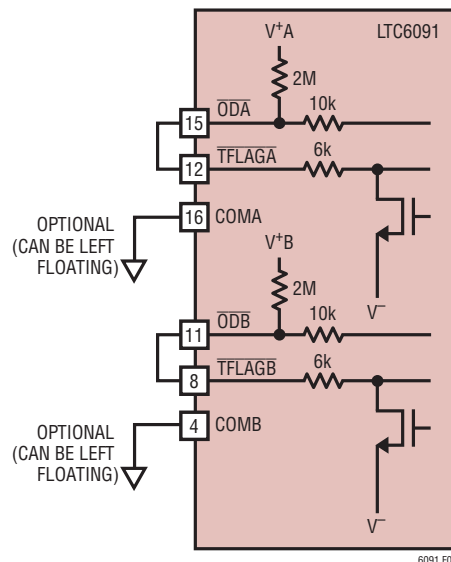


Figure 4. Automatic Thermal Output Disable Using the TFLAG Pins

## APPLICATIONS INFORMATION

Since both amplifiers share a common substrate, thermal cross coupling from one channel to the other will occur. Depending on the average die temperature, and temperature sensing accuracy, it is possible, however unlikely, for heat generated in Channel A's output stage to assert Channel B's  $\overline{\text{TFLAGB}}$  or visa-versa. Should this condition occur, it should be understood that both amplifiers are operating close to their thermal shutdown limit.

Since the  $\overline{\text{TFLAG}}$  pin is referenced to the COM pin, absolute maximum ratings should be observed for the COM and  $\overline{\text{TFLAG}}$  pins.

For safety, a second overtemperature threshold shuts down the output stage if internal die temperatures rise to approximately 175°C. This second overtemperature indicator has approximately 7°C of hysteresis requiring the die temperature to cool 7°C. Once the device has cooled sufficiently, the output stage will enable. **Degradation can occur or reliability may be affected when the junction temperature of the device exceeds 150°C.**

### Board Layout

Because the two amplifiers share a common substrate, a single bypass capacitor of 0.1 $\mu\text{F}$  can be used to bypass the  $V^-$  (as close to the pins as possible) to a low impedance ground plane. Additional bypass capacitance may be required for heavy loads. For the positive supplies, there are two independent positive supply pins ( $V^+A$ ,  $V^+B$ ): one for each amplifier. If these two supplies are tied together, they may be bypassed to a low impedance ground plane with a single capacitor (typically 0.1 $\mu\text{F}$ ) as close to the supply pins as possible. Likewise, when driving heavy loads, additional bypass capacitance may be required.

There are other important considerations for high voltage and high power: trace spacing, humidity and dust. High voltage electric fields between adjacent conductors attract dust. Moisture absorbed by dust can contribute to PCB leakage and electrical breakdown. Vias biased to high voltage should have additional spacing to nearby ground plane.

PCB leakage related errors require special layout and cleaning practices. As little as 1000G $\Omega$  of PCB leakage between Pin 2 ( $+INA$ ) and Pin 3 ( $V^-$ ) will generate 70pA of leakage with  $\pm 70\text{V}$  power supplies! It becomes important to clean the PCB after soldering down the part. Solder flux will accumulate dust and become a leakage hazard. It is recommended to clean the PCB with a solvent, or simply use soap and water to remove residue. Baking the PCB will remove leftover moisture. Depending on the application, a special low leakage board material may be considered. Also guarding sensitive traces as shown in Figures 5 and 6 to the greatest extent possible will also help to mitigate PCB leakage.

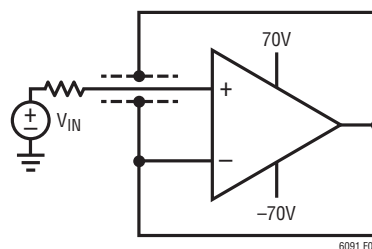


Figure 5. Example of a Noninverting Amplifier Guard Configuration

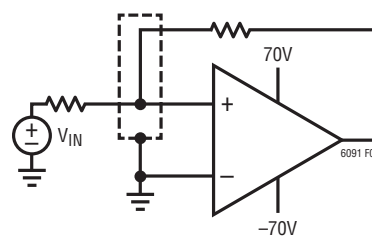


Figure 6. Example of an Inverting Amplifier Guard Configuration

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Power Dissipation and Thermal Considerations

In order to avoid damaging the device, the absolute maximum junction temperature of the LTC6091 ( $T_{JMAX} = 150^{\circ}\text{C}$ ), should not be exceeded. At 5.6mA of quiescent supply current on  $\pm 70\text{V}$  supplies, the LTC6091 will consume approximately 0.8W.

In general, the die’s junction temperature ( $T_J$ ) can be estimated from the ambient temperature  $T_A$ , and the power dissipated in the device  $P_D$ :

$$T_J = T_A + P_D \cdot (\theta_{JC} + \theta_{CA})$$

$\theta_{JC}$  is the junction-to-case thermal resistance and is characterized to be approximately  $15^{\circ}\text{C/W}$ .  $\theta_{CA}$  is the case-to-ambient thermal resistance and depends on circuit board layout, air flow and proximity to other sources of heat. The power dissipated in the IC is a function of supply voltage and the load being driven. Assuming split supplies, and a resistive load, the worst-case power dissipation  $P_{D(MAX)}$  occurs when the output is driving the load to half of either supply voltage.  $P_{D(MAX)}$ , then is the sum of the quiescent power plus the power dissipated in the device due to the load with symmetric supply:

$$P_{D(MAX)} \text{ (per amplifier)} = (V_S \cdot I_S) + (V_S/4)^2/R_{LOAD}$$

( $I_S$  is the quiescent supply current for a single amplifier)

For example, the resulting peak power dissipation in the LTC6091 for 2 channels driving  $5\text{k}\Omega$  to ground with a  $\pm 70\text{V}$  supply would be approximately 1.3W.

The exposed pad under the LTC6091 is the primary conduit for conducting heat out of the package. Junction-to-ambient thermal resistance is strongly influenced by the number of thermal vias to which the exposed pad is soldered to, the size of the thermal plane connected to these thermal vias, PCB thickness, air-flow, and proximity of other sources of heat. To minimize the amount of temperature rise within the package, the exposed pad must be soldered down to a PCB with multiple thermal vias tied to a thermal plane.

For a 4-layer PCB with the exposed pad of the LTC6091 soldered to a land pattern containing eight 10mil diameter thermal vias which are connected to two 2 inch by 2 inch  $V^-$  thermal/power planes, the junction-to-ambient thermal resistance may be as low as  $38^{\circ}\text{C/W}$  in still air. If the density of the PCB layout makes such large thermal planes impractical, Table 1 lists the thermal performance achieved of alternative layout examples. A minimally sized single layer thermal land under the device as shown in column D of Table 1 will result in a junction-to-ambient thermal resistance approaching  $115^{\circ}\text{C/W}$ . Since the LTC6091 will dissipate 0.8W on  $\pm 70\text{V}$  supplies, there will

Table 1. Thermal Resistance vs PCB Thermal Plane Area

EXAMPLE A TOP LAYER A	EXAMPLE B TOP LAYER B	EXAMPLE C TOP LAYER C	EXAMPLE D TOP LAYER D
BOTTOM LAYER A	BOTTOM LAYER B	BOTTOM LAYER C	BOTTOM LAYER D
$\theta_{JA} = 90^{\circ}\text{C/W}$ $\theta_{JC} = 15^{\circ}\text{C/W}$ $\theta_{CA} = 75^{\circ}\text{C/W}$	$\theta_{JA} = 100^{\circ}\text{C/W}$ $\theta_{JC} = 15^{\circ}\text{C/W}$ $\theta_{CA} = 85^{\circ}\text{C/W}$	$\theta_{JA} = 108^{\circ}\text{C/W}$ $\theta_{JC} = 15^{\circ}\text{C/W}$ $\theta_{CA} = 93^{\circ}\text{C/W}$	$\theta_{JA} = 115^{\circ}\text{C/W}$ $\theta_{JC} = 15^{\circ}\text{C/W}$ $\theta_{CA} = 100^{\circ}\text{C/W}$

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## APPLICATIONS INFORMATION

be approximately 90°C of junction-to-ambient temperature rise due to the device operation alone. This will then limit the specified ambient temperature range of the LTC6091 can operate and/or will limit the load driven to prevent junction temperatures from exceeding  $T_{JMAX}$  (150°C).

### Stability with Large Resistor Values

A large feedback resistor along with the intrinsic input capacitance will create an additional pole that affects stability and causes peaking in the closed-loop response. To mitigate the peaking a small feedback capacitor placed around the feedback resistor, as shown in Figure 7, will reduce the peaking and overshoot. Figure 8 shows the

closed-loop response with various feedback capacitors. Additional stray capacitance on the input pins should be kept to a minimum.

### Slew Enhancement

The LTC6091 includes a slew enhancement circuit which boosts the slew rate to 21V/μs making the part capable of slewing rail-to-rail across the 140V output range in less than 7μs. To optimize the slew rate and minimize settling time, stray capacitance should be kept to a minimum. A feedback capacitor reduces overshoot and nonlinearities associated with the slew enhancement circuit. The size of

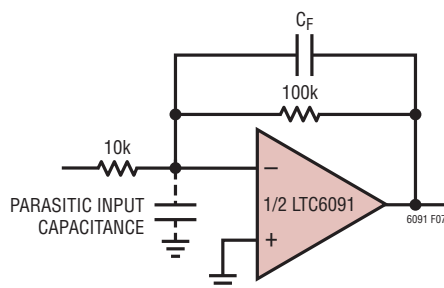


Figure 7. LTC6091 with Feedback Capacitance to Reduce Peaking

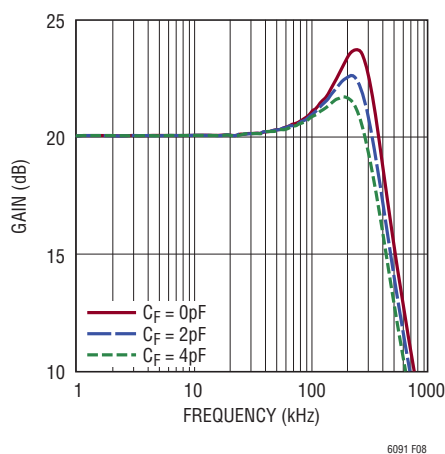


Figure 8. Compensated Closed-Loop Response Reduces Peaking

## APPLICATIONS INFORMATION

the feedback capacitor should be tailored to the specific board, supply voltage and load conditions.

Slewing is a nonlinear behavior and will affect distortion. The relationship between slew rate and full-power bandwidth is given in the relationship below.

$$SR = V_{PEAK} \cdot \omega$$

where  $V_{PEAK}$  is the peak output voltage and  $\omega$  is frequency in radians/sec. The fidelity of a large sine wave output is limited by the slew rate. The graph in Figure 9 shows distortion versus frequency for several output levels.

### Multiplexer Application

A single LTC6091 may be arranged to act as a 2-channel high voltage analog multiplexer as shown in Figure 10. When used in this arrangement, it is possible for the output to affect the source on the disabled amplifier's noninverting input. The inverting and noninverting inputs are clamped through resistors and back-to-back diodes. There is a path for current to flow from the multiplexer output through the disabled amplifier's feedback resistor, and through the inputs to the noninverting input's source.

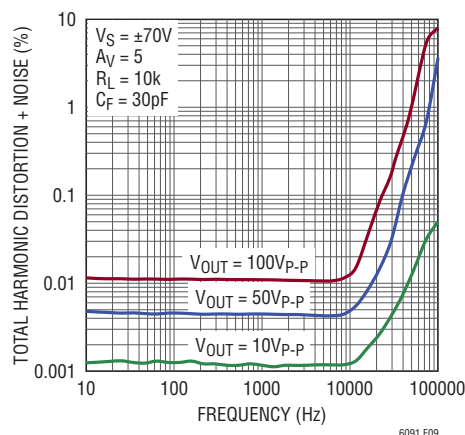


Figure 9. Distortion vs Frequency for Large Output Swings

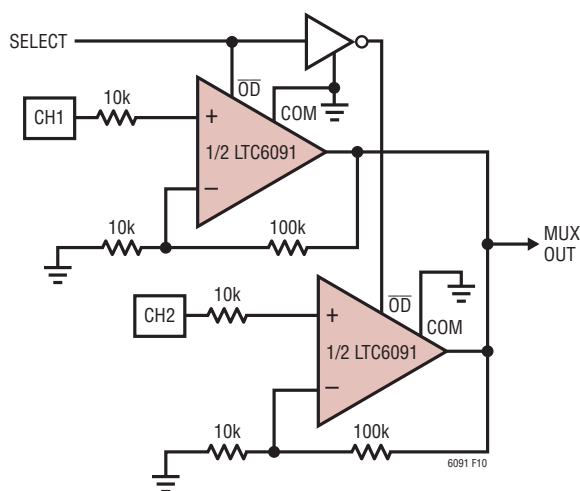


Figure 10. Multiplexer Application

## APPLICATIONS INFORMATION

For example, if the enabled amplifier has a  $-70V$  output, and the disabled amplifier has a  $5V$  input, there is  $75V$  across the two resistors and the input pins. To keep this current below  $1mA$  the combined resistance of the  $R_{IN}$  and feedback resistor needs to be about  $75k$  or higher.

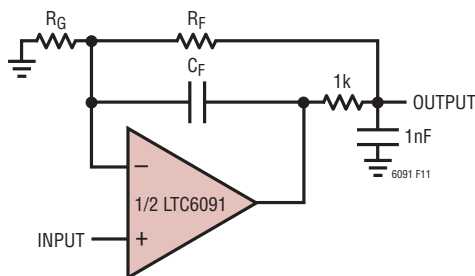
The output impedance of the disabled amplifier is  $> 10M\Omega$  at DC. The AC output impedance is shown in the Typical Performance Characteristics section.

### Minimizing Noise

The LTC6091 circuit shown in Figure 11 includes an output filter that reduces noise (and signals) starting at about  $150kHz$ . This filtering reduces out-of-band noise to a relatively insignificant level. Loop compensation is included to provide a well-stabilized overall response. Since the large-signal bandwidth is dictated largely by the op amp slew rate to signals below about  $100kHz$ , the net result is that little is compromised due to the added filtration.

The following table shows the suggested component values for a range of amplification factors.

GAIN	$R_G$	$R_F$	$C_F$
1	N/A	4.99k	330pF
2	50k	50k	33pF
5	20k	80.6k	22pF
10	11k	100k	18pF
20	5.23k	100k	18pF
50	2.05k	100k	18pF
100	1k	100k	18pF

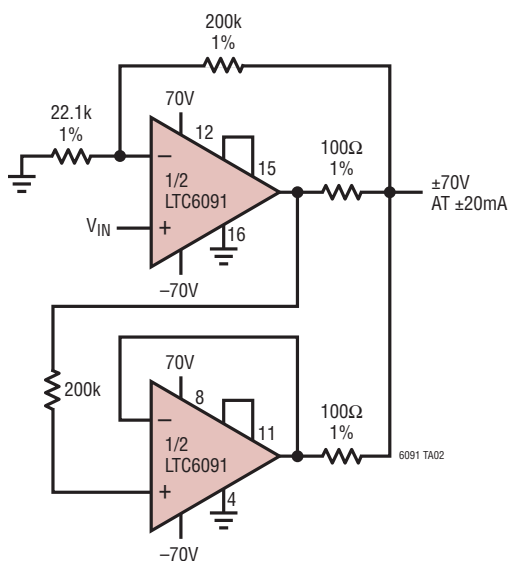


**Figure 11. Modified Gain-Block Application That Includes Noise-Reducing Filter**

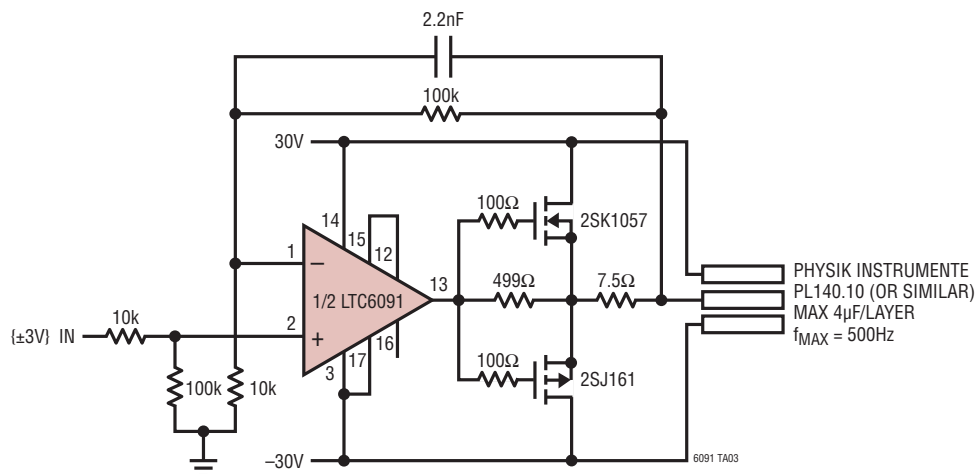


## TYPICAL APPLICATIONS

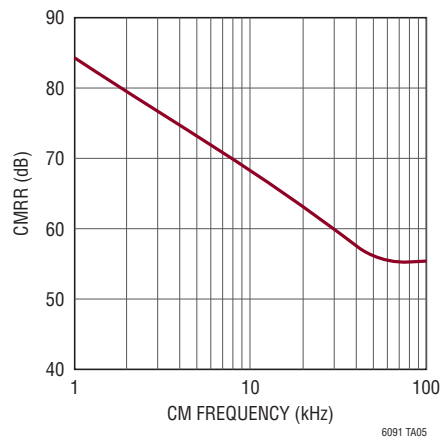
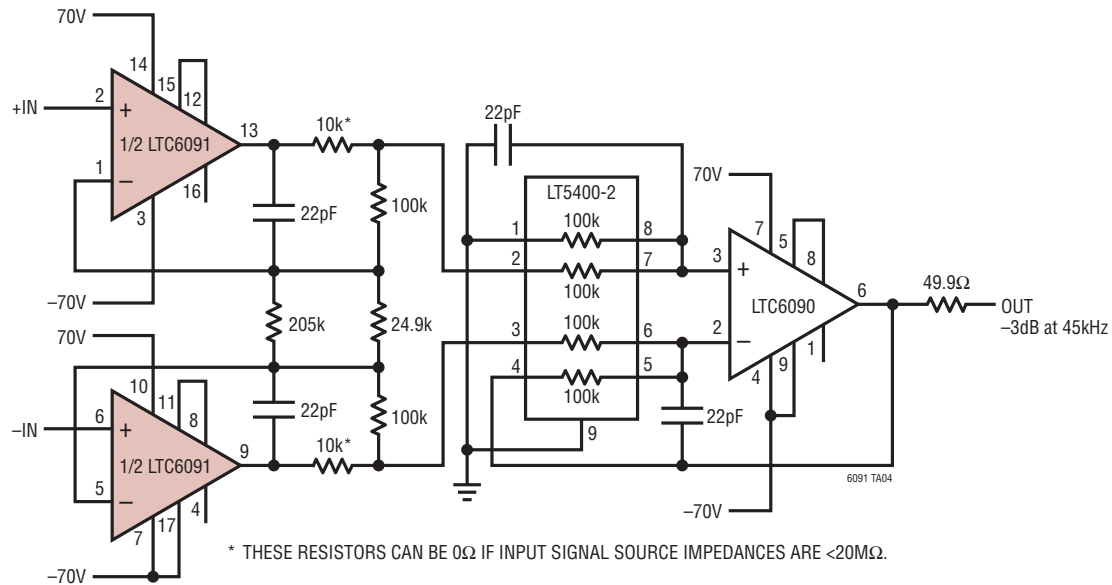
## Gain of 10 with Protected Output Current Doubler



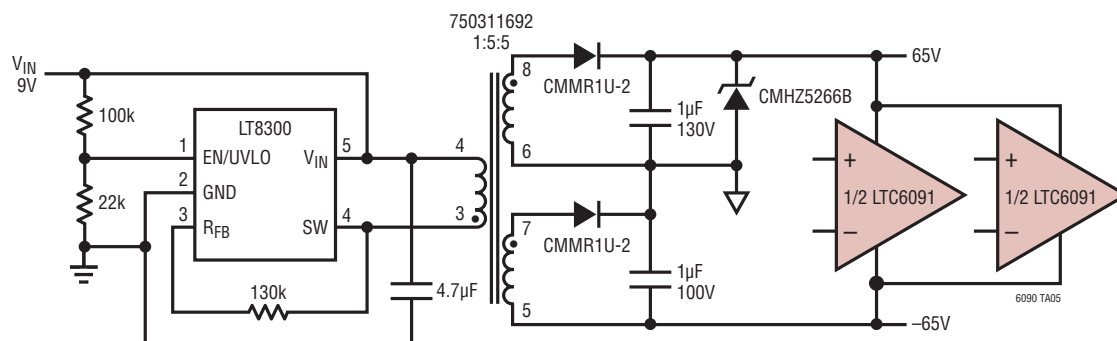
## Piezo Bimorph Bender Driver



## TYPICAL APPLICATIONS

Wide Common Mode Range 10x Gain Instrumentation Amplifier  
Typically <1mV Input-Referred Error

## 9V to ±65V Isolated Flyback Converter for Amplifier Supply





## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/15	Removed ESD statement to reflect improved ESD Performance	2
		Changed internal TFLAG circuit resistor values	10, 11, 12
		Updated Thermal Shutdown description	12
		Added pin numbers to application circuit	18

