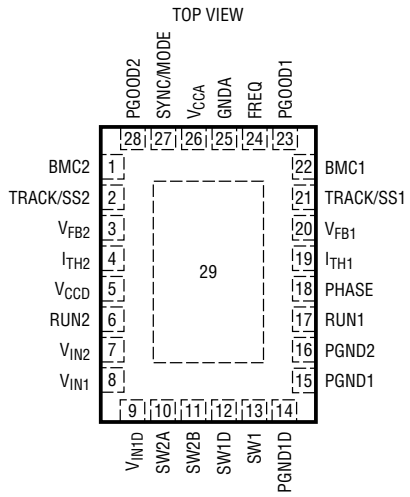
ABSOLUTE MAXIMUM RATINGS

(Note 1)

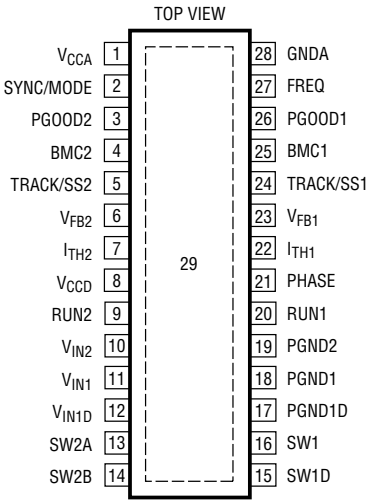
V_{IN1}, V_{IN1D}, V_{IN2}, V_{CCA}, V_{CCD} Voltages..... –0.3V to 6V
SYNC/MODE, SW1, SW1D, SW2A, SW2B,
RUN1, RUN2, V_{FB1}, V_{FB2}, PHASE, FREQ,
I_{TH1}, I_{TH2}, TRACK/SS1, TRACK/SS2, BMC1,
BMC2 Voltages .....–0.3V to (V_{IN1} or V_{IN2}) + 0.3V

Maximum Difference Between Any of
V_{IN1}, V_{IN1D}, V_{IN2}, V_{CCA}, V_{CCD} 0.3V
PGOOD1, PGOOD2 Voltage..... –0.3V to 6V
Operating Junction Temperature Range
(Notes 2, 6, 7).....–40°C to 125°C
Storage Temperature Range.....–65°C to 125°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 29) IS GNDD



FE PACKAGE
28-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 29) IS GNDD MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LTC3546#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3546EUFD#PBF	LTC3546EUFD#TRPBF	3546	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC3546IUFD#PBF	LTC3546IUFD#TRPBF	3546	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3546EFE#PBF	LTC3546EFE#TRPBF	LTC3546FE	28-Lead Plastic TSSOP	–40°C to 85°C
LTC3546IFE#PBF	LTC3546IFE#TRPBF	LTC3546FE	28-Lead Plastic TSSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3546EUFD	LTC3546EUFD#TR	3546	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC3546IUFD	LTC3546IUFD#TR	3546	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3546EFE	LTC3546EFE#TR	LTC3546FE	28-Lead Plastic TSSOP	–40°C to 85°C
LTC3546IFE	LTC3546IFE#TR	LTC3546FE	28-Lead Plastic TSSOP	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{CCA} = 3.6V, unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1}, V_{IN1D}, V_{IN2}, V_{CCA}, V_{CCD}	Operating Voltage Range	V_{IN1} = V_{IN1D} = V_{IN2} = V_{CCA} = V_{CCD}		2.3		5.5	V
I_{FB1}, I_{FB2}	Feedback Pin Input Current	(Note 3)				±0.1	µA
V_{FB1}, V_{FB2}	Feedback Voltage	(Note 3)	●	0.588	0.6	0.612	V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation %/V is The Percentage Change in V_{OUT} with a Change in V_{IN}	V_{IN} = 2.3V to 5.5V (Note 3)			0.04	0.2	%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	I_{TH1}, I_{TH2} = 0.36V (Note 3) I_{TH1}, I_{TH2} = 0.84V (Note 3)	● ●		0.02 –0.02	0.2 –0.2	% %
$g_{m(EA)}$	Error Amplifier Transconductance	(Note 3)			1400		µS
$V_{TRACK/SS1}$, $V_{TRACK/SS2}$	Tracking Voltage Offset	$V_{TRACK/SS1,2}$ = 0.3V				15	mV
$I_{TRACK/SS1}$, $I_{TRACK/SS2}$	Tracking Current Source	$V_{TRACK/SS1,2}$ = 0V		0.8	1.15	1.5	µA
I_S	Input DC Supply Current (Note 4)						
	Active Mode	V_{FB1} = V_{FB2} = 0.55V, V_{MODE} = V_{IN}, V_{RUN1} = V_{RUN2} = V_{IN}			600	990	µA
	Half Active Mode (V_{RUN1} = V_{IN}, V_{RUN2} = 0)	V_{FB1} = 0.55V, V_{MODE} = V_{IN}, V_{RUN1} = V_{IN}, V_{RUN2} = 0V			400	800	µA
	Half Active Mode (V_{RUN1} = 0, V_{RUN2} = V_{IN})	V_{FB2} = 0.55V, V_{MODE} = V_{IN}, V_{RUN1} = 0V, V_{RUN2} = V_{IN}			400	800	µA
	Both Channels in Sleep Mode	V_{FB1} = V_{FB2} = 0.75V, V_{MODE} = V_{IN}, V_{RUN1} = V_{RUN2} = V_{IN}			160	300	µA
	Shutdown	V_{RUN1} = V_{RUN2} = 0V			0.2	1	µA
f_{OSC}	Oscillator Frequency	V_{FREQ}: R_T = V_{IN} V_{FREQ}: R_T = 143k V_{FREQ}: Resistor (Note 5)	 ● 	1.8 1.2 0.75	2.25 1.5 	2.9 1.8 4	MHz MHz MHz
I_{LIM1}	Peak Switch Current Limit on SW1 (1A)	BMC1 = V_{IN}, V_{ITH1} = 1.4V BMC1 = 0.4V, V_{ITH1} = 0V		1.4	1.6 0.45		A A
I_{LIM2}	Peak Switch Current Limit on SW2A/B (2A)	BMC2 = V_{IN}, V_{ITH1} = 1.4V BMC2 = 0.4V, V_{ITH1} = 0V		2.8	3.2 0.9		A A
$I_{LIM1+1D}$	Peak Switch Current Limit on SW1 + SW1D (2A)	SW1 Externally Connected to SW1D BMC1 = V_{IN} (Note 8) BMC1 = 0.4V (Note 8)		 2.5	 3.2 1.6		 A A
$I_{LIM2+1D}$	Peak Switch Current Limit on SW2A/B + SW1D (3A)	SW2A/B Externally Connected to SW1D BMC2 = V_{IN} (Note 8) BMC2 = 0.4V (Note 8)		 3.75	 4.8 2.4		 A A
$R_{DS(ON)1}$	SW1 Top Switch On-Resistance (1A) SW1 Bottom Switch On-Resistance	V_{IN2} = 3.6V V_{IN2} = 3.6V			0.19 0.18		Ω Ω
$R_{DS(ON)1D}$	SW1D Top Switch On-Resistance (1A) SW1D Bottom Switch On-Resistance	V_{IN2} = 3.6V V_{IN2} = 3.6V			0.19 0.17		Ω Ω
$R_{DS(ON)2}$	SW2A/B Top Switch On-Resistance (2A) SW2A/B Bottom Switch On-Resistance	V_{IN1} = 3.6V V_{IN1} = 3.6V			0.096 0.085		Ω Ω
$I_{SW1(LKG)}$	Switch Leakage Current SW1	V_{IN} = 6V V_{ITH1} = 0V V_{RUN1} = 0V			0.01	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{CCA} = 3.6V, unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{SW1D(LKG)}$	Switch Leakage Current SW1D	V_{IN} = 6V V_{ITH1} = V_{ITH2} = 0V V_{RUN1} = V_{RUN2} = 0V			0.01	1	µA
$I_{SW2A/B(LKG)}$	Switch Leakage Current SW2A/B	V_{IN} = 6V V_{ITH2} = 0V V_{RUN2} = 0V			0.01	1	µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{IN1}, V_{IN2}, V_{CCA}, V_{CCD} Rising V_{IN1}, V_{IN2}, V_{CCA}, V_{CCD} Falling		2.03 1.86	2.14 1.97	2.28 2.11	V V
T_{PGOOD1}	Threshold for Power Good Percentage Deviation from Regulated V_{FB1} (Typically 0.6V).	V_{FB1} Ramping Up, $V_{SYNC/MODE}$ = 0V			–8		%
T_{PGOOD2}	Threshold for Power Good Percentage Deviation from Regulated V_{FB2} (Typically 0.6V).	V_{FB2} Ramping Up, $V_{SYNC/MODE}$ = 0V			–8		%
R_{PGOOD1}	Power Good Pull-Down On-Resistance				132	300	Ω
R_{PGOOD2}	Power Good Pull-Down On-Resistance				132	300	Ω
t_{SS}	Soft-Start Internal Time.	V_{FB} from 0% to 95%, $V_{TRACK/SS}$ Is Floating		0.8	1.2	1.9	ms
V_{RUN1}, V_{RUN2}, V_{PHASE}	RUN1, RUN2, and PHASE Threshold			0.3	0.8	1.2	V
I_{RUN1}, I_{RUN2}, I_{PHASE}	RUN1, RUN2, and PHASE Leakage Current	V_{IN} = 6V, V_{PHASE} = 3V, V_{RUN1} = V_{RUN2} = 3V			±0.01	±1	µA
$VTL_{SYNC/MODE}$	SYNC/MODE Threshold Voltage Low to Put the Part into Pulse-Skipping Mode					0.5	V
$VTH_{SYNC/MODE}$	SYNC/MODE Threshold Voltage High to Put the Part into Burst Mode Operation			V_{IN} – 0.5			V
$V_{SYNC/MODE}$	SYNC/MODE Threshold for Clock Synchronization			0.3	0.8	1.2	V
$I_{SYNC/MODE}$	SYNC/MODE Leakage Current	V_{IN} = 6V, $V_{SYNC/MODE}$ = 3V			±0.01	±1	µA
VTH_{FREQ}	FREQ Threshold Voltage High			V_{IN} – 0.85			V
I_{BMC1}, I_{BMC2}	BMC1, BMC2 Leakage Current	V_{IN} = 6V, V_{BMC} = 3V				±0.4	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3546 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3546E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3546I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The LTC3546 is tested in feedback loop which servos V_{FB1} to the midpoint for the error amplifier (V_{ITH1} = 0.6V) and V_{FB2} to the midpoint for the error amplifier (V_{ITH2} = 0.6V).

Note 4: Total supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5: Variable frequency operation with resistor is guaranteed by design and is subject to duty cycle limitations.

Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

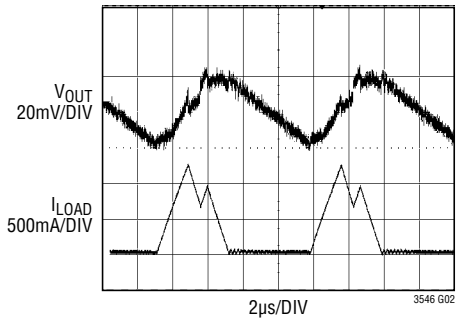
Note 7: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

$T_J = T_A + (P_D \bullet 34°C/W)$

Note 8: Minimum current limit is guaranteed by design and correlation to the $R_{DS(ON)1D}$, I_{LIM1} and I_{LIM2} measurements.

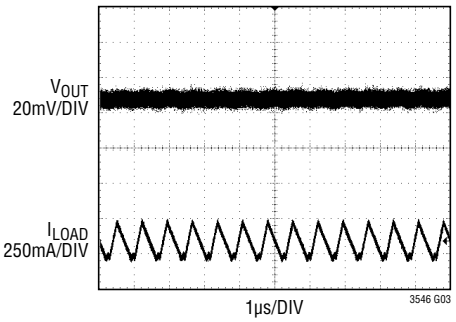
TYPICAL PERFORMANCE CHARACTERISTICS

OUT1 Burst Mode Operation



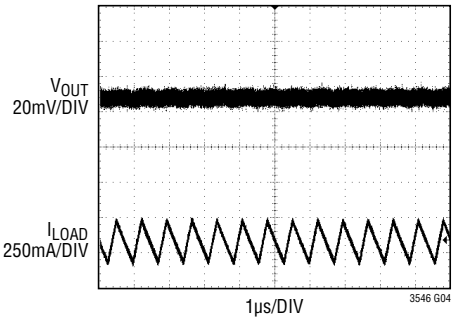
SW1D CONNECTED TO SW1
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 300mA

OUT1 Pulse-Skipping Mode Operation



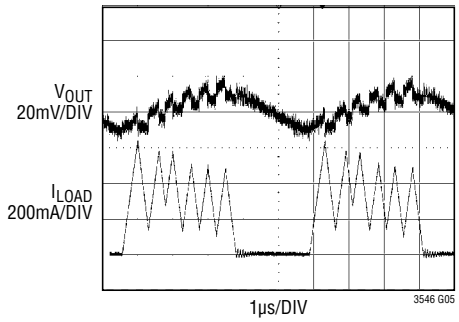
SW1D CONNECTED TO SW1
V_{IN} = 3.6V
V_{OUT} = 1.2V
I_{LOAD} = 100mA

OUT1 Forced Continuous Mode Operation



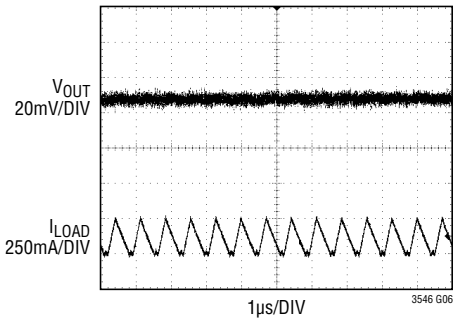
SW1D CONNECTED TO SW1
V_{IN} = 3.6V
V_{OUT} = 1.2V
I_{LOAD} = 100mA

OUT1 Burst Mode Operation



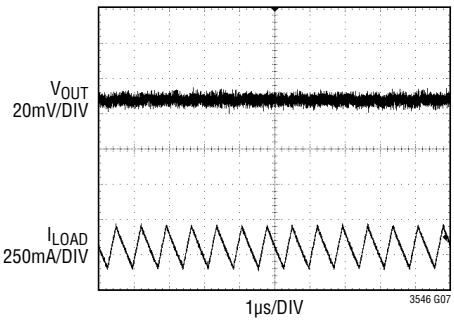
SW1D CONNECTED TO SW2
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 200mA

OUT1 Pulse-Skipping Mode Operation



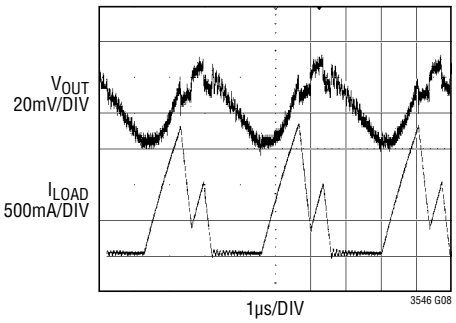
SW1D CONNECTED TO SW2
V_{IN} = 3.6V
V_{OUT} = 1.2V
I_{LOAD} = 100mA

OUT1 Forced Continuous Mode Operation



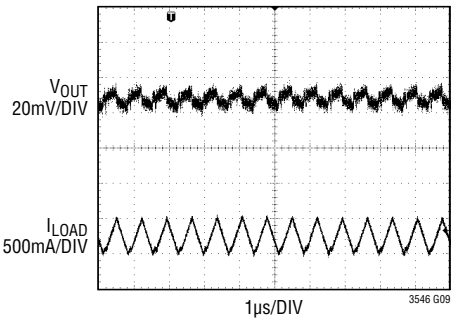
SW1D CONNECTED TO SW2
V_{IN} = 3.6V
V_{OUT} = 1.2V
I_{LOAD} = 50mA

OUT2 Burst Mode Operation



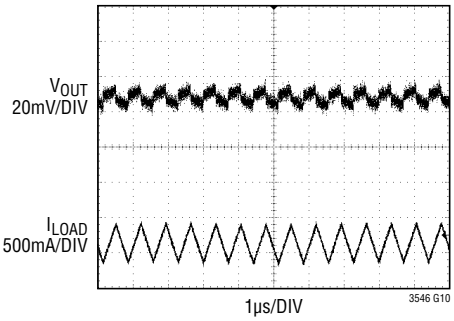
SW1D CONNECTED TO SW2
V_{IN} = 3.6V
V_{OUT} = 2.5V
I_{LOAD} = 500mA

OUT2 Pulse-Skipping Mode Operation



SW1D CONNECTED TO SW2
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 200mA

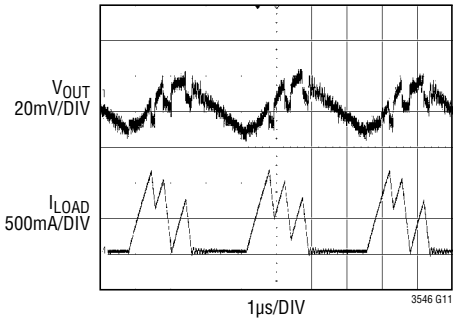
OUT2 Forced Continuous Mode Operation



SW1D CONNECTED TO SW2
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 100mA

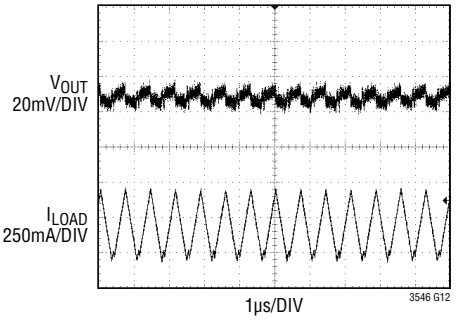
TYPICAL PERFORMANCE CHARACTERISTICS

OUT2 Burst Mode Operation



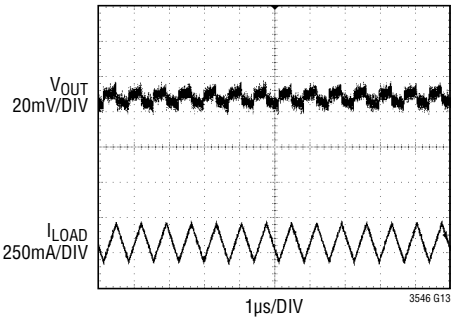
SW1D CONNECTED TO SW1
V_{IN} = 3.6V
V_{OUT} = 2.5V
I_{LOAD} = 300mA

OUT2 Pulse-Skipping Mode Operation



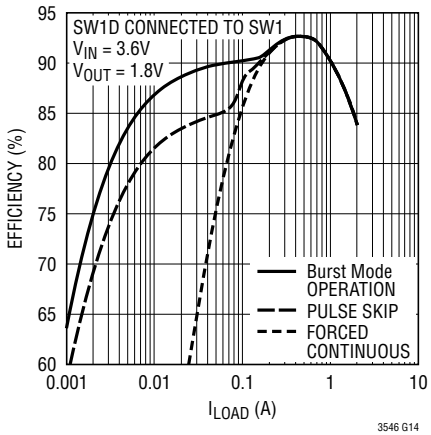
SW1D CONNECTED TO SW1
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 200mA

OUT2 Forced Continuous Mode Operation

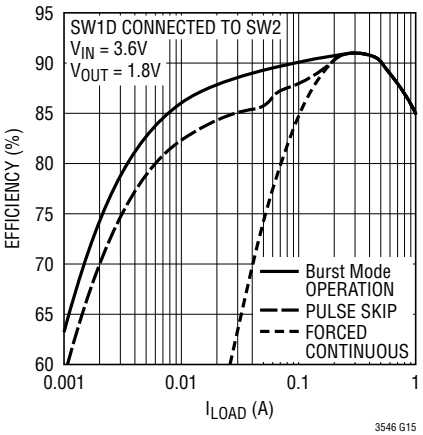


SW1D CONNECTED TO SW1
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 100mA

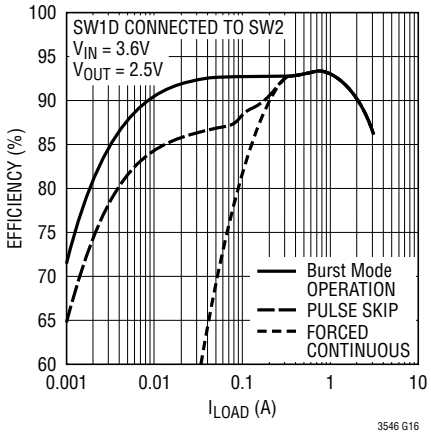
OUT1 Efficiency vs Load Current



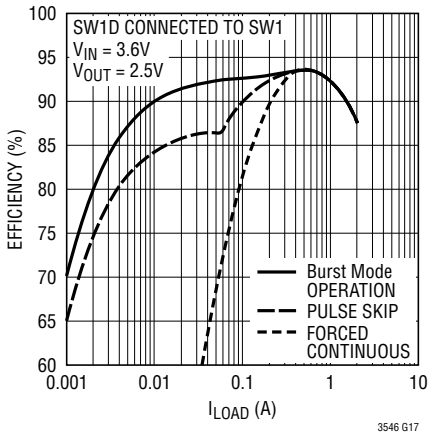
OUT1 Efficiency vs Load Current



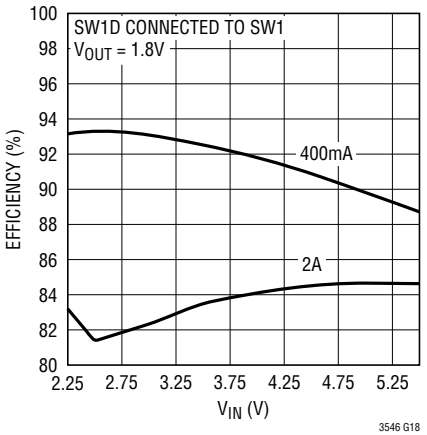
OUT2 Efficiency vs Load Current



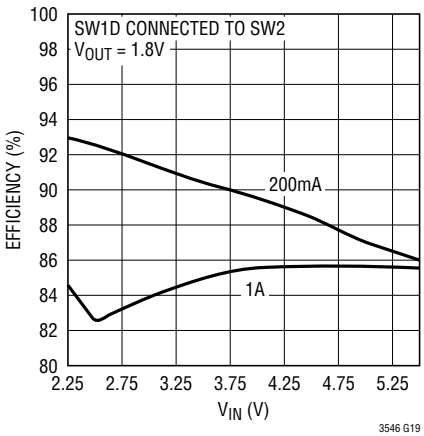
OUT2 Efficiency vs Load Current



OUT1 Efficiency vs V_{IN}

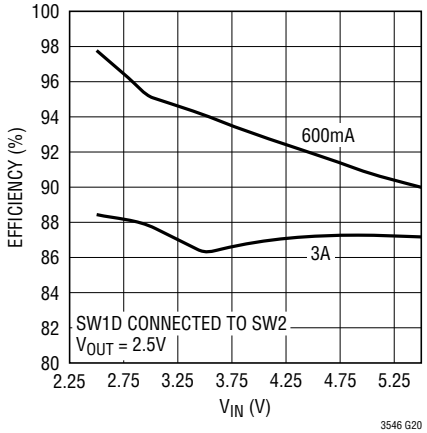


OUT1 Efficiency vs V_{IN}

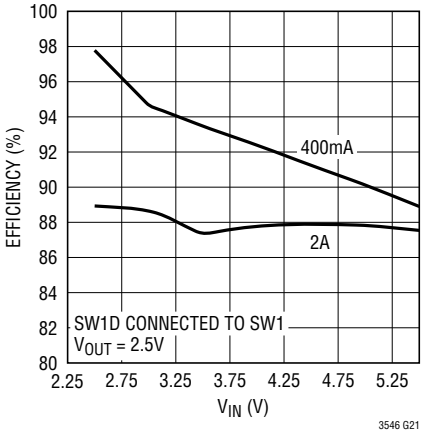


TYPICAL PERFORMANCE CHARACTERISTICS

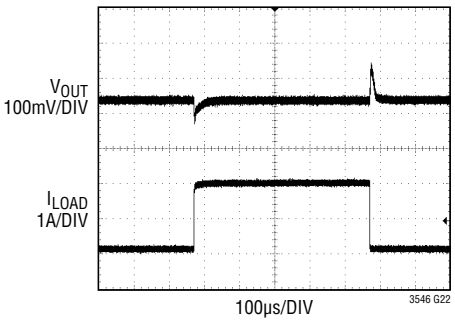
OUT2 Efficiency vs V_{IN}



OUT2 Efficiency vs V_{IN}

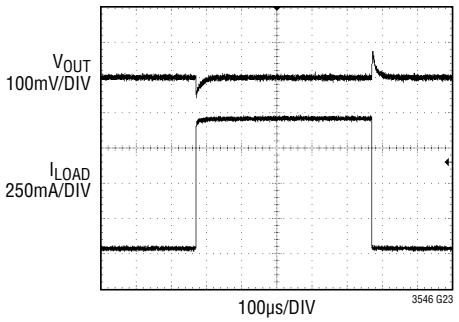


OUT1 Load Step



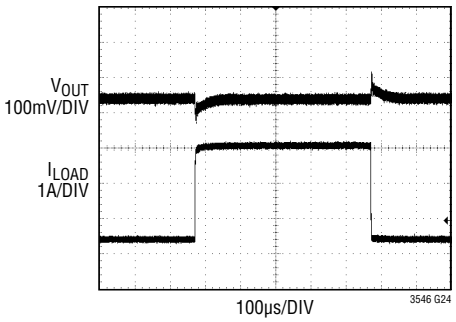
SW1D CONNECTED TO SW1
V_{IN} = 3.6V
V_{OUT} = 1.2V
I_{LOAD} = 200mA TO 1.9A

OUT1 Load Step



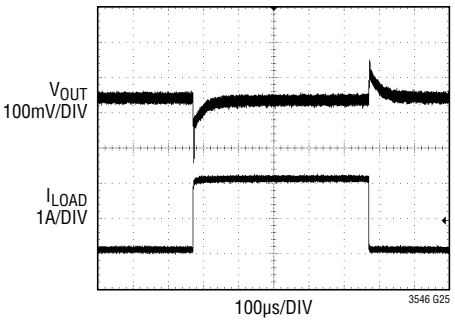
SW1D CONNECTED TO SW2
V_{IN} = 3.6V
V_{OUT} = 1.2V
I_{LOAD} = 100mA TO 0.9A

OUT2 Load Step



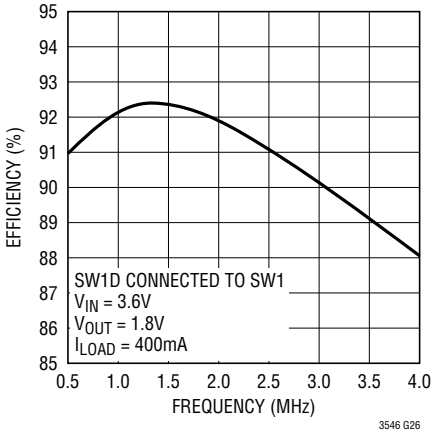
SW1D CONNECTED TO SW2
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 300mA TO 2.9A

OUT2 Load Step

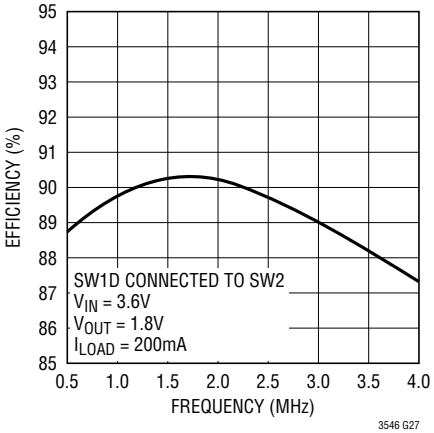


SW1D CONNECTED TO SW1
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 200mA TO 1.9A

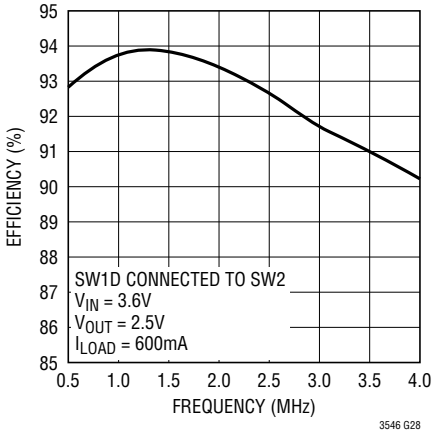
OUT1 Efficiency vs Frequency



OUT1 Efficiency vs Frequency

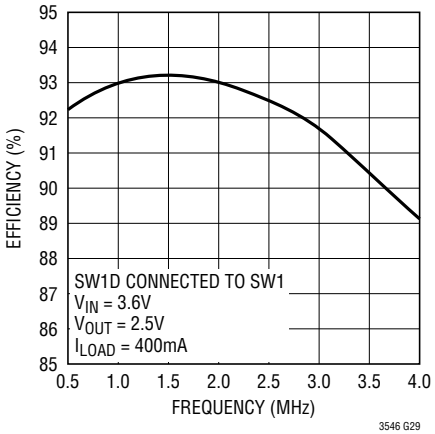


OUT2 Efficiency vs Frequency

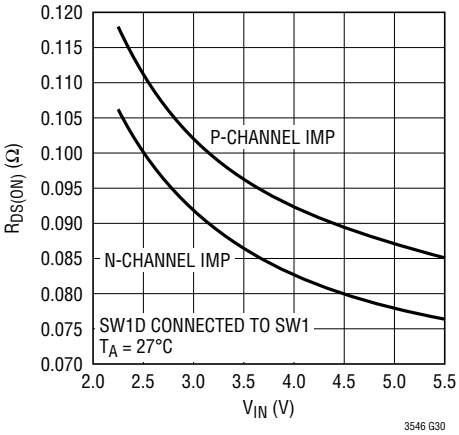


TYPICAL PERFORMANCE CHARACTERISTICS

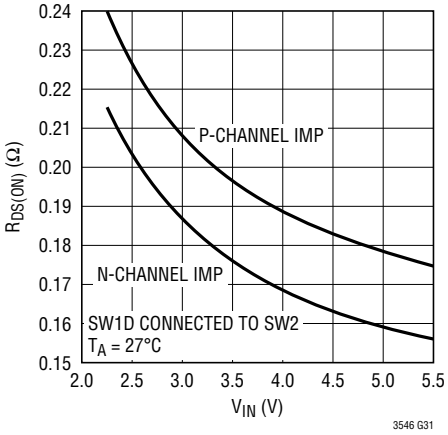
OUT2 Efficiency vs Frequency



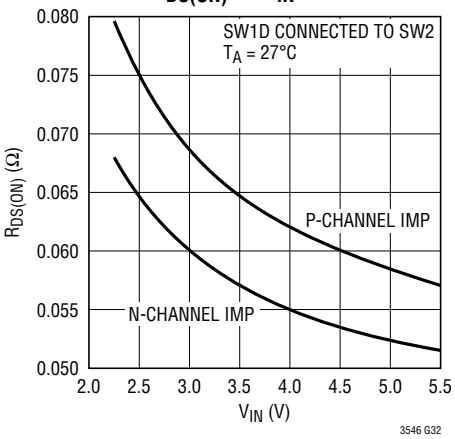
OUT1 $R_{DS(ON)}$ vs V_{IN}



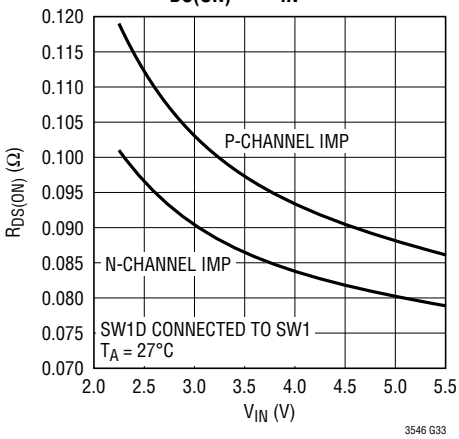
OUT1 $R_{DS(ON)}$ vs V_{IN}



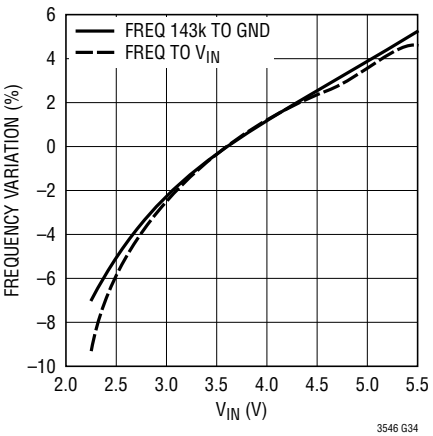
OUT2 $R_{DS(ON)}$ vs V_{IN}



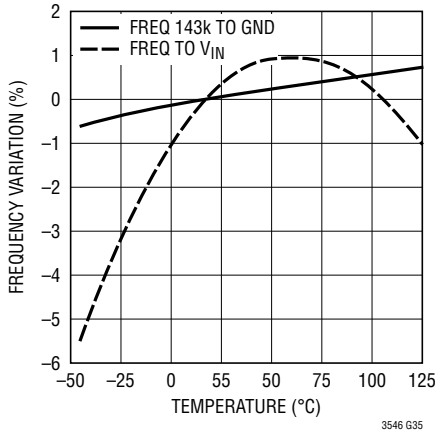
OUT2 $R_{DS(ON)}$ vs V_{IN}



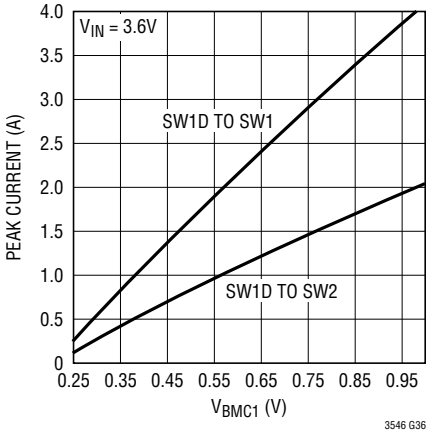
Frequency Variation vs V_{IN}



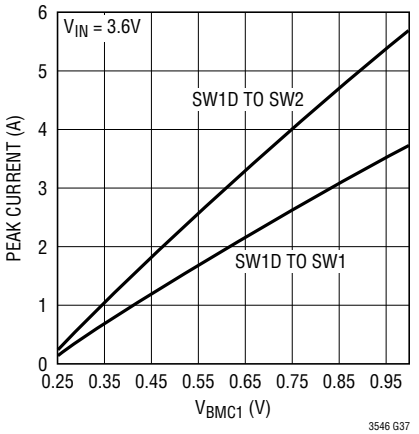
Frequency Variation vs Temperature



OUT1 Minimum Peak Current vs V_{BMC1}



OUT2 Minimum Peak Current vs V_{BMC2}



PIN FUNCTIONS (UFD/FE)

BMC2 (Pin 1/Pin 4): Burst Mode Clamp for Channel 2. Connecting this pin to an external voltage between 0V and 0.6V sets the Burst Mode clamp level. If this pin is pulled to V_{CCA}, an internal Burst Mode clamp level is used. This pin should be tied to GND when Burst Mode operation is not selected.

TRACK/SS2 (Pin 2/Pin 5): Tracking input for Channel 2 output or optional external soft-start input. V_{OUT2} will track an external voltage at this pin. Leaving this pin floating allows V_{OUT2} to start-up using the internal soft-start. An external soft-start can be programmed by connecting a capacitor between this pin and ground. External soft-start ramp time must be greater than the internal soft-start time of 1.2ms. Refer to the Applications Information section for more details.

V_{FB2} (Pin 3/Pin 6): Feedback voltage from external resistive divider from the Channel 2 regulator output. Nominal voltage for this pin is 0.6V.

I_{TH2} (Pin 4/Pin 7): Error Amplifier Compensation for Channel 2 Regulator. Peak current increases with an increase in the voltage on this pin. Nominal voltage range for this pin is 0V to 1.5V.

V_{CCD} (Pin 5/Pin 8): Supply Pin for Internal Digital Circuitry.

RUN2 (Pin 6/Pin 9): Low Level Logic Input. Enable for Channel 2. When pulled high, regulator is running. When at 0V, regulator is off. When both RUN1 and RUN2 are at 0V the part is in shutdown.

V_{IN2} (Pin 7/Pin 10): Supply pin for 2A P-channel switch which connects from V_{IN2} to SW2A/B.

V_{IN1} (Pin 8/Pin 11): Supply pin for 1A P-channel switch which connects from V_{IN1} to SW1.

V_{IN1D} (Pin 9/Pin 12): Supply pin for 1A dependent P-channel switch which connects from V_{IN1D} to SW1D.

SW2A (Pin 10/Pin 13): Half of the switch node connection to the inductor for Channel 2. SW2A and SW2B must be externally tied together. This pin swings from V_{IN2} to PGND2.

SW2B (Pin 11/Pin 14): Half of the switch node connection to the inductor for Channel 2 SW2A and SW2B must be externally tied together. This pin swings from V_{IN2} to PGND2.

SW1D (Pin 12/Pin 15): The Dependent Switch Node Connection. The pin is externally connected to SW1 for a 2A/2A regulator or to SW2A/B for a 3A/1A regulator. Internal circuitry detects which pin SW1D is externally connected to, SW1 or SW2A/B. This pin swings from V_{IN1D} to PGND1D. SW1D switching will be controlled by the output switch to which it is connected, i.e., SW1 or SW2A/SW2B. The dependant 1A power stage can be disabled by floating the SW1D pin. The SW1D pin must never be connected to V_{IN} or GND. When disabled, SW1D is pulled high internally.

SW1 (Pin 13/Pin 16): The switch node connection to the Inductor for the Channel 1 regulator. This pin swings from V_{IN1} to PGND1.

PGND1D (Pin 14/Pin 17): Ground for SW1D Switching N-Channel Driver.

PGND1 (Pin 15/Pin 18): Ground for SW1 Switching N-Channel Driver.

PGND2 (Pin 16/Pin 19): Ground for SW2A and SW2B Switching N-Channel Driver.

RUN1 (Pin 17/Pin 20): Low Level Logic Input. Enable for Channel 1. When pulled high, regulator is running. When at 0V, regulator is off. When both RUN1 and RUN2 are at 0V the part is in shutdown.

PHASE (Pin 18/Pin 21): Low Level Logic Input. Selects Channel 2 regulator switching phase with respect to Channel 1 regulator switching. When pulled high, the SW1 regulator and the SW2A/B regulator are in phase. When PHASE is at 0V the SW1 regulator and the SW2A/B regulator are switching 180° out-of-phase.

I_{TH1} (Pin 19/Pin 22): Error Amplifier Compensation for Channel 1. Peak current increases with an increase in the voltage on this pin. Nominal voltage range for this pin is 0V to 1.5V.

PIN FUNCTIONS (UFD/FE)

V_{FB1} (Pin 20/Pin 23): Feedback voltage from external resistive divider from Channel 1 output. Nominal voltage for this pin is 0.6V.

TRACK/SS1 (Pin 21/Pin 24): Tracking input for Channel 1 output or optional external soft-start input. V_{OUT1} will track an external voltage at this pin. Leaving this pin floating allows V_{OUT1} to start-up using the internal soft-start. An external soft-start can be programmed by connecting a capacitor between this pin and ground. External soft-start ramp time must be greater than the internal soft-start time of 1.2ms. Refer to the Applications Information section for more details.

BMC1 (Pin 22/Pin 25): Burst Mode Clamp for Channel 1. Connecting this pin to an external voltage between 0V and 0.6V sets the Burst Mode clamp level. If this pin is pulled to V_{CCA}, an internal Burst Mode clamp level is used. This pin should be tied to GND when Burst Mode operation is not selected.

PGOOD1 (Pin 23/Pin 26): Power Good Pin for the 1A Regulator. This common drain logic output is pulled to GND when the output voltage of Channel 1 is below –8% of regulation.

FREQ (Pin 24/Pin 27): Frequency Set Pin. When FREQ is at V_{CCA}, the internal oscillator runs at 2.25MHz. When a resistor is connected from this pin to GNDA, the internal oscillator frequency can be varied from 0.75MHz to 4MHz. When using external synchronization this pin compensates the internal PLL. Typical compensation components are a 200k resistor in series with a 100pF capacitor.

GNDA (Pin 25/Pin 28): Ground Pin for Internal Analog Circuitry.

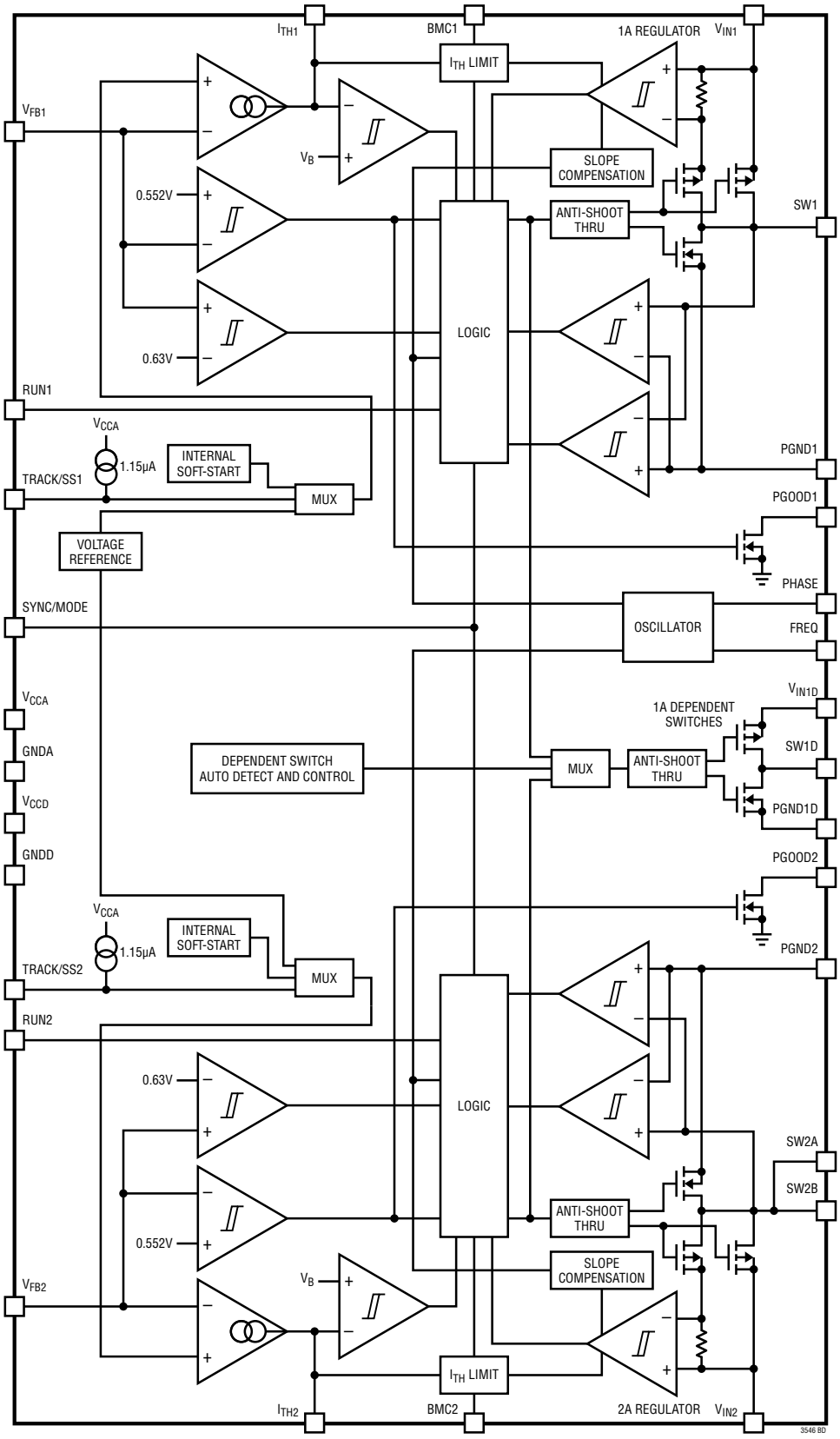
V_{CCA} (Pin 26/Pin 1): Supply Pin for Internal Analog Circuitry.

SYNC/MODE (Pin 27/Pin 2): Combination Mode Selection and Oscillator Synchronization Pin. This pin controls the operation of the device. When the voltage on the SYNC/MODE pin is > (V_{IN} – 0.5V), Burst Mode operation is selected for both regulators. When the voltage on the SYNC/MODE pin is <0.5V, pulse-skipping mode is selected for both regulators. When the SYNC/MODE pin is held at V_{IN}/2, forced continuous mode is selected for both regulators. The oscillation frequency can be synchronized to an external oscillator applied to this pin. When synchronized to an external clock, pulse-skipping mode is selected.

PGOOD2 (Pin 28/Pin 3): Power Good Pin for Channel 2 This common drain logic output is pulled to GND when the output voltage of Channel 2 is below –8% of regulation.

GNDD (Exposed Pad Pin 29/Exposed Pad Pin 29): Digital Ground. Connect to Electrical Ground for substrate and internal digital circuitry. Solder to PCB for rated thermal performance.

FUNCTIONAL DIAGRAM



OPERATION

The LTC3546 uses a constant-frequency, current mode architecture. Both channels share the same clock frequency. The PHASE pin sets whether the channels are running in-phase, or 180° out-of-phase. The operating frequency is determined by connecting the FREQ pin to V_{IN} for 2.25MHz operation or by connecting a resistor from FREQ to GNDA for frequencies between 0.75MHz to 4MHz. A 143k resistor to GNDA will set the frequency to 1.5MHz. The part can also be synchronized to an external clock through the SYNC/MODE pin. To suit a variety of applications, the selectable SYNC/MODE pin allows the user to trade-off noise for efficiency.

The output voltages are set by external dividers returned to the V_{FB1} and V_{FB2} pins. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and adjusts an internal peak inductor current setting accordingly. Peak inductor current during Burst Mode operation can also be set externally through the BMC1 and BMC2 pins. Undervoltage comparators will pull the PGOOD1 or PGOOD2 outputs low when their respective outputs drop below –8% of the set output voltage.

The TRACK/SS pins allow for controlled start-up via an externally or internally generated voltage ramp. It can also track an externally applied voltage.

A 1A dependent switch, SW1D, can be externally connected to the SW1 output or the SW2A/SW2B output. Internal circuitry auto detects which output SW1D is connected to and controls them accordingly. With this flexibility, the LTC3546 can be configured as either a 2A/2A dual regulator (when SW1D is connected to SW1) or as a 3A/1A dual regulator (when SW1D is connected to SW2A/SW2B).

Main Control Loop

For each regulator, during normal operation, the P-channel MOSFET power switch is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the 0.6V reference voltage. The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom N-channel MOSFET switch into the load until the next clock cycle.

The peak inductor current is controlled by the voltage on the I_{TH} pin, which is the output of the 2.5MHz bandwidth error amplifier. The error amplifier compares the V_{FB} pin to the 0.6V reference. When the load current increases, the V_{FB} voltage decreases slightly below the reference. This decrease causes the error amplifier to increase the I_{TH} voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground. When the RUN pin is pulled high, the control loop goes through start-up. Start-up is dependent on the TRACK/SS pin. If TRACK/SS is left floating, an internal soft-start is enabled which will ramp up the output voltage to the desired level in 1.2ms. The output voltage will track the voltage on its associated TRACK/SS pin. If the TRACK/SS pin is connected through a resistor divider from another supply, such as the output voltage from the other LTC3546 regulator, the output voltage will track this supply thus allowing the LTC3546 output voltage to track the other supply start-up. If a capacitor is connected from the TRACK/SS pin to ground, when RUN goes high, an internal 1.15µA current source will charge the external capacitor controlling the output voltage start-up. Care must be taken to make sure the external start-up ramp time is greater than the 1.2ms internal start-up time.

Low Current Operation

Three modes are available to control the operation of the LTC3546 at low currents. All three modes automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, Burst Mode operation can be selected. When the load is relatively light, the LTC3546 automatically switches into Burst Mode operation in which the switches operate intermittently based on load demand. By running cycles periodically, the switching losses which are dominated by the gate charge losses of the power MOSFETs are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value.

A voltage comparator with hysteresis trips when I_{TH} is below 0.24V, shutting off the switches and reducing the power.

OPERATION

The output capacitor and the inductor supply the power to the load until I_{TH} exceeds 0.31V, turning on the switch and the main control loop which starts another cycle.

The Burst Mode peak inductor current can be set externally via the BMC pin. When this pin is set somewhere between 0V to 0.6V, the voltage on this pin controls the Burst Mode clamp level. When the BMC pin is pulled to V_{IN}, an internal Burst Mode clamp level is used.

For lower output voltage ripple at low currents, pulse-skipping mode can be used. In this mode, the LTC3546 continues to switch at constant frequency down to very low currents, where it will eventually begin skipping pulses.

Finally, in forced continuous mode, the inductor current is constantly cycled which creates a fixed output voltage ripple at all output current levels. This feature is desirable in telecommunications since the noise is a constant frequency and is thus easy to filter out. Another advantage of this mode is that the regulator is capable of both sourcing current into a load and sinking some current from the output. In forced continuous operation, an overvoltage comparator monitors the V_{FB} pin and decreases the current limit whenever an overvoltage condition is detected (V_{FB} > 0.63V).

The SYNC/MODE pin selects what mode the LTC3546 is in. The SYNC/MODE pin sets the mode for both regulators.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100% which is the dropout condition. In the dropout condition, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFETs and inductors.

Low Supply Operation

The LTC3546 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below about 2.14V to prevent unstable operation.

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A general LTC3546 application circuit is shown in Figure 7. External component selection is driven by the load requirement, and begins with the selection of the inductors L1, and L2. Once L1 and L2 are chosen, C_{IN}, C_{OUT1}, and C_{OUT2} can be selected.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency, f_O, of the LTC3546 is determined by pulling the FREQ pin to V_{IN}, for 2.25MHz operation, by connecting an external resistor from FREQ to ground, or by driving an external clock signal into SYNC/MODE.

When using an external resistor to set the oscillator frequency use the following equation:

$$R_T = \frac{2.51 \bullet 10^{11}}{f_O}(\Omega) - 20k\Omega$$

for 0.75MHz ≤ f_O ≤ 4MHz. Or use Figure 1 to select the value for R_T.

The maximum operating frequency is also constrained by the minimum on-time (typically 70ns) and duty cycle, especially when forced continuous mode is selected. Assuming a worst-case minimum on-time of 150ns, this can be calculated as:

$$f_{O(MAX)} \approx 6.67\left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)(MHz)$$

The minimum frequency is limited by leakage and noise coupling due to the large resistance of R_T.

Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

$$\Delta I_L = \frac{V_{OUT}}{f_O \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability.

A reasonable starting point for setting ripple current is $\Delta I_L = 0.35 I_{LOAD(MAX)}$, where $I_{LOAD(MAX)}$ is the maximum output current. The largest ripple ΔI_L occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L \geq \frac{V_{OUT}}{f_O \bullet \Delta I_L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

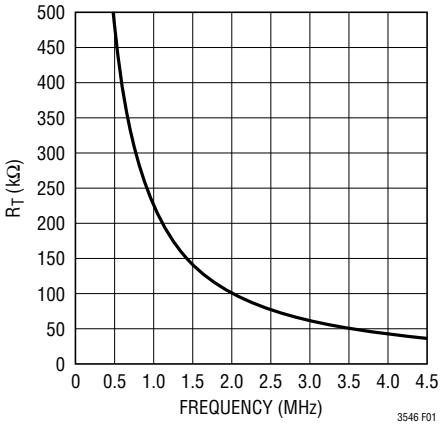

Figure 1. Frequency vs R_T

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Burst Mode Operation Considerations

There are two factors that determine the load current at which the LTC3546 enters Burst Mode operation: the inductor value and the BMC pin voltage. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes Burst Mode operation to occur at lower load currents. Lower inductor values will also cause a dip in efficiency in the upper range of low current operation. Lower inductor values will also cause the burst frequency to increase in Burst Mode operation.

The burst clamp level can be set by the voltage on the BMC pin. If BMC is tied to V_{IN}, an internally set level is used. A BMC pin voltage between 0V and 0.6V will set the burst clamp level (see charts OUT1 Minimum Peak Current vs V_{BMC1} and OUT2 Minimum Peak Current vs V_{BMC2} in the Typical Performance Characteristics section). Generally, a higher clamp level results in improved light load efficiency and higher output voltage ripple, while a lower clamp level results in small output voltage ripple at the expense of efficiency. The BMC pin should be connected to ground when Burst Mode operation is not selected.

Inductor Core Selection

Different core materials and shapes will change the size/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements of any radiated field/EMI requirements than on what the LTC3546 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3546 applications.

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter can be approximated by the sum of two square waves with duty cycles of approximately V_{OUT1}/V_{IN} and V_{OUT2}/V_{IN}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. Some capacitors have a derating spec for maximum RMS current. If the capacitor being used has this requirement it is necessary to calculate

Table 1.

MANUFACTURER	PART NUMBER	VALUE (µH)	MAX DC CURRENT (A)	DCR	DIMENSIONS L × W × H (mm)
Würth Elektronik	WE-PD2 MS 7447745012	1.2	4.6	0.017	5.2 × 5.8 × 2
Würth Elektronik	WE-PD2 MS 74477450056	0.56	6.5	0.0078	5.2 × 5.8 × 2
Vishay	IHLP-1616AB-11	1.2	3.75	0.068	4.06 × 4.45 × 1.20
Vishay	IHLP-1616AB-11	0.47	6	0.019	4.06 × 4.45 × 1.20
Coilcraft	LPS6225-122	1.2	5.4	0.04	6.2 × 6.2 × 2.5
Coilcraft	DO1813H-561	0.56	7.7	0.01	6.10 × 8.89 × 5.00
Coiltronics	SD20-1R2	1.2	2.55	0.0275	5.2 × 5.2 × 2
Coiltronics	SD20-R47	0.47	4	0.02	5.2 × 5.2 × 2
Sumida	CDRH3D23NP-1R5NC	1	2.8	0.025	3.8 × 3.8 × 2.3

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the maximum RMS current. The RMS current calculation is different if the part is used in-phase or out-of-phase.

For in-phase, there are two different equations:

$V_{OUT1} > V_{OUT2}$:

$$I_{RMS} = \sqrt{2 \bullet I1 \bullet I2 \bullet D2(1-D1) + I2^2\left(D2-D2^2\right) + I1^2\left(D1-D1^2\right)}$$

$V_{OUT2} > V_{OUT1}$:

$$I_{RMS} = \sqrt{2 \bullet I1 \bullet I2 \bullet D1(1-D2) + I2^2\left(D2-D2^2\right) + I1^2\left(D1-D1^2\right)}$$

Where:

$$D1 = \frac{V_{OUT1}}{V_{IN}} \text{ and } D2 = \frac{V_{OUT2}}{V_{IN}}$$

When D1 = D2, then the equation simplifies to:

$$I_{RMS} = (I1+I2)\sqrt{D(1-D)}$$

or

$$I_{RMS} = (I1+I2)\frac{\sqrt{V_{OUT}\left(V_{IN}-V_{OUT}\right)}}{V_{IN}}$$

where the maximum average output currents I1 and I2 equals the peak current minus half the peak-to-peak ripple current:

$$I1 = I_{LIM1} - \frac{\Delta I_{L1}}{2}$$

$$I2 = I_{LIM2} - \frac{\Delta I_{L2}}{2}$$

These formula have a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = (I1 + I2)/2$. This simple worst-case is commonly used to determine the worst-case I_{RMS}.

For out-of-phase (PHASE pin is at ground), the ripple current can be lower than the in-phase.

In the out-of-phase case, the maximum I_{RMS} does not occur when $V_{OUT1} = V_{OUT2}$. The maximum typically occurs when $V_{OUT1} - V_{IN}/2 = V_{OUT2}$ and when $V_{OUT2} - V_{IN}/2 = V_{OUT1}$. As a good rule of thumb, the amount of worst-case ripple is about 75% of the worst-case ripple in the in-phase mode. Note, that when $V_{OUT1} = V_{OUT2} = V_{IN}/2$ and $I_1 = I_2$, the ripple is at its minimum.

Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{IN} for high frequency decoupling, when not using an all ceramic capacitor solution.

Output Capacitor (C_{OUT1} and C_{OUT2}) Selection

The selection of C_{OUT1} and C_{OUT2} is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8 \bullet f_O \bullet C_{OUT}}\right)$$

where f_O = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantalum capacitors are all available in surface mount packages. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR(size) product of any aluminum electrolytic at a somewhat higher price. Special polymer capacitors, such as Sanyo POSCAP, offer very low ESR, but have a lower capacitance density than other types. Tantalum capacitors have the highest capacitance

APPLICATIONS INFORMATION

density, but it has a larger ESR and it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors have a significantly larger ESR, and are often used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have the lowest ESR and cost but also have the lowest capacitance density, high voltage and temperature coefficient and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing. Other capacitor types include the Panasonic specialty polymer (SP) capacitors.

Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Because the LTC3546 control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size. When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Great care must be taken when using only ceramic input and output capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to disrupt circuit operation or damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 2 to 3 times the linear droop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx 2.5 \frac{\Delta I_{OUT}}{f_0 V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions.

Setting the Output Voltage

The LTC3546 generates a 0.6V reference voltage between the feedback pin, V_{FB1} and V_{FB2}, and the signal ground. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT1} \approx 0.6V\left(1+\frac{R1}{R2}\right)$$

$$V_{OUT2} \approx 0.6V\left(1+\frac{R3}{R4}\right)$$

Resistor locations are shown in Figure 2.

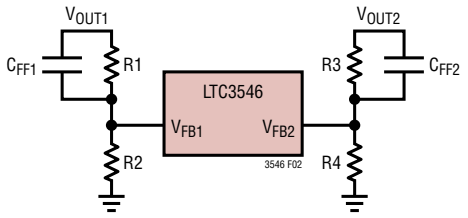

Figure 2. Setting Output Voltages

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Keeping the current small (<20µA) in these resistors maximizes efficiency, but making the current too small may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

To improve the frequency response, a feedforward capacitor C_{FF} may also be used. Typical values used here are 10pf to 100pf. Great care should be taken to route the V_{FB} node away from noise sources, such as the inductor or an SW line.

Shutdown, Soft-Start and Tracking Start-Up

The LTC3546 start-up works by comparing two inputs, an internal 1.2ms linear soft-start ramp and the TRACK/SS pin. Whichever input is lower in voltage is the controlling voltage used for start-up. The internal start-up ramps to 0.6V in 1.2ms. If a slower start-up is desired, the TRACK/SS pin has a 1.15µA pull up current so a start-up ramp rate can be programmed with an external capacitor, or a voltage divider from another signal can be applied to the TRACK/SS pin.

During start-up the controlling voltage must rise above 120mV before the output will start switching.

When the RUN pin is low, both the internal 1.2ms soft-start ramp and the TRACK/SS pin are pulled to ground. When the RUN pin is pulled high, both the internal soft-start ramp and the TRACK/SS pin are released. From the time when the RUN pin is asserted until the controlling voltage reaches 0.6V, the regulator is in the start-up state. In this state, the error amplifier will compare the feedback signal at V_{FB} to the controlling voltage (the lower of either the TRACK/SS voltage or the internal ramp voltage) and the regulator will force them to be equal. In this state, the mode of the regulator is forced to pulse skipping. The regulator will continue in this manner until the voltage on the controlling voltage rises above 0.6V. Once the controlling ramp signal is above 0.6V the error amplifier uses the internal 0.6V reference and the operational mode will switch to the mode set by the SYNC/MODE pin.

If the TRACK/SS pin is ramped down after start-up, the error amplifier will compare the feedback signal at V_{FB} to the voltage on the TRACK/SS pin once the TRACK/SS voltage drops 6% below the internal reference voltage of 0.6V (0.564V). The regulator will try to force the V_{FB} voltage to equal the TRACK/SS voltage if there is sufficient load current to pull the output low at this rate, otherwise the output will ramp down at the discharge rate of the output capacitor. Once the TRACK/SS voltage drops below about 100mV all switching functions cease and the regulator is forced back into pulse-skipping mode. The operational mode while TRACK/SS is ramping down is set by the MODE/SYNC pin.

To use the internal 1.2ms linear soft-start controlling voltage leave the TRACK/SS pin floating. By floating the TRACK/SS pin the internal 1.15µA pull up current will pull the TRACK/SS pin up faster than the internal 1.2ms ramp. Care must be taken to insure the TRACK/SS ramp up time (from 0V to 0.6V) is much shorter than the internal 1.2ms ramp time. Parasitic capacitance on this pin should be much smaller than:

$$C_{PARASITICTRACK/SS} \ll \frac{1.15\mu A \bullet 1.2ms}{0.6V}$$

or

$$C_{PARASITICTRACK/SS} \ll 2.3nF$$

An externally controlled soft-start ramp is obtained when an external capacitor is connected from the TRACK/SS pin to ground and its ramp rate is slower than the internal soft-start ramp. In this configuration, soft-start times longer than 1.2ms can be achieved. When RUN is pulled high, the internal 1.15µA current source charges the external capacitor linearly from 0V. While the TRACK/SS pin is below 0.6V the error amplifier forces the regulator to drive the V_{FB} pin to the voltage on the TRACK/SS pin. Once the V_{FB} pin reaches 0.6V the regulator switches to the internal 0.6V reference. The ramp-up time for the output is calculated as:

$$t_{RAMP} = \frac{C_{TRACK/SS} \bullet 0.6V}{1.15\mu A}$$

For this equation to be valid, the ramp time must be greater than 1.2ms thus:

$$C_{TRACK/SS} \geq \frac{1.15\mu A \bullet 1.2ms}{0.6V}$$

or

$$C_{TRACK/SS} \geq 2.3nF$$

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The LTC3546 can also track an external voltage during startup by using an external voltage divider to the TRACK/SS pin, and also insuring that the ramp rate on the TRACK/SS pin is slower than the internal 1.2ms ramp rate.

As indicated in Figure 3, a resistor divider from an external voltage can be connected to the TRACK/SS pin to allow the start-up of V_{OUT} to ratiometrically track an external voltage V_X.

For $V_{TRACKSS} < 0.6V$

$$V_{OUT} = V_X \bullet \frac{R2X}{R1X+R2X} \bullet \frac{R1+R2}{R2}$$

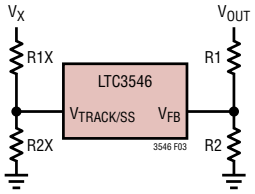

Figure 3. Tracking External Voltages

Coincident tracking is where $V_{OUT} = V_X$ during startup. To implement coincident tracking R1X in Figure 3 is set to the same value as R1 and R2X to the value of R2. Coincident tracking is illustrated in Figure 4. The voltage at TRACK/SS when V_X is at its final value should be ≥0.8V (sufficient margin above the 0.6V reference voltage).

Ratiometric tracking is where $V_{OUT} \neq V_X$ during startup but rather, it is set to some fractional value of V_X. To implement ratiometric tracking (as illustrated in Figure 5), set R1X in Figure 3 to the same value as R1 and R2X to the value of R2 + ΔR. The ΔR added to R2 should be sufficient so that the TRACK/SS voltage is ≥ 0.8V when V_X is at its final value.

The internal 1.15µA pull up current on TRACK/SS can cause a tracking error at V_{OUT} when using a resistor divider on TRACK/SS. For example, if a 59k resistor is chosen for R2X, the R2X current will be about 10µA (0.6V/59k). In this case, the 1.15µA internal current source will cause about 11% (1.15µA/10µA) tracking error, which is about 66mV referred to V_{FB}. This is acceptable for most applications. If a better tracking accuracy is required, the value of R2X can be reduced or the 1.15µA current can be taken into account in the equations.

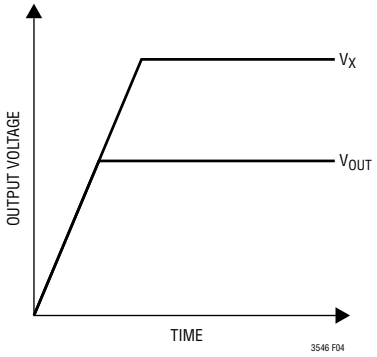

Figure 4. Coincident Tracking

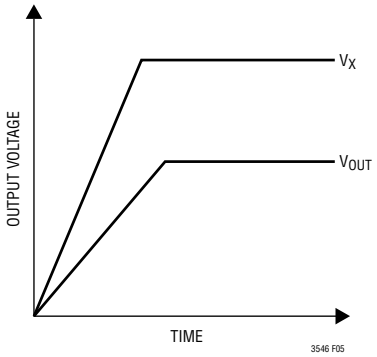

Figure 5. Ratiometric Tracking

Table 2 summarizes the different states in which the TRACK/SS can be used.

Table 2. The States of the TRACK/SS Pin

TRACK/SS PIN	RESULT
Capacitor to Ground	External Soft-Start
Floating	Internal Soft-Start
Resistor Divider	V_{OUT} Tracking an External Voltage V_X

Regardless of the mode implemented, the TRACK/SS pin should never be pulled high externally as this will result in excessive current during shutdown.

The LTC3546 can smoothly handle starting up into a pre-biased output. The tracking function will pick up from the pre-biased voltage and ramp the output up from there.

Mode Selection

The SYNC/MODE pin is a multipurpose pin which provides mode selection and frequency synchronization. Connecting this pin to V_{IN} enables Burst Mode operation for both reg-

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ulators. This mode provides the best low current efficiency at the cost of a higher output voltage ripple. When SYNC/MODE is connected to ground, pulse-skipping operation is selected for both regulators. This mode provides a lower output voltage and current ripple at the cost of low current efficiency. Applying $V_{IN}/2$ results in forced continuous mode for both regulators. This mode creates a fixed output ripple and is capable of sinking some current (about $1/2 \bullet \Delta I_L$). Since the switching noise is constant in this mode, it is also the easiest to filter out. During initial start-up, pulse-skipping mode is forced until the PGOOD pin goes high.

The LTC3546 can also be synchronized to an external clock signal by the SYNC/MODE pin. An internal phase locked loop locks to the incoming signal to provide for 180° out-of-phase operation as well as correct slope compensation. With external synchronization the FREQ pin is used for externally compensating the internal phase locked loop. Typical values used for compensation are 200k and 100pf, as shown in Figure 6. During synchronization, the regulator operating mode is forced to pulse skipping. The P-channel switch turn on is synchronized to the rising edge of the external clock.

When using an external clock, with the PHASE pin low, the switching of the two channels occur 180° out-of-phase.

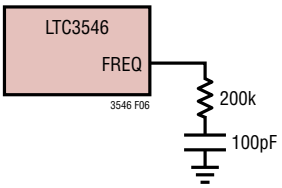

Figure 6. PLL Compensation

Checking Transient Response

The I_{TH} pin compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the I_{TH} pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated using the percentage of overshoot seen at this pin, or by examining the rise time at this pin.

The I_{TH} external components shown in the Figure 9 circuit will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because of various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. The ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH}. If R_{ITH} is increased by the same factor that C_{ITH} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, feedforward capacitors, C_{FF1} and C_{FF2}, can be added to improve the high frequency response, as shown in Figure 9. Capacitor C_{FF1} provides phase lead by creating a high frequency zero with R1 which improves the phase margin for the 1A SW1 channel. Capacitor C_{FF2} provides phase lead by creating a high frequency zero with R3 which improves the phase margin for the 3A SW1D/SW2 channel.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual

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overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

Although a buck regulator is capable of providing the full output current in dropout, it should be noted that as the input voltage V_{IN} drops toward V_{OUT}, the load step capability does decrease due to the decreasing voltage across the inductor. Applications that require large load step capability near dropout should use a different topology such as SEPIC, Zeta, or single inductor, positive buck boost.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A hot swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (P1 + P2 + P3 + \ldots)$$

where P1, P2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3546 circuits: 1) LTC3546 V_{IN} current, 2) switching losses, 3) I^2R losses, 4) other losses.

1. The V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no-load.
2. The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge moves from V_{IN} to ground. The resulting charge over the switching period is a current out of V_{IN} that is typically much larger than the DC bias current. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.
3. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and the external inductor, R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)}TOP)(DC) + (R_{DS(ON)}BOT)(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

   $$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

   Where R_L is the resistance of the inductor.
4. Other hidden losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3546 requires the backplane metal (Pin 29) to be well soldered to the PC board. This gives the UFD package exceptional thermal properties, compared to similar packages of this size, making it difficult in normal opera-

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tion to exceed the maximum junction temperature of the part. In a majority of applications, the LTC3546 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3546 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both switches in both regulators will be turned off and the SW nodes will become high impedance.

To avoid the LTC3546 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As an example, consider the case when the LTC3546 is in dropout in both regulators at an input voltage of 3.3V with load currents of 3A (SW1D externally connected to SW2) and 1A. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the 3A P-channel switch parallel combination of SW2 and SW1D is 0.06Ω and the $R_{DS(ON)}$ of the 1A P-channel switch is 0.18Ω. The power dissipated by the part is:

$$P_D = I1^2\ R_{DS(ON)1} + I2^2\ R_{DS(ON)2}$$

$$P_D = 3^2 \bullet 0.064 + 1^2 \bullet 0.19$$

$$P_D = 0.77W$$

The UFD package junction-to-ambient thermal resistance, θ_{JA}, is about 34°C/W. Therefore, the junction temperature of the regulator operating in a 85°C ambient temperature is approximately:

$$T_J = 0.77 \bullet 34 + 85$$

$$T_J = 111.2°C$$

This junction temperature is obtained from an $R_{DS(ON)}$ at 25°C. At 125°C the $R_{DS(ON)}$ increases by about 30%. This will put the junction temperature at 122°C. If the supply is lower, like 2.3V, the $R_{DS(ON)}$ is higher still. Special care needs to be taken if the part is expected to be operating in dropout so that the maximum junction temperature of 125°C is not exceeded.

Design Example

As a design example, consider using the LTC3546 in a portable application with a Li-Ion battery. The battery provides a V_{IN} = 2.3V to 4.2V. One output requires 1.8V at 2.5A in active mode, and 1mA in standby mode. The other output requires 1.2V at 800mA in active mode, and 500µA in stand-by mode. Since both loads still need power in stand-by, Burst Mode operation is selected for good low load efficiency.

First, determine what frequency should be used. Higher frequency results in a lower inductor value for a given ΔI_L (ΔI_L is estimated as $0.35I_{LOAD(MAX)}$). Reasonable values for wire wound surface mount inductors are in the 1µH and up. Look at the different frequencies with the ΔI_L = $0.35I_{LOAD(MAX)}$.

CONVERTER OUTPUT	$I_{LOAD(MAX)}$	ΔI_L
SW2/SW1D, 1.2V	2.5A	875mA
SW1, 1.8V	800mA	280mA

Using the 1.5MHz frequency setting (FREQ = 143k to GNDA) we get the following equations for L1 and L2.

$$L1 = \frac{1.2V}{1.5MHz \bullet 280mA} \bullet \left(1 - \frac{1.2V}{4.2V}\right) = 2\mu H$$

$$L2 = \frac{1.8V}{1.5MHz \bullet 875mA} \bullet \left(1 - \frac{1.8V}{4.2V}\right) = 0.78\mu H$$

Use 1µH and 2.2µH.

C_{OUT} selection is typically based on load step rather than the ripple requirements. The minimum required capacitance will increase with a decrease in compensation loop bandwidth and/or increases in maximum load step or output voltage tolerance. A good starting point is about 22µF per ampere of output current for a nominal

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operating frequency of 1.5MHz and assumes roughly a 300mA/A load step.

$$C_{OUT1} = \frac{22\mu F}{A} \bullet 0.8A \bullet \frac{280mA}{\frac{300mA}{A} \bullet 0.8A} = 20.5\mu F$$

$$C_{OUT1} = \frac{22\mu F}{A} \bullet 2.5A \bullet \frac{875mA}{\frac{300mA}{A} \bullet 2.5A} = 64.2\mu F$$

The closest values are 22µF and 68µF.

The output voltages can now be programmed by choosing the values of R1, R2, R3, and R4. To maintain high efficiency, the current in these resistors should be kept small. Choosing 2µA with the 0.6V feedback voltages makes R2 and R4 equal to 300k. A close standard 1% resistor is 301k. This then makes R1 = 300k. A close standard 1% is 301k. R3 then equals 600k. A close 1% resistor is 604k.

The compensation should be optimized for these components by examining the load step response but a good place to start for the LTC3546 is with a 13kΩ and 1000pF filter on both I_{TH1} and I_{TH2}. The output capacitor may need to be increased depending on the actual transient during a load step.

The PGOOD pin is a common drain output and requires a pull-up resistor. A 100k resistor is used for adequate speed. Figure 9 shows a complete schematic for this design.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3546. These items are also illustrated graphically in the layout diagram of Figure 7. Check the following in your layout.

1. Make sure SW1, SW2A, SW2B and SW1D are connected on the PC board through a wide piece of copper.
2. All, or part, of C_{IN} should connect from Pin 9 to Pin 14 on the same side of the PC board as the chip and as close to the chip as possible, where the SW traces will go directly under the capacitor. C_{IN} provides the AC current to the internal power MOSFETs and their drivers.
3. Are the respective C_{OUT}, L closely connected? The (–) plate of C_{OUT1} returns current to PGND1, and the (–) plate of C_{OUT2} returns current to the PGND2. The (–) plate of C_{IN} should also return current to PGND1 and PGND2.
4. The resistor divider, R1 and R2, must be connected between the (+) plate of C_{OUT1} and a ground line terminated near GNDA. The resistor divider R3 and R4, must be connected between the (+) plate of C_{OUT2} and the ground connection terminated to the GNDA pin. The feedback signals V_{FB1} and V_{FB2} should be routed away from noise components and traces, such as the SW lines, and its trace should be minimized.
5. When using the R_{FREQ} resistor, the ground connection of the resistor should be terminated to the GNDA pin. When using the internal PLL, the ground connection of the R-C compensation network should be terminated to the GNDA pin.
6. Keep sensitive components away from the SW pins. The input capacitor C_{IN}, the compensation capacitors C_{FF1}, C_{FF2}, C_{ITH1}, and C_{ITH2} and all resistors R1, R2, R3, R4, R_{ITH1} and R_{ITH2} should be routed away from the SW traces and the inductors L1 and L2.
7. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the SGND pin at one point which is then connected to the PGND1/PGND2/PGND1D/GNDD pins.
8. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to the Exposed Pad (Pin 29).

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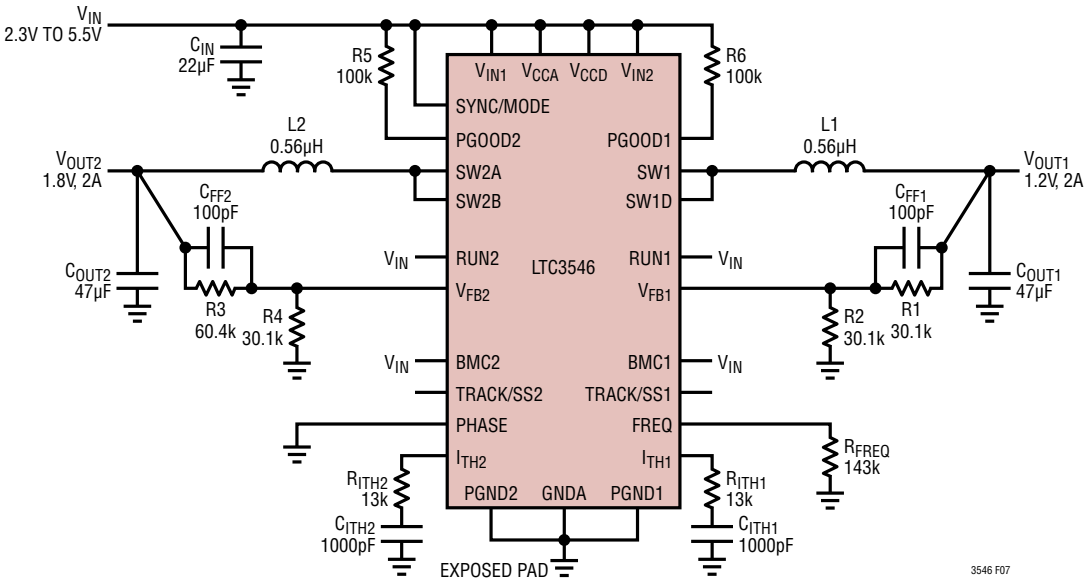

Figure 7. Typical Schematic for 2A/2A Regulator

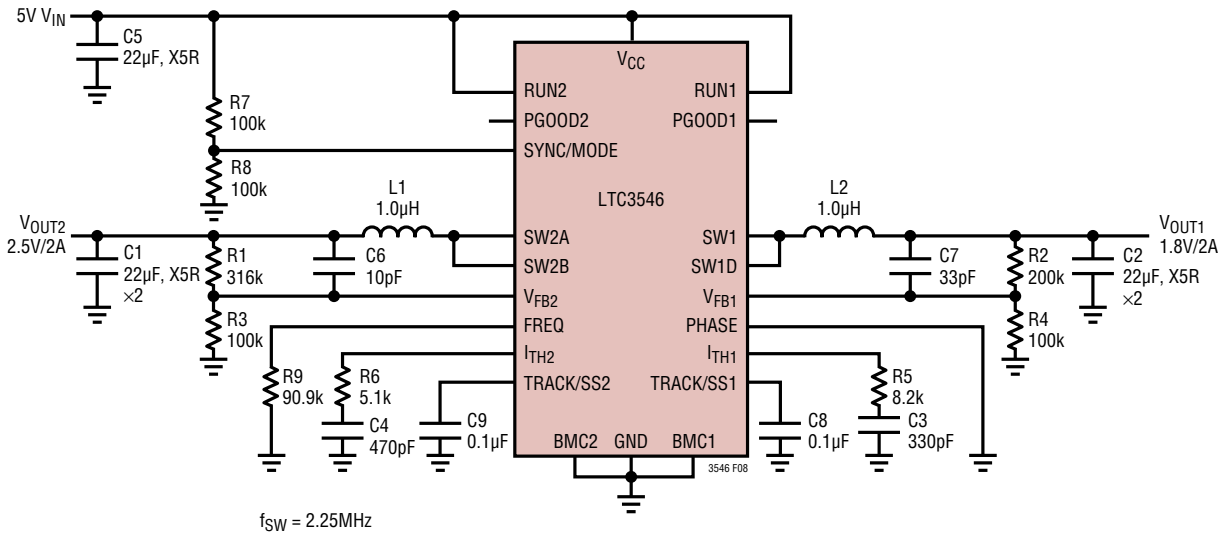

Figure 8. A 2.25MHz Fixed Frequency 2A/2A Regulator

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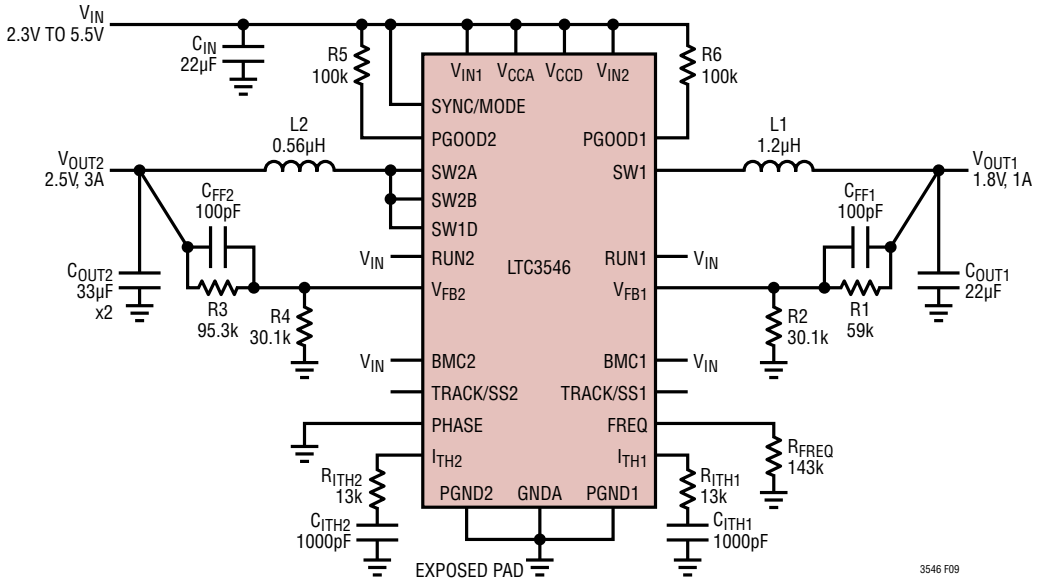
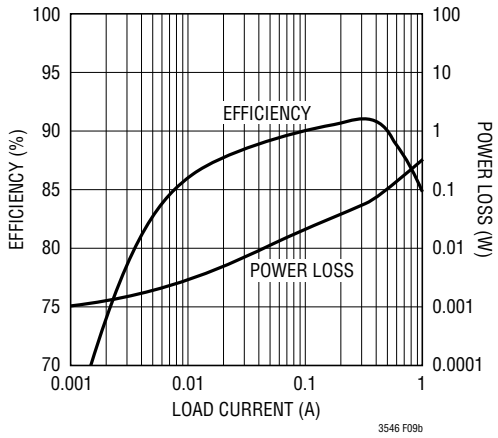
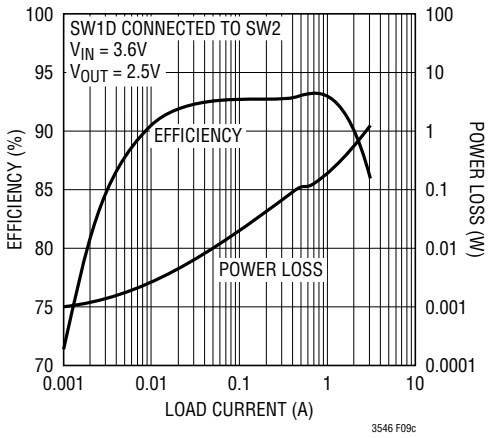


Figure 9. Typical Schematic for 3A/1A Regulator

OUT1 Efficiency (Burst Mode Operation)



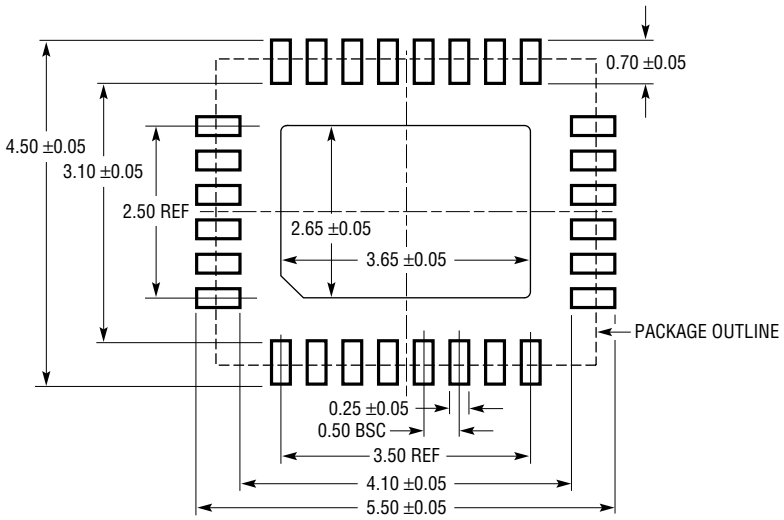
OUT2 Efficiency (Burst Mode Operation)



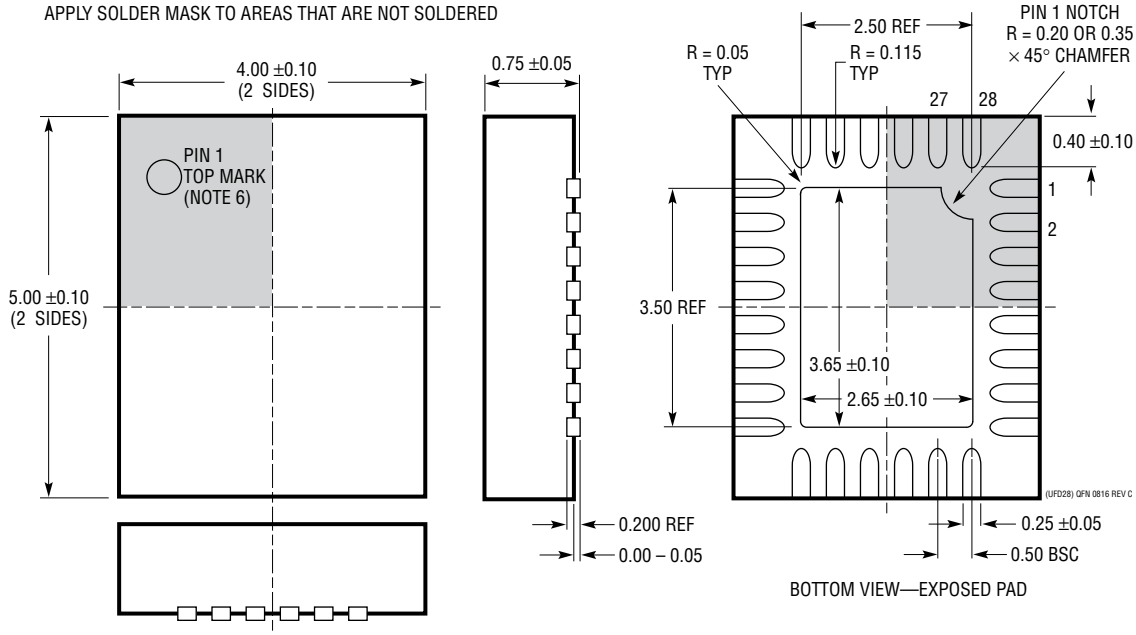
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3546#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



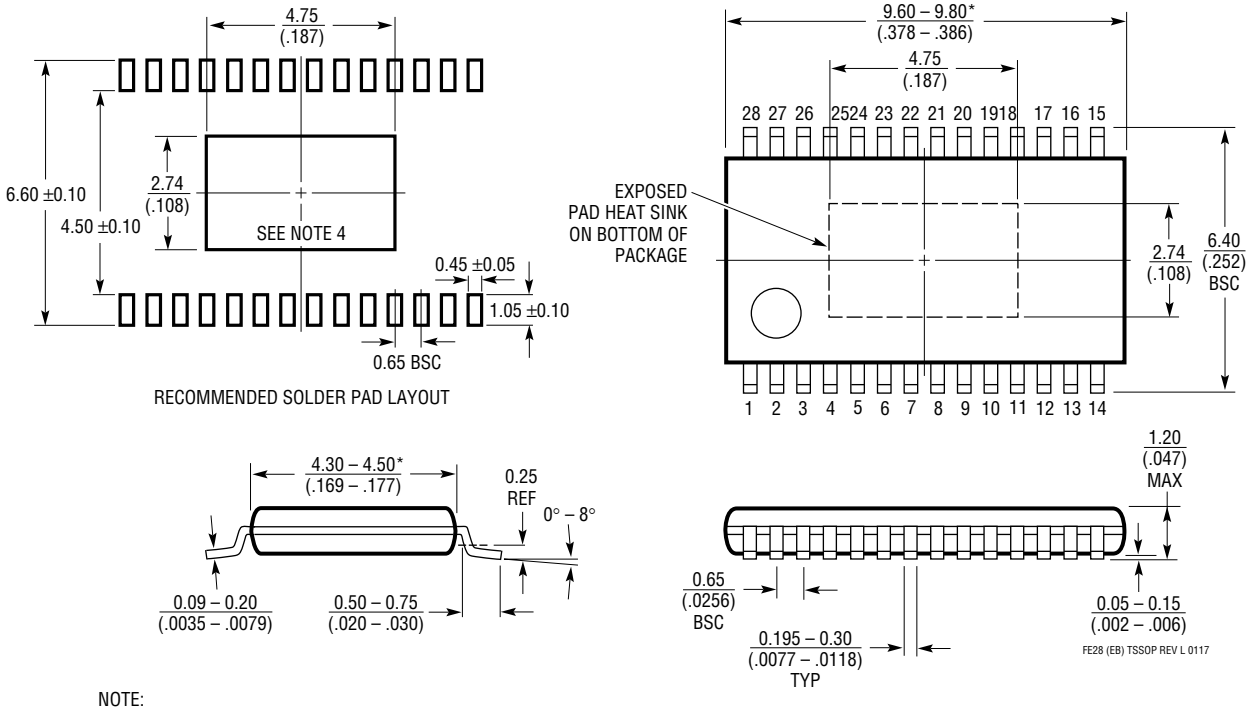
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3546#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	03/13	Modified Typical App Circuit V_{IN} Range	1
		Clarified Electrical Characteristics Notes for Temp Ranges	3, 4
		Clarified BMC, BMC1 and GNDD pin operation	9, 10
D	02/18	Changed $V_{IN(MIN)}$ to 2.3V	1, 4, 22, 24, 26

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3406A/ LTC3406B	600mA, 1.5MHz, Synchronous Step-Down DC/DC Converters	96% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT™ Package
LTC3407A-2	Dual 800mA/800mA 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E, 3mm × 3mm DFN-10 Packages
LTC3409	600mA, 1.7MHz/2.6MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, $V_{IN(MIN)}$: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 65µA, I_{SD} < 1µA, 3mm × 3mm DFN-8 Package
LTC3410/ LTC3410B	300mA, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26µA, I_{SD} < 1µA, SC70 Package
LTC3411A	1.25A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, MS10, 3mm × 3mm DFN-10 Packages
LTC3412A	2.5A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, 4mm × 4mm QFN-16, TSSOP-16E Packages
LTC3417A-2	Dual 1.5A/1A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$: 2.3V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 125µA, I_{SD} < 1µA, TSSOP-16E, 3mm × 5mm DFN-16 Packages
LTC3419/ LTC3419-1	Dual 600mA/600mA 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 35µA, I_{SD} < 1µA, MS10, 3mm × 3mm DFN-10 Packages
LTC3542	500mA, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 26µA, I_{SD} < 1µA, 2mm × 2mm DFN-6, ThinSOT Packages
LTC3544/ LTC3544B	Quad 100mA/200mA/200mA/300mA, 2.25MHz Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$: 2.3V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm QFN-16 Package
LTC3545/ LTC3545-1	Triple, 800mA ×3, 2.25MHz Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$: 2.3V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 58µA, I_{SD} < 1µA, 3mm × 3mm QFN-16 Package
LTC3547/ LTC3547B	Dual 300mA, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, DFN-8 Package
LTC3548/ LTC3548-1/ LTC3548-2	Dual 400mA and 800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E, 3mm × 3mm DFN-10 Packages
LTC3560	800mA 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 16µA, I_{SD} < 1µA, ThinSOT Package
LTC3561	1.25A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 240µA, I_{SD} < 1µA, 3mm × 3mm DFN-8 Package
LTC3562	Quad, I^2C Interface, 600mA/600mA/400mA/400mA , 2.25MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$: 2.9V to 5.5V, $V_{OUT(MIN)}$ = 0.425V, I_Q = 100µA, I_{SD} < 1µA, 3mm × 3mm QFN-20 Package

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