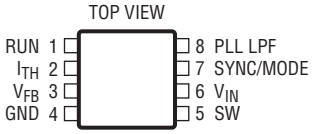
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 11V
I_{TH}, PLL LPF Voltage ..... –0.3V to 2.7V
RUN, V_{FB} Voltages ..... –0.3V to V_{IN}
SYNC/MODE Voltage ..... –0.3V to V_{IN}
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
P-Channel MOSFET Source Current (DC) 800mA
N-Channel MOSFET Sink Current (DC) 800mA
Peak SW Sink and Source Current 1.5A
Operating Temperature Range (Note 2) ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1877EMS8#PBF	LTC1877EMS8#TRPBF	LTLU	8-Lead Plastic MSOP	–40°C to 85°C
LTC1877IMS8#PBF	LTC1877IMS8#TRPBF	LTLV	8-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VFB}	Feedback Current	(Note 4)	●		4	30	nA
V_{FB}	Regulated Output Voltage	(Note 4) 0°C ≤ T_A ≤ 85°C (Note 4) –40°C ≤ T_A ≤ 85°C	 ●	0.784 0.74	0.8 0.8	0.816 0.84	V V
ΔV_{OVL}	Output Overvoltage Lockout	$\Delta V_{OVL} = V_{OVL} - V_{FB}$	●	20	50	110	mV
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN} = 2.65V to 10V (Note 4)			0.05	0.15	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	Measured in Servo Loop; V_{ITH} = 0.9V to 1.2V Measured in Servo Loop; V_{ITH} = 1.6V to 1.2V	● ●		0.1 –0.1	0.5 –0.5	% %
V_{IN}	Input Voltage Range		●	2.65		10	V
I_Q	Input DC Bias Current Pulse-Skipping Mode Burst Mode Operation Shutdown	(Note 5) 2.65V < V_{IN} < 10V, $V_{SYNC/MODE}$ = 0V, I_{OUT} = 0A $V_{SYNC/MODE}$ = V_{IN}, I_{OUT} = 0A V_{RUN} = 0V, V_{IN} = 10V			 230 10 0	 350 15 1	 µA µA µA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.8V V_{FB} = 0V		495	550 80	605	kHz kHz
f_{SYNC}	SYNC Capture Range			400		700	kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{PLL\ LPF}$	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{PLLIN} < f_{OSC}$ $f_{PLLIN} > f_{OSC}$	 ● ●	 3 –3	 10 –10	 20 –20	 µA µA
R_{PFET}	$R_{DS(ON)}$ of P-Channel MOSFET	I_{SW} = 100mA			0.65	0.85	Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel MOSFET	I_{SW} = –100mA			0.75	0.95	Ω
I_{PK}	Peak Inductor Current	V_{FB} = 0.7V, Duty Cycle < 35%		0.8	1.0	1.25	A
I_{LSW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 8.5V, V_{IN} = 8.5V			±0.01	±1	µA
$V_{SYNC/MODE}$	SYNC/MODE Threshold		●	0.3	1.0	1.5	V
$I_{SYNC/MODE}$	SYNC/MODE Leakage Current				±0.01	±1	µA
V_{RUN}	RUN Threshold		●	0.3	0.7	1.5	V
I_{RUN}	RUN Input Current				±0.01	±1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC1877E is guaranteed to meet specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC1877I is guaranteed over the full –40°C to 85°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

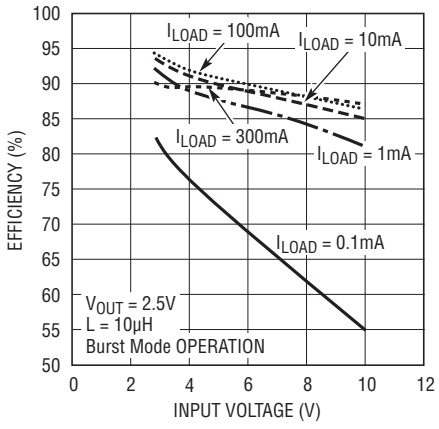
LTC1877EMS8: $T_J = T_A + (P_D)(150°C/W)$

Note 4: The LTC1877 is tested in a feedback loop which servos V_{FB} to the balance point for the error amplifier (V_{ITH} = 1.2V).

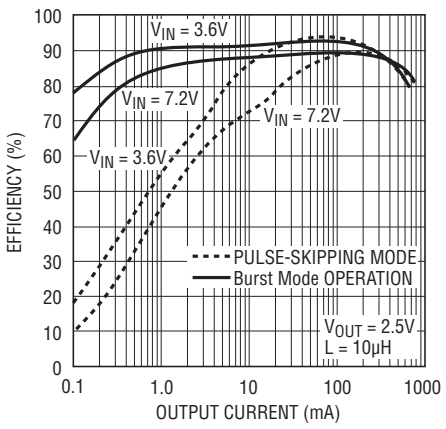
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

TYPICAL PERFORMANCE CHARACTERISTICS

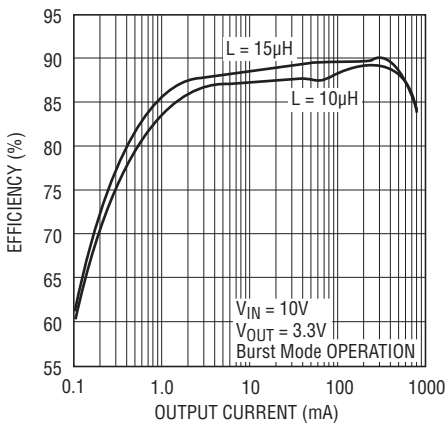
Efficiency vs Input Voltage



Efficiency vs Output Current

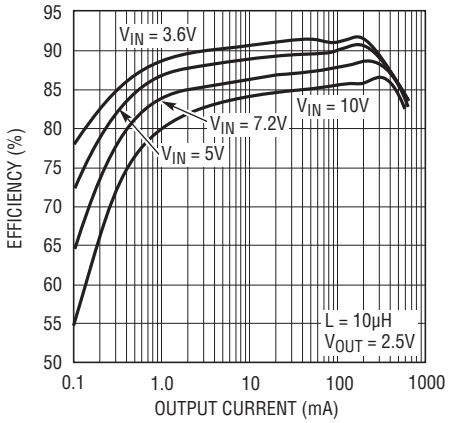


Efficiency vs Output Current

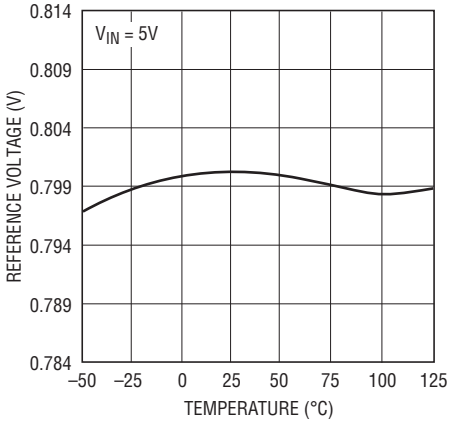


TYPICAL PERFORMANCE CHARACTERISTICS

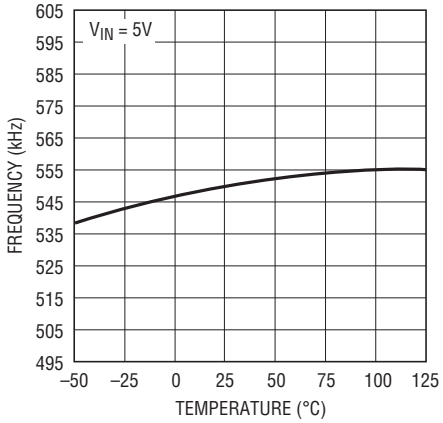
Efficiency vs Output Current



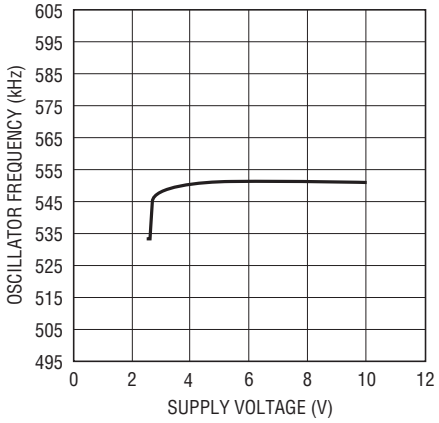
Reference Voltage vs Temperature



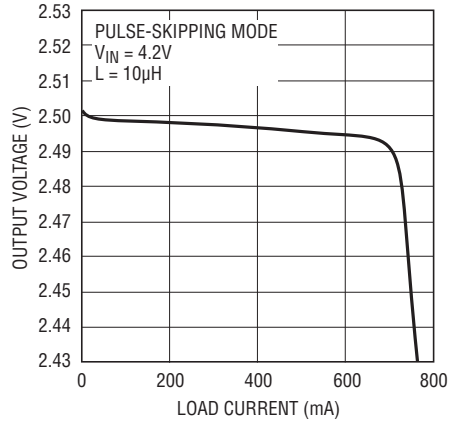
Oscillator Frequency vs Temperature



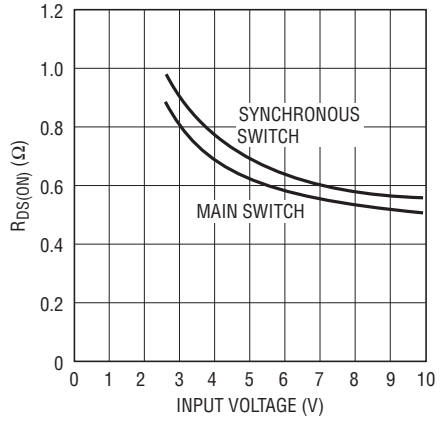
Oscillator Frequency vs Supply Voltage



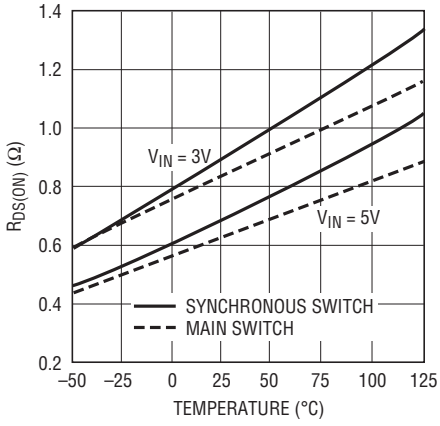
Output Voltage vs Load Current



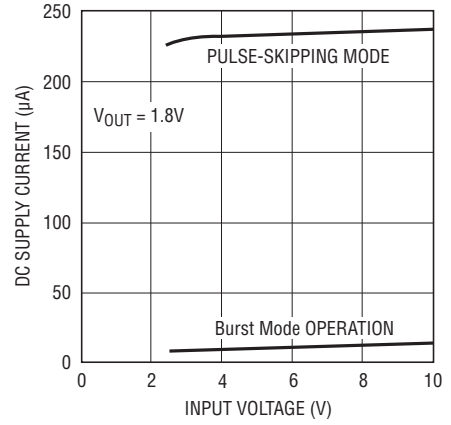
RDS(ON) vs Input Voltage



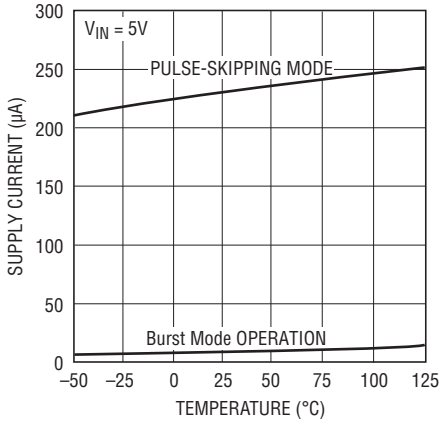
RDS(ON) vs Temperature



DC Supply Current vs Input Voltage

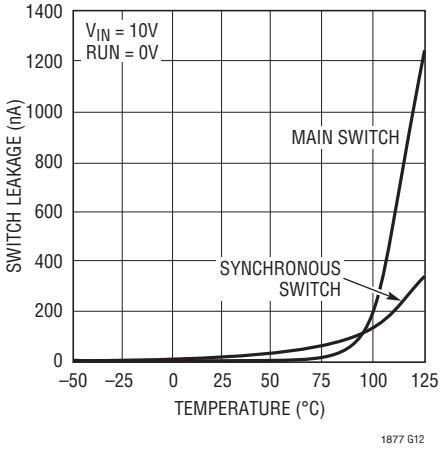


DC Supply Current vs Temperature

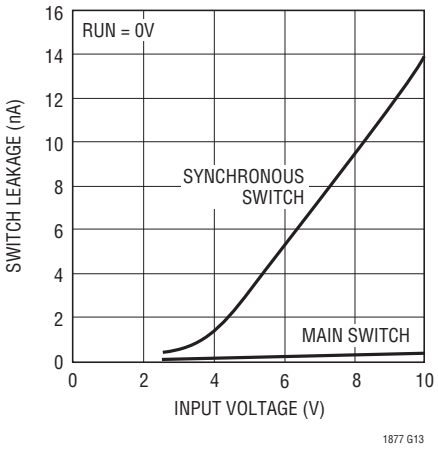


TYPICAL PERFORMANCE CHARACTERISTICS

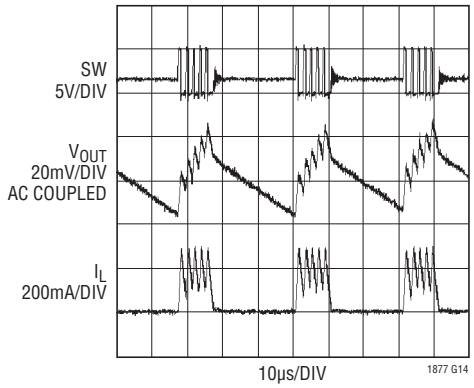
Switch Leakage vs Temperature



Switch Leakage vs Input Voltage

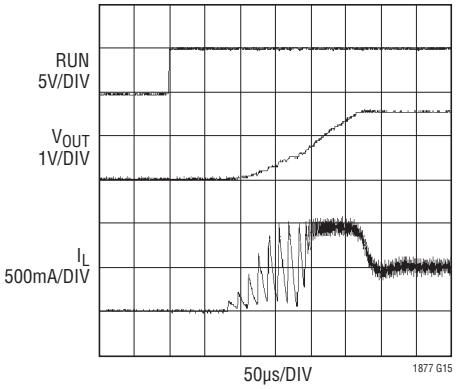


Burst Mode Operation



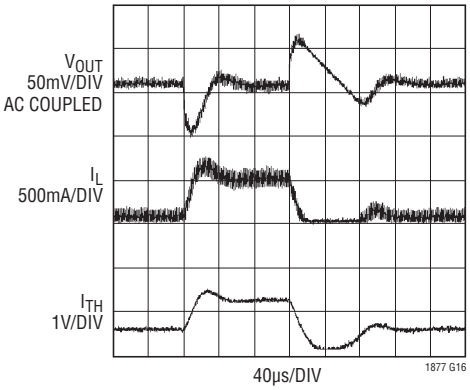
V_{IN} = 5V
V_{OUT} = 1.5V
C_{IN} = 10µF
L = 10µH
C_{OUT} = 47µF
I_{LOAD} = 50mA

Start-Up from Shutdown



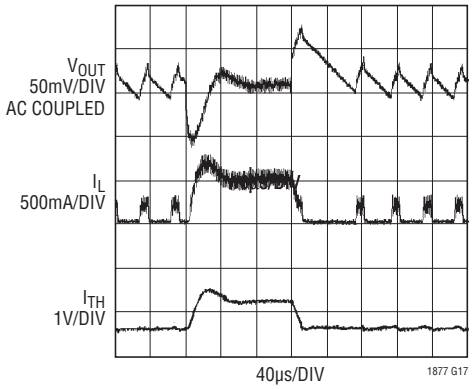
V_{IN} = 5V
V_{OUT} = 1.5V
L = 10µH
C_{IN} = 10µF
C_{OUT} = 47µF
I_{LOAD} = 500mA

Load Step Response



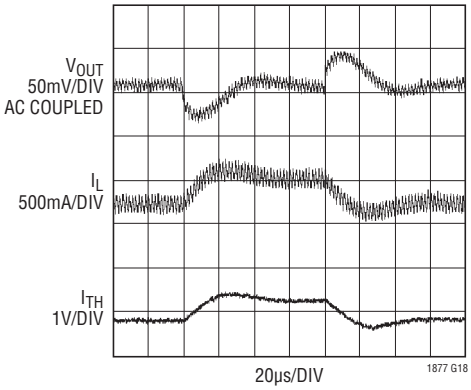
V_{IN} = 5V
V_{OUT} = 1.5V
L = 10µH
C_{IN} = 10µF
C_{OUT} = 47µF
I_{LOAD} = 50mA TO 500mA
PULSE-SKIPPING MODE

Load Step Response



V_{IN} = 5V
V_{OUT} = 1.5V
L = 10µH
C_{IN} = 10µF
C_{OUT} = 47µF
I_{LOAD} = 50mA TO 500mA
Burst Mode OPERATION

Load Step Response



V_{IN} = 5V
V_{OUT} = 1.5V
L = 10µH
C_{IN} = 10µF
C_{OUT} = 47µF
I_{LOAD} = 200mA TO 500mA
PULSE-SKIPPING MODE

PIN FUNCTIONS

RUN (Pin 1): Run Control Input. Forcing this pin below 0.4V shuts down the LTC1877. In shutdown, all functions are disabled drawing <1µA supply current. Forcing this pin above 1.2V enables the LTC1877. Do not leave RUN floating.

I_{TH} (Pin 2): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is from 0.5V to 1.9V.

V_{FB} (Pin 3): Feedback Pin. Receives the feedback voltage from an external resistive divider across the output.

GND (Pin 4): Ground Pin.

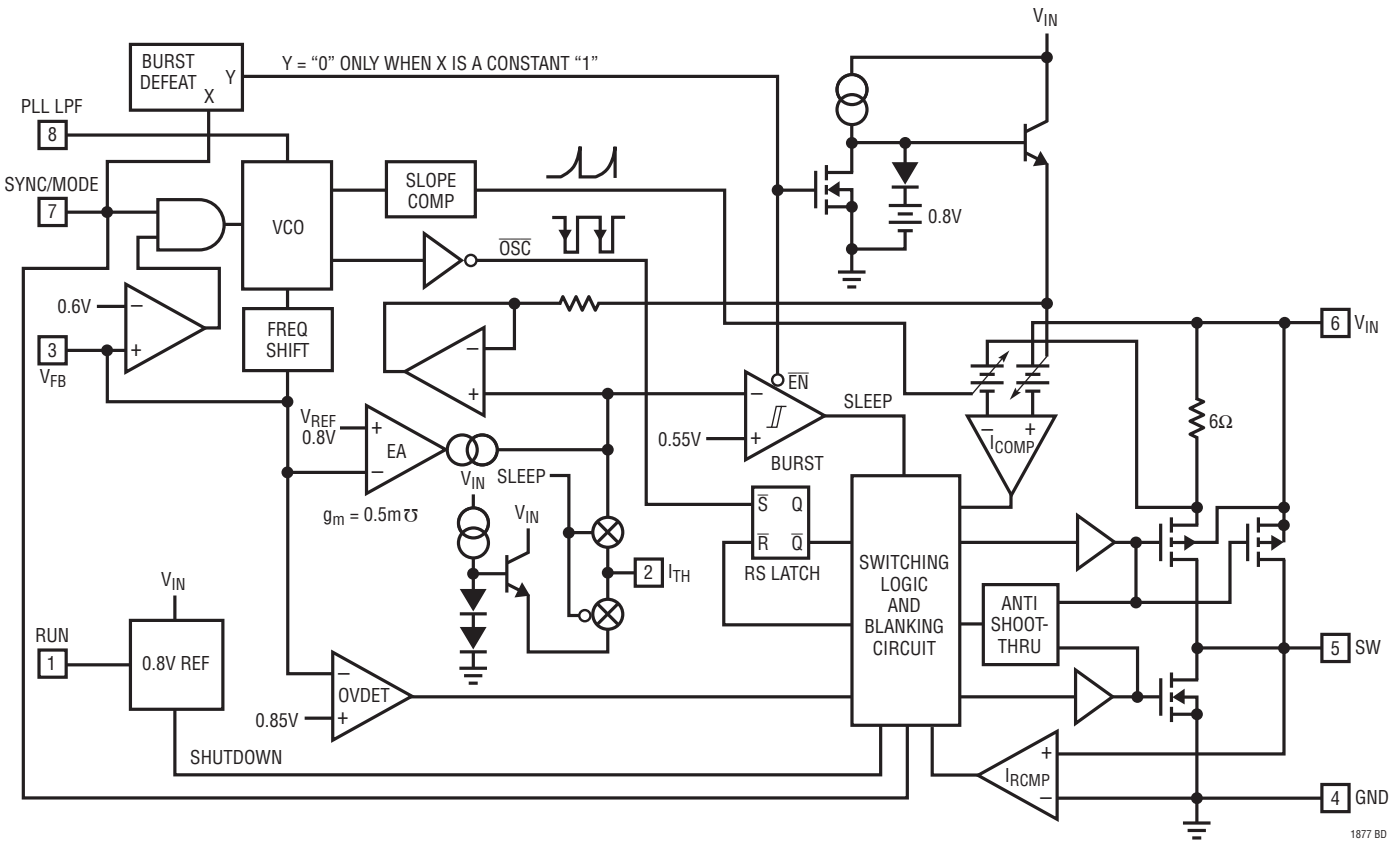
SW (Pin 5): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

V_{IN} (Pin 6): Main Supply Pin. Must be closely decoupled to GND, Pin 4.

SYNC/MODE (Pin 7): External Clock Synchronization and Mode Select Input. To synchronize with an external clock, apply a clock with a frequency between 400kHz and 700kHz. To select Burst Mode operation, tie to V_{IN}. Grounding this pin selects pulse-skipping mode. Do not leave this pin floating.

PLL LPF (Pin 8): Output of the Phase Detector and Control Input of Oscillator. Connect a series RC lowpass network from this pin to ground if externally synchronized. If unused, this pin may be left open.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

The LTC1877 uses a constant-frequency, current mode step-down architecture. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of error amplifier EA. The V_{FB} pin, described in the Pin Functions section, allows EA to receive an output feedback voltage from an external resistive divider. When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.8V reference, which in turn, causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse as indicated by the current reversal comparator I_{RCMP}, or the beginning of the next clock cycle.

Comparator OVDET guards against transient overshoots > 6.25% by turning the main switch off and keeping it off until the fault is removed.

Burst Mode Operation

The LTC1877 is capable of Burst Mode operation in which the internal power MOSFETs operate intermittently based on load demand. To enable Burst Mode operation, simply tie the SYNC/MODE pin to V_{IN} or connect it to a logic high ($V_{SYNC/MODE}$ > 1.5V). To disable Burst Mode operation and enable PWM pulse-skipping mode, connect the SYNC/MODE pin to GND. In this mode, the efficiency is lower at light loads, but becomes comparable to Burst Mode operation when the output load exceeds 50mA. The advantage of pulse-skipping mode is lower output ripple and less interference to audio circuitry.

When the converter is in Burst Mode operation, the peak current of the inductor is set to approximately 250mA, even though the voltage at the I_{TH} pin indicates a lower value. The voltage at the I_{TH} pin drops when the inductor's average current is greater than the load requirement. As the I_{TH} voltage drops below approximately 0.55V, the BURST comparator trips, causing the internal sleep line to go high and forces off both power MOSFETs. The I_{TH} pin is then disconnected from the output of the EA amplifier and parked a diode voltage above ground.

In sleep mode, both power MOSFETs are held off and a majority of the internal circuitry is partially turned off, reducing the quiescent current to 10µA. The load current is now being supplied solely from the output capacitor. When the output voltage drops, the I_{TH} pin reconnects to the output of the EA amplifier and the top MOSFET is again turned on and this process repeats.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator is reduced to about 80kHz, one-seventh the nominal frequency. This frequency foldback ensures that the inductor current has ample time to decay, thereby preventing runaway. The oscillator's frequency will progressively increase to 550kHz (or the synchronized frequency) when V_{FB} rises above 0.3V.

Frequency Synchronization

A phase-locked loop (PLL) is available on the LTC1877 to allow the internal oscillator to be synchronized to an external source connected to the SYNC/MODE pin. The output of the phase detector at the PLL LPF pin operates over a 0V to 2.4V range corresponding to 400kHz to 700kHz. When locked, the PLL aligns the turn-on of the top MOSFET to the rising edge of the synchronizing signal.

When the LTC1877 is clocked by an external source, Burst Mode operation is disabled; the LTC1877 then operates in PWM pulse-skipping mode. In this mode, when the output load is very low, current comparator I_{COMP} may remain tripped for several cycles and force the main switch to stay off for the same number of cycles. Increasing the output load slightly allows constant-frequency PWM operation to resume. This mode exhibits low output ripple as well as low audio noise and reduced RF interference while providing reasonable low current efficiency.

Frequency synchronization is inhibited when the feedback voltage V_{FB} is below 0.6V. This prevents the external clock from interfering with the frequency foldback for short-circuit protection.

OPERATION

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC1877 is designed to operate down to an input supply voltage of 2.65V although the maximum allowable output current is reduced at this low voltage. Figure 1 shows the reduction in the maximum output current as a function of input voltage for various output voltages.

Another important detail to remember is that at low input supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases. Therefore, the user should calculate the power dissipation when the LTC1877 is used at 100% duty cycle with a low input voltage (see Thermal Considerations in the Applications Information section).

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. As a result, the maximum inductor peak current is reduced for duty cycles >40%. This is shown in the decrease of the inductor peak current as a function of duty cycle graph in Figure 2.

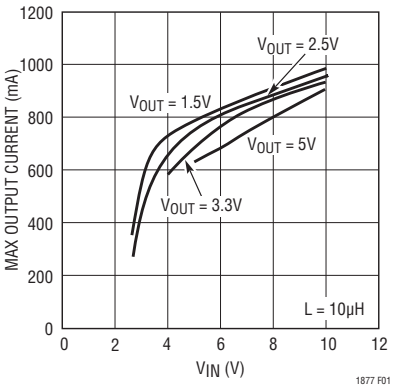


Figure 1. Maximum Output Current vs Input Voltage

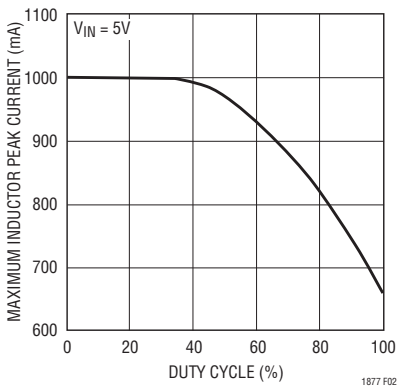


Figure 2. Maximum Inductor Peak Current vs Duty Cycle

APPLICATIONS INFORMATION

The basic LTC1877 application circuit is shown on the first page. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

Inductor Value Calculation

The inductor selection will depend on the operating frequency of the LTC1877. The internal nominal frequency is 550kHz, but can be externally synchronized from 400kHz to 700kHz.

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. However, operating at a higher frequency generally results in lower efficiency because of increased internal gate charge losses.

The inductor value has a direct effect on ripple current. The ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

APPLICATIONS INFORMATION

Accepting larger values of ΔI_L allows the use of low inductance, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$.

The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 250mA. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Kool Mμ (from Magnetics, Inc.) is a very good, low loss core material for toroids with a soft saturation characteristic. Molypermalloy is slightly more efficient at high (>200kHz) switching frequencies but quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire, while inductors wound on bobbins are generally easier to surface mount. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Dale and Sumida.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{required}\ I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. For the LTC1877, the general rule for proper operation is:

C_{OUT} required ESR < 0.25Ω

The choice of using a smaller output capacitance increases the output ripple voltage due to the frequency dependent term but can be compensated for by using capacitor(s) of very low ESR to maintain low ripple voltage. The I_{TH} pin compensation components can be optimized to provide stable high performance transient response regardless of the output capacitor selected.

ESR is a direct function of the volume of the capacitor. Manufacturers such as Taiyo Yuden, AVX, Sprague, Kemet and Sanyo should be considered for high performance ca-

APPLICATIONS INFORMATION

pacitors. The POSCAP solid electrolytic capacitor available from Sanyo is an excellent choice for output bulk capacitors due to its low ESR/size ratio. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

When using tantalum capacitors, it is critical that they are surge tested for use in switching power supplies. A good choice is the AVX TPS series of surface mount tantalum, available in case heights ranging from 2mm to 4mm. Other capacitor types include KEMET T510 and T495 series and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.8V\left(1+\frac{R2}{R1}\right) \quad (2)$$

The external resistive divider is connected to the output, allowing remote voltage sensing, as shown in Figure 3.

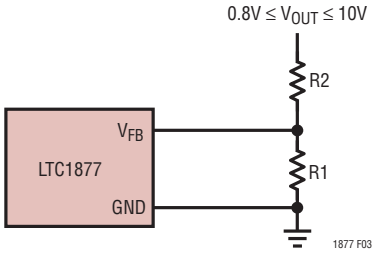


Figure 3. Setting the LTC1877 Output Voltage

Phase-Locked Loop and Frequency Synchronization

The LTC1877 has an internal voltage-controlled oscillator and phase detector comprising a phase-locked loop. This allows the top MOSFET turn-on to be locked to the rising edge of an external frequency source. The frequency range of the voltage-controlled oscillator is 400kHz to 700kHz. The phase detector used is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the V_{CO} center frequency. The PLL hold-in range Δf_H is equal to the capture range, $\Delta f_H = \Delta f_C = \pm 150kHz$.

The output of the phase detector is a pair of complementary current sources charging or discharging the external filter network on the PLL LPF pin. The relationship between the voltage on the PLL LPF pin and operating frequency is shown in Figure 4. A simplified block diagram is shown in Figure 5.

If the external frequency ($V_{SYNC/MODE}$) is greater than 550kHz, the center frequency, current is sourced continuously, pulling up the PLL LPF pin. When the external frequency is less than 550kHz, current is sunk continuously, pulling down the PLL LPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus, the voltage on the PLL LPF pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At

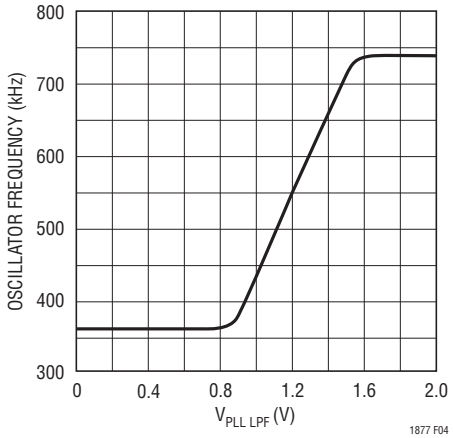


Figure 4. Relationship Between Oscillator Frequency and Voltage at PLL LPF Pin

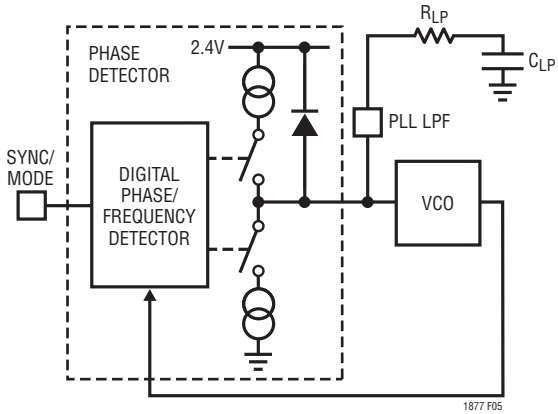


Figure 5. Phase-Locked Loop Block Diagram

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this stable operating point the phase comparator output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components C_{LP} and R_{LP} smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter component's C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF. When not synchronized to an external clock, the internal connection to the V_{CO} is disconnected. This disallows setting the internal oscillator frequency by a DC voltage on the $V_{PLL\ LPF}$ pin.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC1877 circuits: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents, whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence, as illustrated in Figure 6.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics section and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.
2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is chopped between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

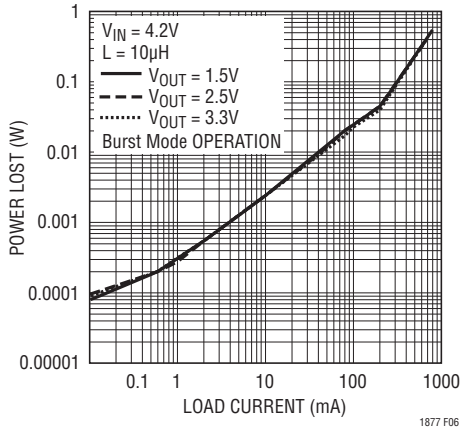

Figure 6. Power Lost vs Load Current

Thermal Considerations

In most applications the LTC1877 does not dissipate much heat due to its high efficiency. But, in applications where the LTC1877 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction

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temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC1877 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC1877 in dropout at an input voltage of 3V, a load current of 500mA, and an ambient temperature of 70°C. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 70°C is approximately 0.9Ω. Therefore, power dissipated by the part is:

$$P_D = I_{LOAD}^2 \bullet R_{DS(ON)} = 0.225W$$

For the MSOP package, the θ_{JA} is 150°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 70°C + (0.225)(150) = 104°C$$

which is below the maximum junction temperature of 125°C.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD} • ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The internal compensation provides adequate compensation for most applications. But if additional compensation is required, the I_{TH} pin can be used for external compensation using R_C, C_{C1}, as shown in Figure 7. The 220pF capacitor, C_{C2}, is typically needed for noise decoupling.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • C_{LOAD}). Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1877. These items are also illustrated graphically in the layout diagram of Figure 7. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1877 signal ground consists of the resistive divider, the optional compensation network (R_C and C_{C1}) and C_{C2}. The power ground consists of the (–) plate of C_{IN}, the (–) plate of C_{OUT} and Pin 4 of the LTC1877. The power ground traces should be kept short, direct and wide. The signal ground and power ground should converge to a common node in a star-ground configuration.
2. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and signal ground.
3. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.
4. Keep the switching node SW away from sensitive small signal nodes.

APPLICATIONS INFORMATION

Design Example

As a design example, assume the LTC1877 is used in a single lithium-ion battery-powered cellular phone application. The input voltage will be operating from a maximum of 4.2V down to about 2.7V. The load current requirement is a maximum of 0.3A but most of the time it will be in standby mode, requiring only 2mA. Efficiency at both low and high load currents is important. Output voltage is 2.5V. With this information we can calculate L using Equation (1),

$$L = \frac{1}{(f)(\Delta I_L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Substituting V_{OUT} = 2.5V, V_{IN} = 4.2V, ΔI_L=120mA and f = 550kHz in Equation (3) gives:

$$L = \frac{2.5V}{550kHz(120mA)}\left(1-\frac{2.5V}{4.2V}\right) = 15.3\mu H$$

A 15µH inductor works well for this application. For best efficiency choose a 1A inductor with less than 0.25Ω series resistance.

C_{IN} will require an RMS current rating of at least 0.15A at temperature and C_{OUT} will require an ESR of less than 0.25Ω. In most applications, the requirements for these capacitors are fairly similar.

For the feedback resistors, choose R1 = 412k. R2 can then be calculated from Equation (2) to be:

$$R2 = \left(\frac{V_{OUT}}{0.8}-1\right)R1 = 875.5k; \text{ use } 887k$$

Figure 8 shows the complete circuit along with its efficiency curve.

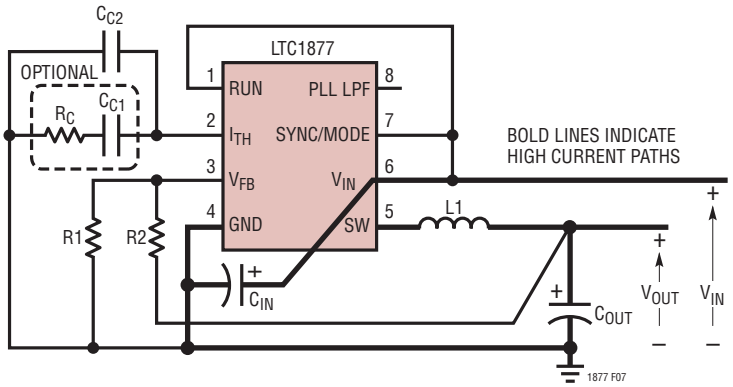


Figure 7. LTC1877 Layout Diagram

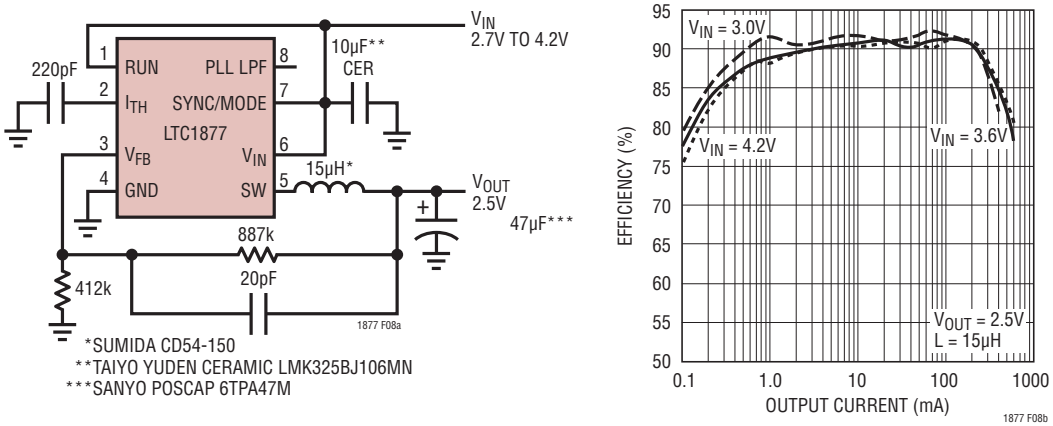
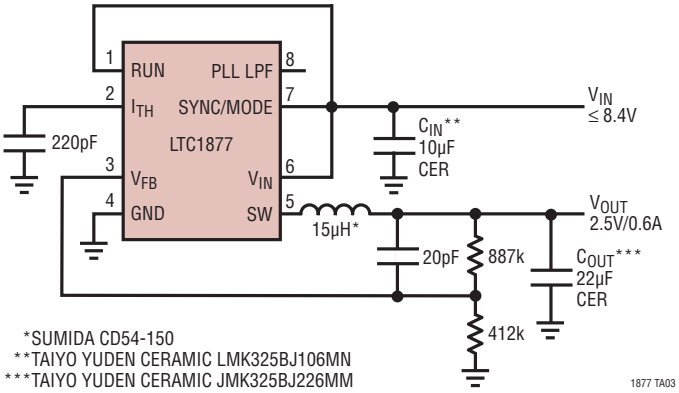


Figure 8. Single Lithium-Ion to 2.5V/0.3A Regulator from Design Example

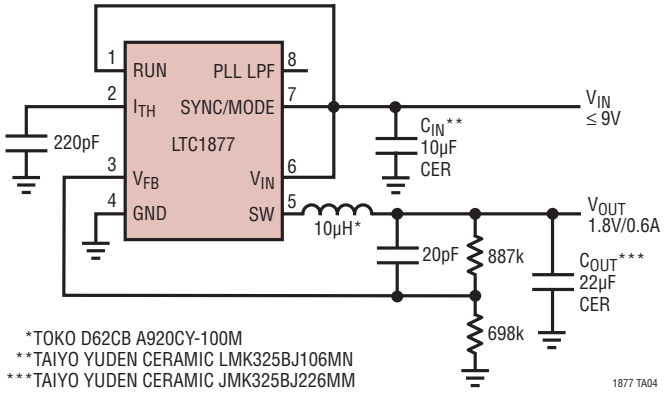
TYPICAL APPLICATIONS

Dual Lithium-Ion to 2.5V/0.6A Regulator Using All Ceramic Capacitors



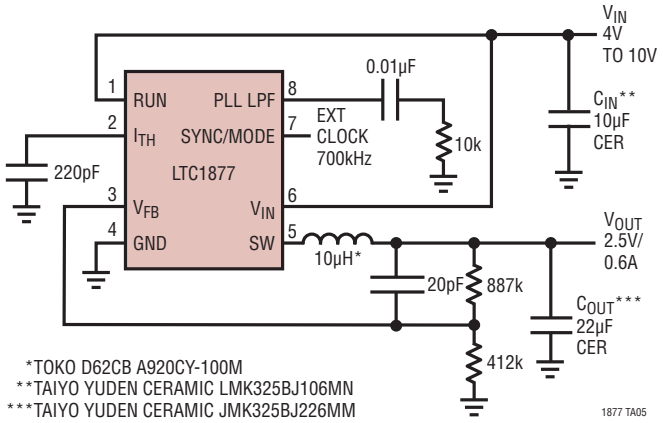
*SUMIDA CD54-150
**TAIYO YUDEN CERAMIC LMK325BJ106MN
***TAIYO YUDEN CERAMIC JMK325BJ226MM

4-to 6-Cell NiCd/NiMH to 1.8V/0.6A Regulator Using All Ceramic Capacitors



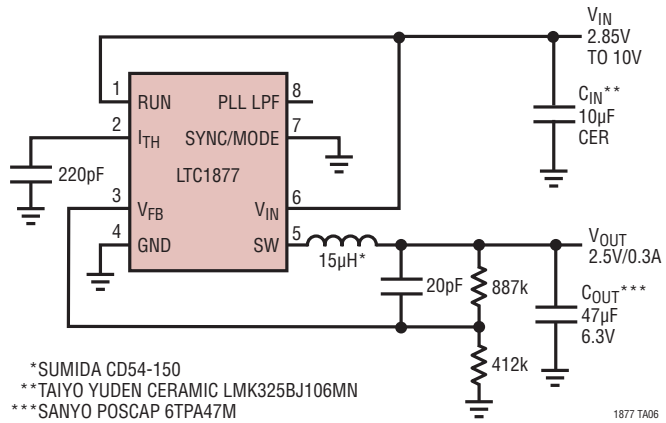
*TOKO D62CB A920CY-100M
**TAIYO YUDEN CERAMIC LMK325BJ106MN
***TAIYO YUDEN CERAMIC JMK325BJ226MM

Externally Synchronized 2.5V/0.6A Regulator Using All Ceramic Capacitors



*TOKO D62CB A920CY-100M
**TAIYO YUDEN CERAMIC LMK325BJ106MN
***TAIYO YUDEN CERAMIC JMK325BJ226MM

Low Noise 2.5V/0.3A Regulator

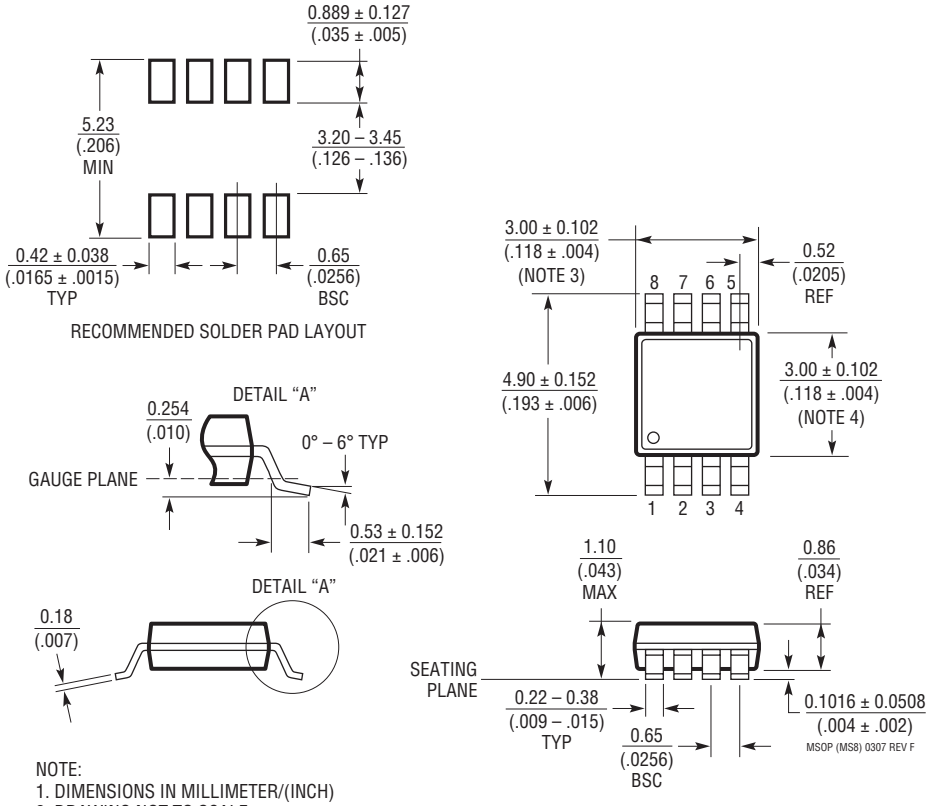


*SUMIDA CD54-150
**TAIYO YUDEN CERAMIC LMK325BJ106MN
***SANYO POSCAP 6TPA47M

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



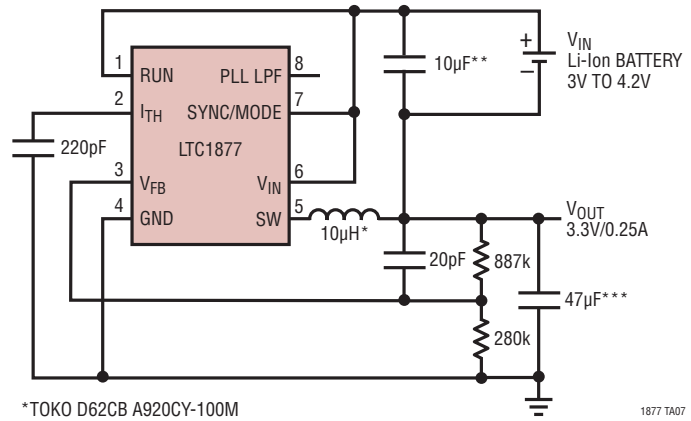
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	11/11	Part marking for LTC1877IMS8 corrected from LTLU to LTLV	2

TYPICAL APPLICATION

Single Lithium-Ion to 3.3V/0.3A Regulator



*TOKO D62CB A920CY-100M
**TAIYO YUDEN CERAMIC LMK325BJ106MN
***SANYO POSCAP 6TPA47M

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1174/LTC1174-3.3/ LTC1174-5	High Efficiency Step-Down and Inverting DC/DC Converters	Monolithic Switching Regulators, I_{OUT} to 450mA, Burst Mode Operation
LTC1265	1.2A, High Efficiency Step-Down DC/DC Converter	Constant Off-Time, Monolithic, Burst Mode Operation
LT®1375/LT1376	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency
LTC1436/LTC1436-PLL	High Efficiency, Low Noise, Synchronous Step-Down Converters	24-Pin Narrow SSOP
LTC1474/LTC1475	Low Quiescent Current Step-Down DC/DC Converters	Monolithic, I_{OUT} to 250mA, I_Q = 10µA, 8-Pin MSOP
LTC1504A	Monolithic Synchronous Step-Down Switching Regulator	Low Cost, Voltage Mode I_{OUT} to 500mA, V_{IN}: 4V to 10V
LTC1622	Low Input Voltage Current Mode Step-Down DC/DC Controller	High Frequency, High Efficiency, 8-Pin MSOP
LTC1626	Low Voltage, High Efficiency Step-Down DC/DC Converter	Monolithic, Constant Off-Time, I_{OUT} to 600mA, Low Supply Voltage Range: 2.5V to 6V
LTC1627	Monolithic Synchronous Step-Down Switching Regulator	Constant Frequency, I_{OUT} to 500mA, Secondary Winding Regulation, V_{IN}: 2.65V to 8.5V
LTC1701	Monolithic Current Mode Step-Down Switching Regulator	Constant Off-Time, I_{OUT} to 500mA, 1MHz Operation, V_{IN}: 2.5V to 5.5V
LTC1707	Monolithic Synchronous Step-Down Switching Regulator	1.19V V_{REF} Pin, Constant Frequency, I_{OUT} to 600mA, V_{IN}: 2.65V to 8.5V
LTC1735	High Efficiency, Synchronous Step-Down Converter	16-Pin SO and SSOP, V_{IN} Up to 36V, Fault Protection
LTC1772	Low Input Voltage Current Mode Step-Down DC/DC Controller	550kHz, 6-Pin SOT-23, I_{OUT} Up to 5A, V_{IN}: 2.2V to 10V
LTC1878	High Efficiency Monolithic Step-Down Regulator	550kHz, MS8, V_{IN} Up to 6V, I_Q = 10µA, I_{OUT} to 600mA

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