

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Note 2)	9V
Output Voltage (Note 5)	0.3V to -9V
Total Voltage, V_{CC} to V_{OUT} (Note 2)	12V
Input Voltage	
SHDN Pin	-0.3V to $V_{CC} + 0.3V$
REG Pin	-0.3V to 12V
ADJ, R_0 , R_1 , R_{ADJ}	$V_{OUT} - 0.3V$ to $V_{CC} + 0.3V$
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Commercial	0°C to 70°C
Extended Commercial (Note 7)	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER
S8 PACKAGE 8-LEAD PLASTIC SO *FOR FIXED VERSIONS $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$	LTC1261CS8 LTC1261CS8-4 LTC1261CS8-4.5
	S8 PART MARKING
	1261 12614 126145
TOP VIEW	ORDER PART NUMBER
S PACKAGE 14-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 110^{\circ}C/W$	LTC1261CS

Consult factory for Industrial or Military grade parts.

ELECTRICAL CHARACTERISTICS

 $V_{CC} = 3V$ to $6.5V$, $T_A = 25^{\circ}C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		0°C ≤ T_A ≤ 70°C			-40°C ≤ T_A ≤ 85°C (Note 7)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{REF}	Reference Voltage		●	1.20	1.24	1.28	1.20	1.24	1.28	V
I_S	Supply Current	No Load, SHDN Floating, Doubler Mode	●		600	1000		600	1500	μA
		No Load, SHDN Floating, Tripler Mode	●		900	1500		900	2000	μA
		No Load, $V_{SHDN} = V_{CC}$	●		5	20		5	20	μA
f_{OSC}	Internal Oscillator Frequency				550			550		kHz
P_{EFF}	Power Efficiency				65			65		%
V_{OL}	REG Output Low Voltage	$I_{REG} = 1mA$	●		0.1	0.8		0.1	0.8	V
I_{REG}	REG Sink Current	$V_{REG} = 0.8V$, $V_{CC} = 3.3V$	●	5	8		5	8		mA
		$V_{REG} = 0.8V$, $V_{CC} = 5.0V$	●	8	15		8	15		mA
I_{ADJ}	Adjust Pin Current	$V_{ADJ} = 1.24V$	●		0.01	1		0.01	1	μA
V_{IH}	SHDN Input High Voltage		●	2			2			V
V_{IL}	SHDN Input Low Voltage		●			0.8			0.8	V
I_{IN}	SHDN Input Current	$V_{SHDN} = V_{CC}$	●		5	20		5	25	μA
t_{ON}	Turn-On Time	$I_{OUT} = 15mA$			500			500		μs

ELECTRICAL CHARACTERISTICS

Doubler Mode. $V_{CC} = 5V \pm 10\%$, $C_1 = 0.1\mu F$, $C_2 = 0$ (Note 4), $C_{OUT} = 3.3\mu F$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		$0^\circ C \leq T_A \leq 70^\circ C$			$-40^\circ C \leq T_A \leq 85^\circ C$ (Note 7)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OUT}	Output Regulation (Note 2)	$-1.24V \geq V_{OUT} \geq -4V$, $0 \leq I_{OUT} \leq 8mA$	●		1	5				%
		$-1.24V \geq V_{OUT} \geq -4V$, $0 \leq I_{OUT} \leq 7mA$	●					1	5	%
		$-4V \geq V_{OUT} \geq -5V$, $0 \leq I_{OUT} \leq 8mA$ (Note 6)			2			2		%
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0V$	●		60	125		60	125	mA
V_{RIP}	Output Ripple Voltage	$I_{OUT} = 5mA$, $V_{OUT} = -4V$			5			5		mV

LTC1261CS Only. Tripler Mode. $V_{CC} = 2.7V$, $C_1 = C_2 = 0.1\mu F$ (Note 4), $C_{OUT} = 3.3\mu F$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		$0^\circ C \leq T_A \leq 70^\circ C$			$-40^\circ C \leq T_A \leq 85^\circ C$ (Note 7)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OUT}	Output Regulation	$-1.24V \geq V_{OUT} \geq -4V$, $0 \leq I_{OUT} \leq 5mA$	●		1	5		1	5	%
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0V$	●		60	125		60	125	mA
V_{RIP}	Output Ripple Voltage	$I_{OUT} = 5mA$, $V_{OUT} = -4V$			5			5		mV

LTC1261CS Only. Tripler Mode. $V_{CC} = 3.3V \pm 10\%$, $C_1 = C_2 = 0.1\mu F$ (Note 4), $C_{OUT} = 3.3\mu F$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		$0^\circ C \leq T_A \leq 70^\circ C$			$-40^\circ C \leq T_A \leq 85^\circ C$ (Note 7)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OUT}	Output Regulation (Note 2)	$-1.24V \geq V_{OUT} \geq -4.5V$, $0 \leq I_{OUT} \leq 6mA$	●		1	5		1	5	%
		$-4.5V \geq V_{OUT} \geq -5V$, $0 \leq I_{OUT} \leq 3.5mA$	●		2	5		2		%
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0V$	●		35	75		35	75	mA
V_{RIP}	Output Ripple Voltage	$I_{OUT} = 5mA$, $V_{OUT} = -4V$			5			5		mV

LTC1261CS Only. Tripler Mode. $V_{CC} = 5V \pm 10\%$, $C_1 = C_2 = 0.1\mu F$ (Note 4), $C_{OUT} = 3.3\mu F$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		$0^\circ C \leq T_A \leq 70^\circ C$			$-40^\circ C \leq T_A \leq 85^\circ C$ (Note 7)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OUT}	Output Regulation	$-1.24V \geq V_{OUT} \geq -4V$, $0 \leq I_{OUT} \leq 12mA$	●		1	5		1	5	%
		$-4V \geq V_{OUT} \geq -5V$, $0 \leq I_{OUT} \leq 10mA$	●		2	5		2	5	%
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0V$	●		35	75		35	75	mA
V_{RIP}	Output Ripple Voltage	$I_{OUT} = 5mA$, $V_{OUT} = -4V$			5			5		mV

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given at $T_A = 25^\circ C$.

Note 4: $C_1 = C_2 = 0.1\mu F$ means the specifications apply to tripler mode where $V_{CC} - V_{OUT} = 3V_{CC}$ (LTC1261CS only; the LTC1261CS8 cannot be connected in tripler mode) with C_1 connected between C_1^+ and C_1^- and C_2 connected between C_2^+ and C_2^- . $C_2 = 0$ implies doubler mode where $V_{CC} - V_{OUT} = 2V_{CC}$; for the LTC1261CS this means C_1 connects from C_1^+

to C_2^- with C_1^- and C_2^+ floating. For the LTC1261CS8 in doubler mode, C_1 connects from C_1^+ to C_1^- ; there are no C_2 pins.

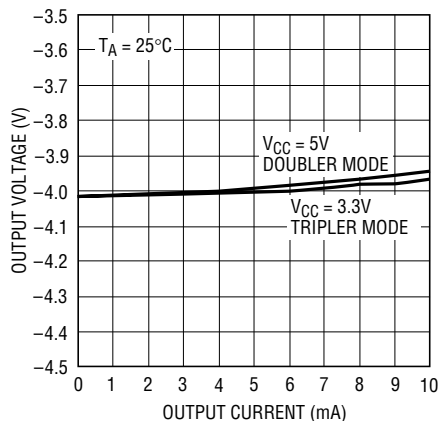
Note 5: Setting output to $< -7V$ will exceed the absolute voltage maximum rating with a 5V supply. With supplies higher than 5V, the output should never be set to exceed $V_{CC} - 12V$.

Note 6: For output voltages below $-4.5V$ the LTC1261 may reach 50% duty cycle and fall out of regulation with heavy load or low input voltages. Beyond this point, the output will follow the input with no regulation.

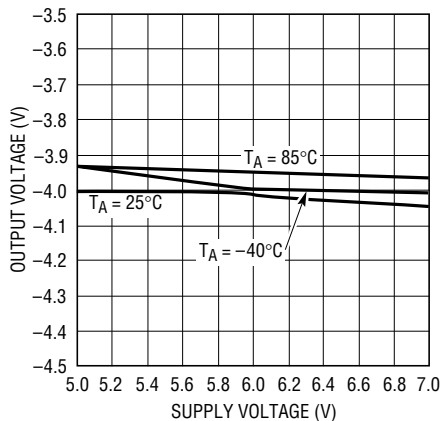
Note 7: C grade device specifications are guaranteed over the $0^\circ C$ to $70^\circ C$ temperature range. In addition, C grade device specifications are assured over the $-40^\circ C$ to $85^\circ C$ temperature range by design or correlation, but are not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS (See Test Circuits)

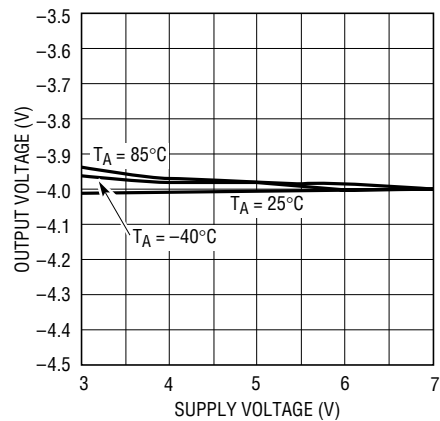
Output Voltage vs Output Current



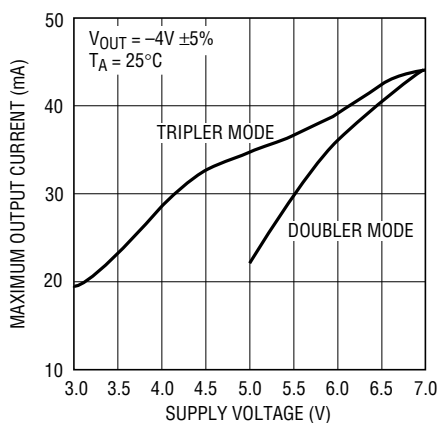
Output Voltage (Doubler Mode) vs Supply Voltage



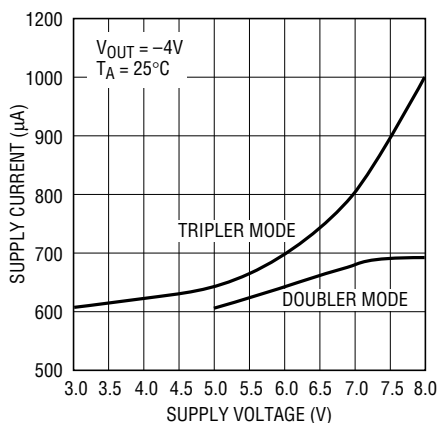
Output Voltage (Tripler Mode) vs Supply Voltage



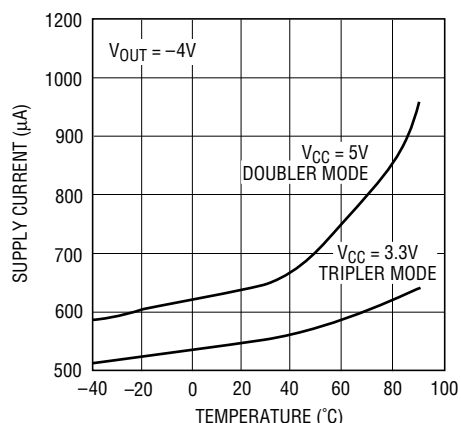
Maximum Output Current vs Supply Voltage



Supply Current vs Supply Voltage

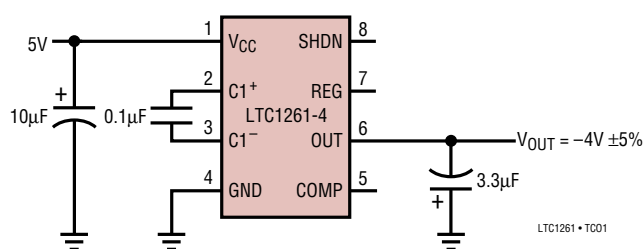


Supply Current vs Temperature

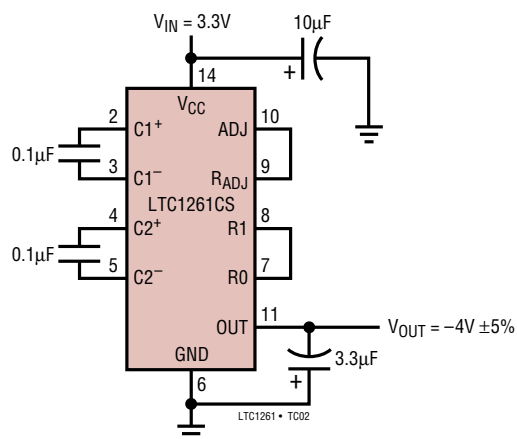


TEST CIRCUITS

Doubler Mode



Tripler Mode



PIN FUNCTIONS

Pin numbers are shown as (LTC1261CS/LTC1261CS8).

NC (Pin 1/NA): No Internal Connection.

C1⁺ (Pin 2/Pin 2): C1 Positive Input. Connect a 0.1 μ F capacitor between C1⁺ and C1⁻. With the LTC1261CS in doubler mode, connect a 0.1 μ F capacitor from C1⁺ to C2⁻.

C1⁻ (Pin 3/Pin 3): C1 Negative Input. Connect a 0.1 μ F capacitor from C1⁺ to C1⁻. With the LTC1261CS in doubler mode only, C1⁻ should float.

C2⁺ (Pin 4/NA): C2 Positive Input. In tripler mode connect a 0.1 μ F capacitor from C2⁺ to C2⁻. This pin is used with the LTC1261CS in tripler mode only; in doubler mode this pin should float.

C2⁻ (Pin 5/NA): C2 Negative Input. In tripler mode connect a 0.1 μ F capacitor from C2⁺ to C2⁻. In doubler mode connect a 0.1 μ F capacitor from C1⁺ to C2⁻.

GND (Pin 6/Pin 4): Ground. Connect to a low impedance ground. A ground plane will help to minimize regulation errors.

R0 (Pin 7/NA): Internal Resistor String, 1st Tap. See Table 2 in the Applications Information section for information on internal resistor string pin connections vs output voltage.

R1 (Pin 8/NA): Internal Resistor String, 2nd Tap.

R_{ADJ} (Pin 9/NA): Internal Resistor String Output. Connect this pin to ADJ to use the internal resistor divider. See Table 2 in the Applications Information section for information on internal resistor string pin connections vs output voltage.

ADJ (COMP for fixed versions) (Pin 10/Pin 5): Output Adjust/Compensation Pin. For adjustable parts this pin is used to set the output voltage. The output voltage should be divided down with a resistor divider and fed back to this pin to set the regulated output voltage. The resistor divider can be external or the internal divider string can

be used if it can provide the required output voltage. Typically the resistor string should draw $\geq 10\mu$ A from the output to minimize errors due to the bias current at the adjust pin. Fixed output parts have the internal resistor string connected to this pin inside the package. The pin can be used to trim the output voltage if desired. It can also be used as an optional feedback compensation pin to reduce output ripple on both adjustable and fixed output voltage parts. See Applications Information section for more information on compensation and output ripple.

OUT (Pin 11/Pin 6): Negative Voltage Output. This pin must be bypassed to ground with a 1 μ F or larger capacitor; it must be at least 3.3 μ F to provide specified output ripple. The size of the output capacitor has a strong effect on output ripple. See the Applications Information section for more details.

REG (Pin 12/Pin 7): This is an open drain output that pulls low when the output voltage is within 5% of the set value. It will sink 8mA to ground with a 5V supply. The external circuitry must provide a pull-up or REG will not swing high. The voltage at REG may exceed V_{CC} and can be pulled up to 12V above ground without damage.

SHDN (Pin 13/Pin 8): Shutdown. When this pin is at ground the LTC1261 operates normally. An internal 5 μ A pull-down keeps SHDN low if it is left floating. When SHDN is pulled high, the LTC1261 enters shutdown mode. In shutdown the charge pump stops, the output collapses to 0V and the quiescent current drops to 5 μ A typically.

V_{CC} (Pin 14/Pin 1): Power Supply. This requires an input voltage between 3V and 6.5V. Certain combinations of output voltage and operating mode may place additional restrictions on the input voltage. V_{CC} must be bypassed to ground with at least a 0.1 μ F capacitor placed in close proximity to the chip. See the Applications Information section for details.

APPLICATIONS INFORMATION

MODES OF OPERATION

The LTC1261 uses a charge pump to generate a negative output voltage that can be regulated to a value either higher or lower than the original input voltage. It has two modes of operation: a “doubler” inverting mode, which can provide a negative output equal to or less than the positive power supply and a “tripler” inverting mode, which can provide negative output voltages either larger or smaller in magnitude than the original positive supply. The tripler offers greater versatility and wider input range but requires four external capacitors and a 14-pin package. The doubler offers the SO-8 package and requires only three external capacitors.

Doubler Mode

Doubler mode allows the LTC1261 to generate negative output voltage magnitudes up to that of the supply voltage, creating a voltage between V_{CC} and OUT of up to two times V_S . In doubler mode the LTC1261 uses a single flying capacitor to invert the input supply voltage, and the output voltage is stored on the output bypass capacitor between switch cycles. The LTC1261CS8 is always configured in doubler mode and has only one pair of flying capacitor pins (Figure 1a). The LTC1261CS can be configured in doubler mode by connecting a single flying capacitor between the $C1^+$ and $C2^-$ pins. $C1^-$ and $C2^+$ should be left floating (Figure 1b).

Tripler Mode

The LTC1261CS can be used in a tripler mode which can generate negative output voltages up to twice the supply voltage. The total voltage between the V_{CC} and OUT pins can be up to three times V_S . For example, tripler mode can be used to generate $-5V$ from a single positive $3.3V$ supply. Tripler mode requires two external flying capacitors. The first connects between $C1^+$ and $C1^-$ and the second between $C2^+$ and $C2^-$ (Figure 1c). Because of the relatively high voltages that can be generated in this mode, care must be taken to ensure that the total input-to-output voltage never exceeds $12V$ or the LTC1261 may be damaged. In most applications the output voltage will be kept in check by the regulation loop. Damage is possible

however, with supply voltages above $4V$ in tripler mode and above $6V$ in doubler mode. As the input supply voltage rises the allowable output voltage drops, finally reaching $-4V$ with an $8.5V$ supply. To avoid this problem use doubler mode whenever possible with high input supply voltages.

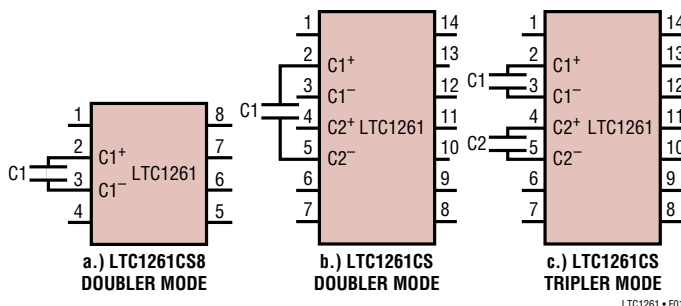


Figure 1. Flying Capacitor Connections

THEORY OF OPERATION

A block diagram of the LTC1261 is shown in Figure 2. The heart of the LTC1261 is the charge pump core shown in the dashed box. It generates a negative output voltage by first charging the flying capacitors between V_{CC} and ground. It then stacks the flying capacitors on top of each other and connects the top of the stack to ground forcing the bottom of the stack to a negative voltage. The charge on the flying capacitors is transferred to the output bypass capacitor, leaving it charged to the negative output voltage. This process is driven by the internal clock.

Figure 2 shows the charge pump configured in tripler mode. With the clock low, $C1$ and $C2$ are charged to V_{CC} by $S1$, $S3$, $S5$ and $S7$. At the next rising clock edge, $S1$, $S3$, $S5$ and $S7$ open and $S2$, $S4$ and $S6$ close, stacking $C1$ and $C2$ on top of each other. $S2$ connects $C1^+$ to ground, $S4$ connects $C1^-$ to $C2^+$ and $C2^-$ is connected to the output by $S6$. The charge in $C1$ and $C2$ is transferred to C_{OUT} , setting it to a negative voltage. Doubler mode works the same way except that the single flying capacitor ($C1$) is connected between $C1^+$ and $C2^-$. $S3$, $S4$ and $S5$ don't do anything useful in doubler mode. $C1$ is charged initially by $S1$ and $S7$ and connected to the output by $S2$ and $S6$.

APPLICATIONS INFORMATION

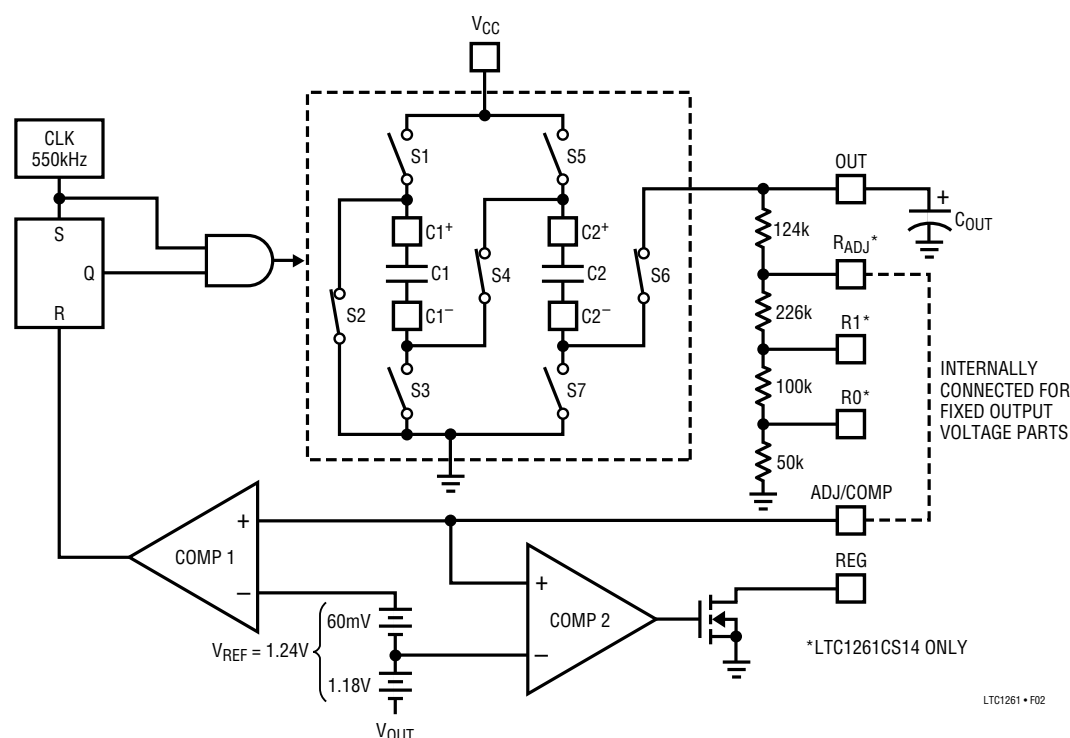


Figure 2. Block Diagram

The output voltage is monitored by COMP1 which compares a divided replica of the output at ADJ (COMP for fixed output parts) to the internal reference. At the beginning of a cycle the clock is low, forcing the output of the AND gate low and charging the flying capacitors. The next rising clock edge sets the RS latch, setting the charge pump to transfer charge from the flying capacitors to the output capacitor. As long as the output is below the set point, COMP1 stays low, the latch stays set and the charge pump runs at the full 50% duty cycle of the clock gated through the AND gate. As the output approaches the set voltage, COMP1 will trip whenever the divided signal exceeds the internal 1.24V reference relative to OUT. This resets the RS latch and truncates the clock pulses, reducing the amount of charge transferred to the output capacitor and regulating the output voltage. If the output exceeds the set point, COMP1 stays high, inhibiting the RS latch and disabling the charge pump.

COMP2 also monitors the divided signal at ADJ but it is connected to a 1.18V reference, 5% below the main reference voltage. When the divided output exceeds this lower reference voltage indicating that the output is within 5% of the set value, COMP2 goes high turning on the REG output transistor. This is an open drain N-channel device capable of sinking 5mA with a 3.3V V_{CC} and 8mA with a 5V V_{CC} . When in the "off" state (divided output more than 5% below V_{REF}) the drain can be pulled above V_{CC} without damage up to a maximum of 12V above ground. Note that the REG output only indicates if the magnitude of the output is *below* the magnitude of the set point by 5% (i.e., $V_{OUT} > -4.75V$ for a $-5V$ set point). If the magnitude of the output is forced *higher* than the magnitude of the set point (i.e., to $-6V$ when the output is set for $-5V$) the REG output will stay low.

APPLICATIONS INFORMATION

OUTPUT RIPPLE

Output ripple in the LTC1261 comes from two sources; voltage droop at the output capacitor between clocks and frequency response of the regulation loop. Voltage droop is easy to calculate. With a typical clock frequency of 550kHz, the charge on the output capacitor is refreshed once every 1.8μs. With a 15mA load and a 3.3μF output capacitor, the output will droop by:

$$I_{\text{LOAD}} \times \left(\frac{\Delta t}{C_{\text{OUT}}} \right) = 15\text{mA} \times \left(\frac{1.8\mu\text{s}}{3.3\mu\text{F}} \right) = 8.2\text{mV}$$

This can be a significant ripple component when the output is heavily loaded, especially if the output capacitor is small. If absolute minimum output ripple is required, a 10μF or greater output capacitor should be used.

Regulation loop frequency response is the other major contributor to output ripple. The LTC1261 regulates the output voltage by limiting the amount of charge transferred to the output capacitor on a cycle-by-cycle basis. The output voltage is sensed at the ADJ pin (COMP for fixed output versions) through an internal or external resistor divider from the OUT pin to ground. As the flying capacitors are first connected to the output, the output voltage begins to change quite rapidly. As soon as it exceeds the set point COMP1 trips, switching the state of the charge pump and stopping the charge transfer. Because the RC time constant of the capacitors and the switches is quite short, the ADJ pin must have a wide AC bandwidth to be able to respond to the output in time. External parasitic capacitance at the ADJ pin can reduce the bandwidth to the point where the comparator cannot respond by the time the clock pulse finishes. When this happens the comparator will allow a few complete pulses through, then overcorrect and disable the charge pump until the output drops below the set point. Under these conditions the output will remain in regulation but the output ripple will increase as the comparator “hunts” for the correct value.

To prevent this from happening, an external capacitor can be connected from ADJ (or COMP for fixed output parts) to ground to compensate for external parasitics and increase the regulation loop bandwidth (Figure 3). This sounds counterintuitive until we remember that the internal reference is generated with respect to OUT, not ground.

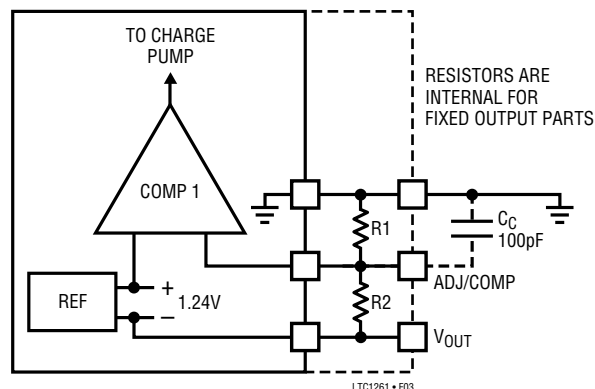


Figure 3. Regulator Loop Compensation

The feedback loop actually sees ground as its “output,” thus the compensation capacitor should be connected across the “top” of the resistor divider, from ADJ (or COMP) to ground. By the same token, avoid adding capacitance between ADJ (or COMP) and V_{OUT}. This will slow down the feedback loop and increase output ripple. A 100pF capacitor from ADJ or COMP to ground will compensate the loop properly under most conditions.

OUTPUT FILTERING

If extremely low output ripple (<5mV) is required, additional output filtering is required. Because the LTC1261 uses a high 550kHz switching frequency, fairly low value RC or LC networks can be used at the output to effectively filter the output ripple. A 10Ω series output resistor and a 3.3μF capacitor will cut output ripple to below 3mV (Figure 4). Further reductions can be obtained with larger filter capacitors or by using an LC output filter.

APPLICATIONS INFORMATION

pump from going into very high frequency oscillation under such conditions but it also creates an output error as the feedback loop regulates based on the top of the spike, not the average value of the output (Figure 5). The resulting output voltage behaves as if a resistor of value $C_{ESR} \times (I_{PK}/I_{AVE})\Omega$ was placed in series with the output. To avoid this nasty sequence of events connect a $0.1\mu\text{F}$ ceramic capacitor in parallel with the larger output capacitor. The ceramic capacitor will “eat” the high frequency spike, preventing it from fooling the feedback loop, while the larger but slower tantalum or aluminum output capacitor supplies output current to the load between charge cycles.

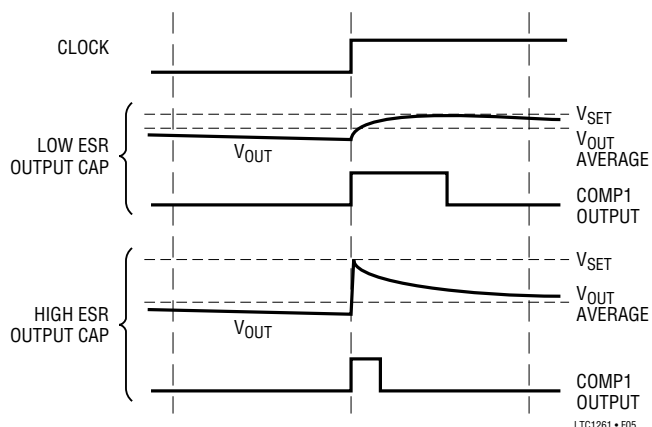


Figure 5. Output Ripple with Low and High ESR Capacitors

Note that ESR in the flying capacitors will not cause the same condition; in fact, it may actually improve the situation by cutting the peak current and lowering the amplitude of the spike. However, more flying capacitor ESR is not necessarily better. As soon as the RC time constant approaches half of a clock period (the time the capacitors have to share charge at full duty cycle) the output current capability of the LTC1261 will begin to diminish. For $0.1\mu\text{F}$ flying capacitors, this gives a maximum total series resistance of:

$$\frac{1}{2} \left(\frac{t_{CLK}}{C_{FLY}} \right) = \frac{1}{2} \left(\frac{1}{550\text{kHz}} \right) / 0.1\mu\text{F} = 9.1\Omega$$

Most of this resistance is already provided by the internal switches in the LTC1261 (especially in tripler mode). More than 1Ω or 2Ω of ESR on the flying capacitors will start to affect the regulation at maximum load.

RESISTOR SELECTION

Resistor selection is easy with the fixed output versions of the LTC1261—no resistors are needed! Selecting the right resistors for the adjustable parts is only a little more difficult. A resistor divider should be used to divide the signal at the output to give 1.24V at the ADJ pin *with respect to V_{OUT}* (Figure 6). The LTC1261 uses a positive reference with respect to V_{OUT} , not a negative reference with respect to ground (Figure 2 shows the reference connection). Be sure to keep this in mind when connecting the resistors! If the initial output is not what you expected, try swapping the two resistors.

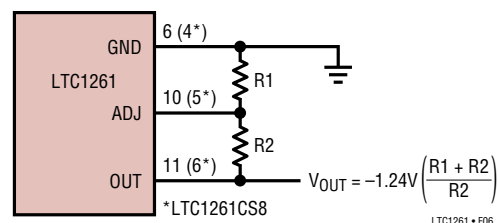


Figure 6. External Resistor Connections

The 14-pin adjustable parts include a built-in resistor string which can provide an assortment of output voltages by using different pin-strapping options at the R0, R1, and R_{ADJ} pins (Table 2). The internal resistors are roughly 124k , 226k , 100k , and 50k (see Figure 2) giving output options of -3.5V , -4V , -4.5V , and -5V . The resistors are carefully matched to provide accurate divider ratios, but the absolute values can vary substantially from part to part. It is not a good idea to create a divider using an external resistor and one of the internal resistors unless the output voltage accuracy is not critical.

APPLICATIONS INFORMATION

Table 2. Output Voltages Using the Internal Resistor Divider

PIN CONNECTIONS	OUTPUT VOLTAGE
ADJ to R _{ADJ}	-5V
ADJ to R _{ADJ} , R0 to GND	-4.5V
ADJ to R _{ADJ} , R1 to R0	-4V
ADJ to R _{ADJ} , R1 to GND	-3.5V
ADJ to R1	-1.77V
ADJ to R0	-1.38V
ADJ to GND	-1.24V

There are some oddball output voltages available by connecting ADJ to R0 or R1 and shorting out some of the internal resistors. If one of these combinations gives you the output voltage you want, by all means use it!

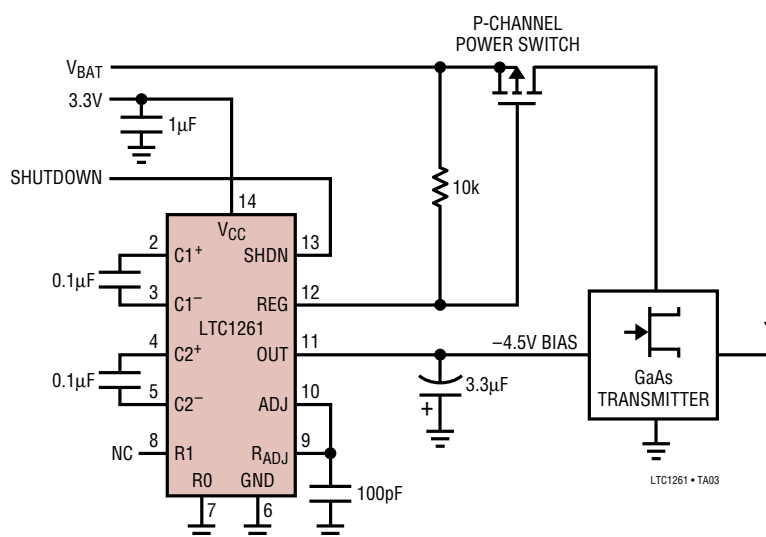
The internal resistor values are the same for the fixed output versions of the LTC1261 as they are for the adjust-

able. The output voltage can be trimmed, if desired, by connecting external resistance from the COMP pin to OUT or ground to alter the divider ratio. As in the adjustable parts, the absolute value of the internal resistors may vary significantly from unit to unit. As a result, the further the trim shifts the output voltage the less accurate the output voltage will be. If a precise output voltage other than one of the available fixed voltages is required, it is better to use an adjustable LTC1261 and use precision external resistors. The internal reference is trimmed at the factory to within 3.5% of 1.24V; with 1% external resistors the output will be within 5.5% of the nominal value, even under worst case conditions.

The LTC1261 can be internally configured with nonstandard fixed output voltages. Contact the Linear Technology Marketing Department for details.

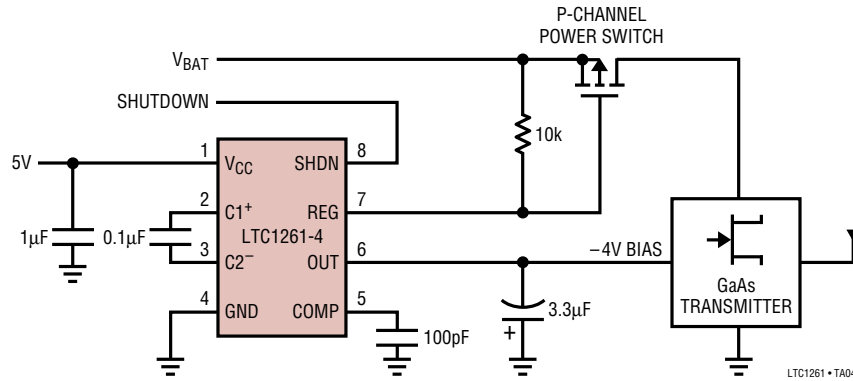
TYPICAL APPLICATIONS

3.3V Input, -4.5V Output GaAs FET Bias Generator

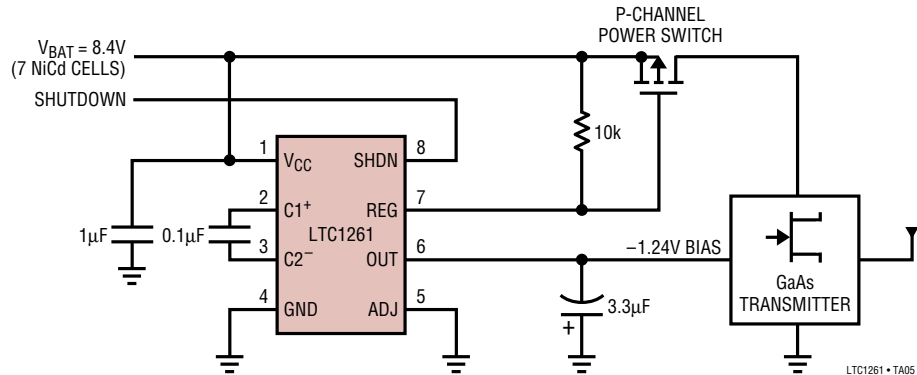


TYPICAL APPLICATIONS

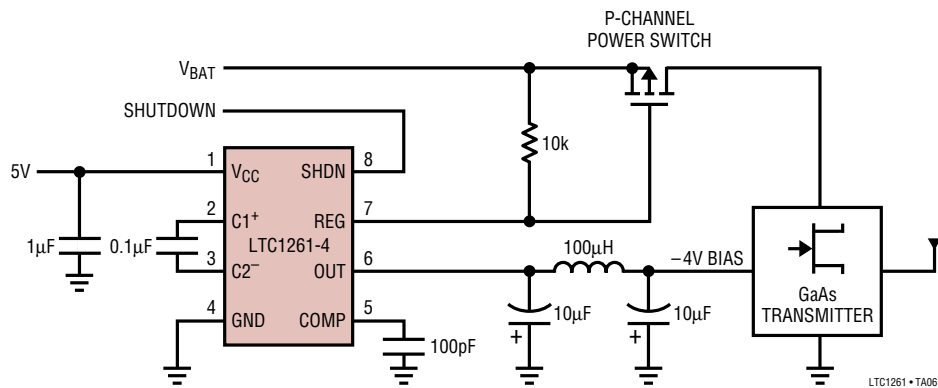
5V Input, -4V Output GaAs FET Bias Generator



7 Cells to -1.24V Output GaAs FET Bias Generator

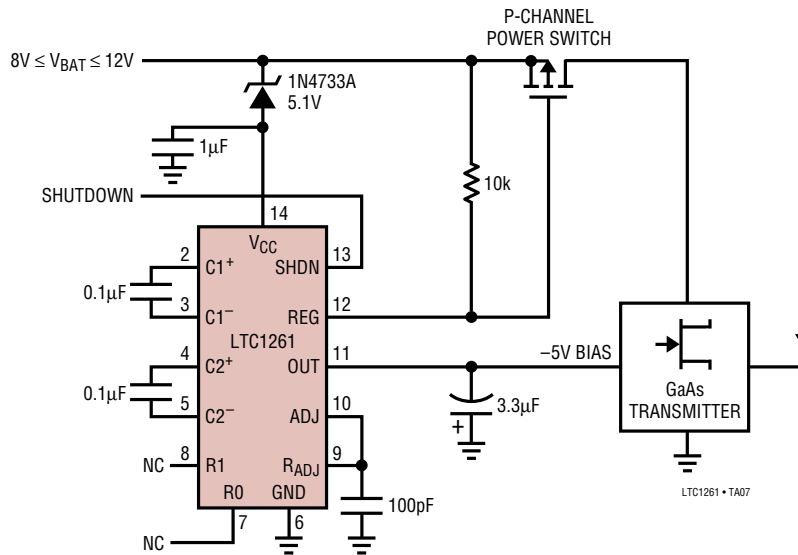


1mV Ripple, 5V Input, -4V Output GaAs FET Bias Generator

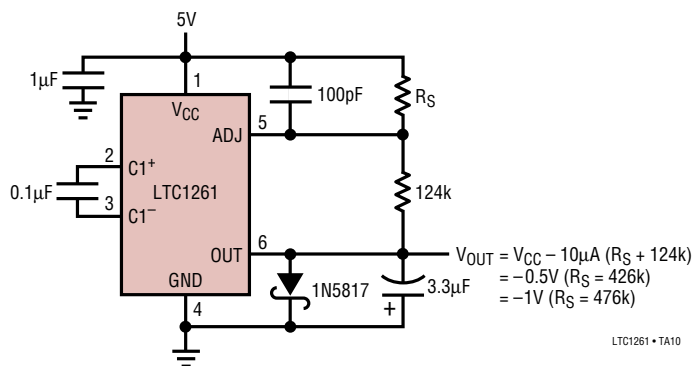


TYPICAL APPLICATIONS

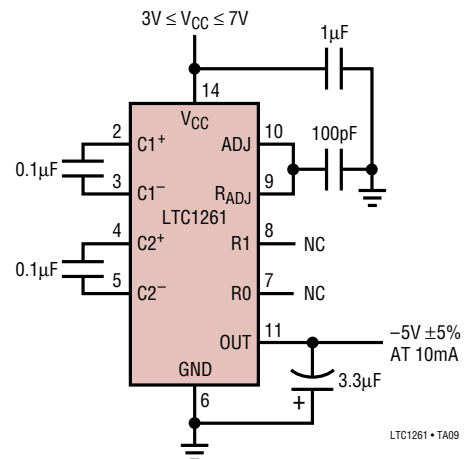
High Supply Voltage, -5V Output GaAs FET Bias Generator



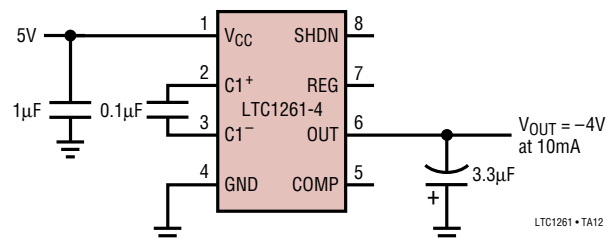
Low Output Voltage Generator



-5V Supply Generator



Minimum Parts Count -4V Generator

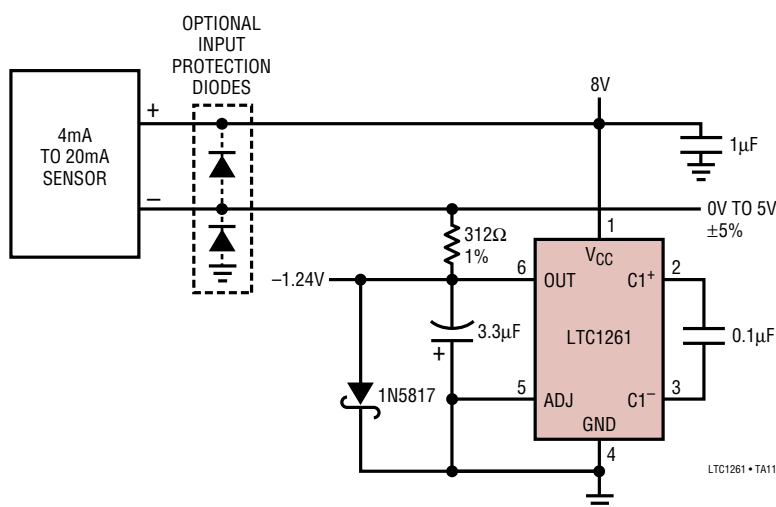


TYPICAL APPLICATIONS

This circuit uses the LTC1261CS8 to generate a -1.24V output at 20mA . Attached to this output is a 312Ω resistor to make the current/voltage conversion. 4mA through 312Ω generates 1.24V , giving a net 0V output. 20mA through 312Ω gives 6.24V across the resistor, giving a net 5V output. If the 4mA to 20mA source requires an operating voltage greater than 8V , it should be powered from a

separate supply; the LTC1261 can then be powered from any convenient supply, $3\text{V} \leq V_S \leq 8\text{V}$. The Schottky diode prevents the external voltage from damaging the LTC1261 in shutdown or under fault conditions. The LTC1261's reference is trimmed to 3.5% and the resistor adds 1% uncertainty, giving 4.5% total output error.

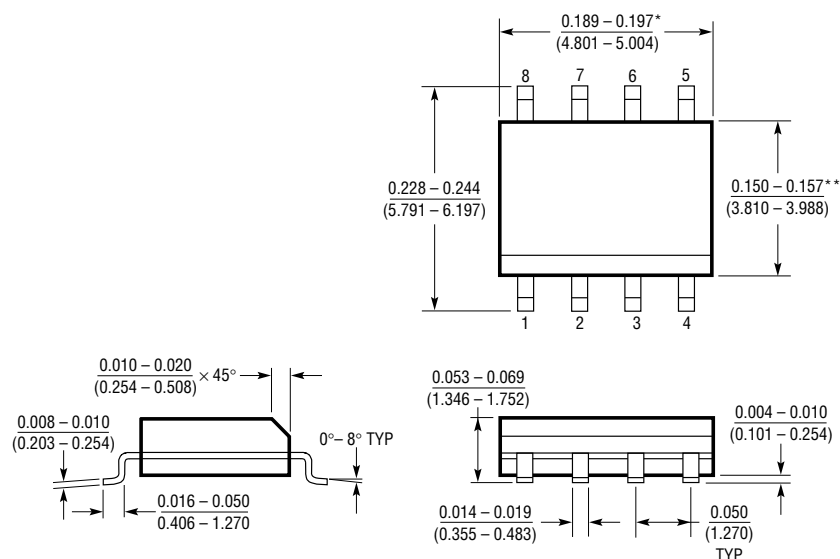
-1.24V Generator for 4mA - 20mA to 0V - 5V Conversion



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)

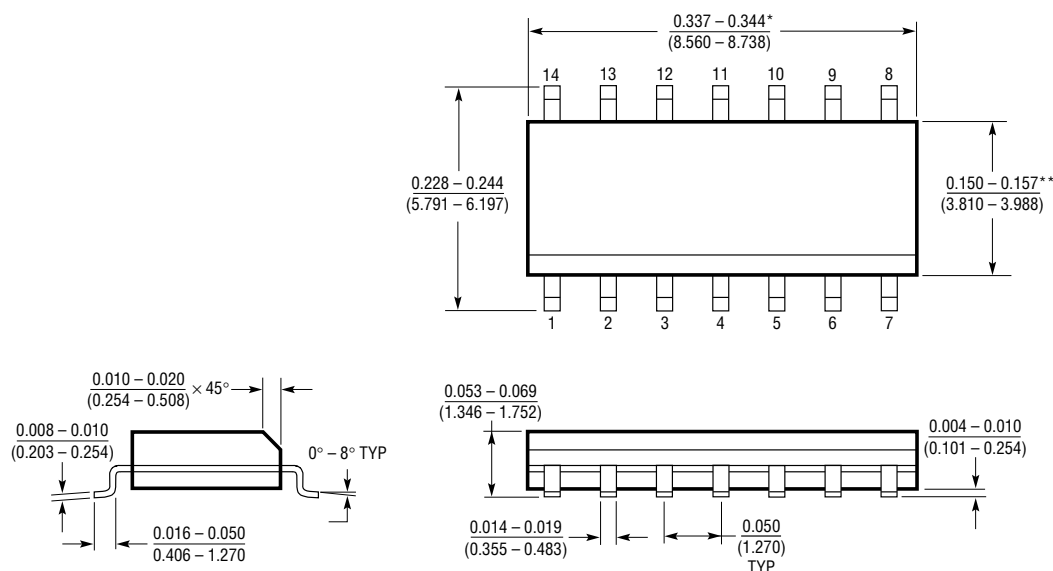


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

S Package 14-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



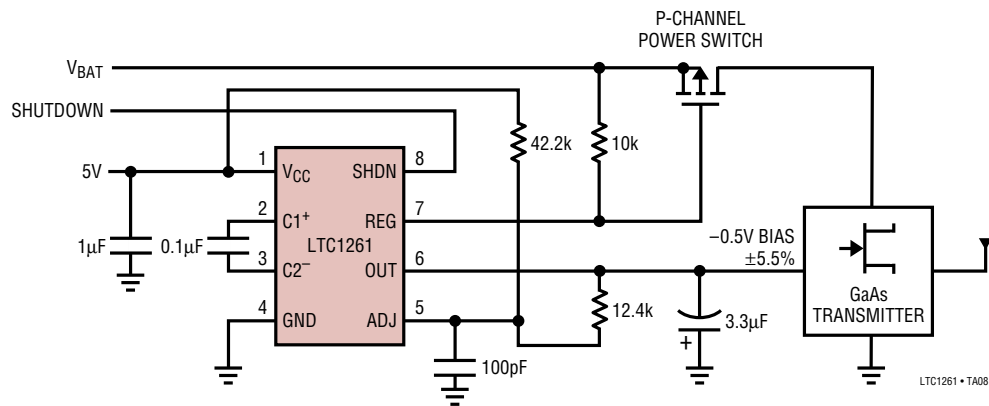
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S14 0695

TYPICAL APPLICATION

5V Input, -0.5V Output GaAs FET Bias Generator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1550/LTC1551	Low Noise Switched Capacitor Regulated Voltage Inverter	GaAs FET Bias with Linear Regulator 1mV Ripple
LTC1429	Clock Synchronized Switched Capacitor Regulated Voltage Inverter	GaAs FET Bias
LT1121	Micropower Low Dropout Regulators with Shutdown	0.4V Dropout Voltage at 150mA, Low Noise, Switched Capacitor Regulated Voltage Inverter