

LTC1100

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range

LTC1100M/AM (OBSOLETE) –55°C to 125°C

LTC1100C –40°C to 85°C

Output Short Circuit Duration Indefinite

Storage Temperature Range –65°C to 150°C

Total Supply Voltage (V^+ to V^-) 18V

Input Voltage ($V^+ + 0.3V$) to ($V^- - 0.3V$)

Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 110^\circ\text{C}$, $\theta_{JA} = 130^\circ\text{C/W}$ J PACKAGE 8-LEAD CERDIP $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 100^\circ\text{C/W}$ OBSOLETE PACKAGE Consider the N Package for an Alternate Source	ORDER PART NUMBER LTC1100CN8 LTC1100CJ8 LTC1100AMJ8 LTC1100MJ8	TOP VIEW SW PACKAGE 16-LEAD PLASTIC SO WIDE $T_{JMAX} = 110^\circ\text{C}$, $\theta_{JA} = 100^\circ\text{C/W}$	ORDER PART NUMBER LTC1100CSW
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Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 5V$, $R_L = 10k$, $C_C = 1000pF$, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1100ACN			LTC1100CN/CJ			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Gain Error		●		0.01	0.05 0.10		0.01	0.075 0.150	±% ±%
Gain Nonlinearity		●		3 12	8 30		3 12	20 60	ppm ppm
Input Offset Voltage	(Note 2)			±1	±10		±1	±10	μV
Input Offset Voltage Drift	(Note 2)	●		±5	±100		±5	±100	nV/°C
Input Noise Voltage	DC to 10Hz, $T_A = 25^\circ\text{C}$			1.9			1.9		μV _{p-p}
Input Bias Current		●		2.5	50 120		2.5	65 135	pA pA
Input Offset Current		●		10	50		10	65	pA
Common Mode Rejection Ratio	$V_{CM} = 2.3V$ to $-4.7V$ (Note 3)	●	104	115		90	110		dB
Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 8V$	●	120			105			dB
Output Voltage Swing	$R_L = 2k$, $V_S = \pm 8V$	●	–7.2		6.2	–7.2		6.2	V
	$R_L = 10k$, $V_S = \pm 8V$	●	–7.7		7.5	–7.7		7.5	V
Supply Current		●		2.4 3.4	2.8 4.0		2.4 3.4	3.3 4.5	mA mA
Internal Sampling Frequency				2.8			2.8		kHz
Bandwidth				18			18		kHz

1100fc

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		LTC1100AMJ (Note 4)			LTC1100MJ			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Gain Error		●		0.01	0.05 0.11		0.01	0.075 0.150	$\pm\%$ $\pm\%$
Gain Nonlinearity		●		3	8 40		3	20 65	ppm ppm
Input Offset Voltage	(Note 2)			± 1	± 10		± 1	± 10	μV
Input Offset Voltage Drift	(Note 2)	●		± 5	± 100		± 5	± 100	$\text{nV}/^\circ\text{C}$
Input Noise Voltage	DC to 10Hz, $T_A = 25^\circ\text{C}$			1.9			1.9		$\mu\text{V}_{\text{P-P}}$
Input Bias Current		●		5	50 300		5	65 450	pA pA
Input Offset Current		●			80			120	pA
Common Mode Rejection Ratio	$V_{\text{CM}} = -4.7\text{V}$ to 2.3V	●	100			90			dB
Power Supply Rejection Ratio	$V_S = \pm 2.375\text{V}$ to $\pm 8\text{V}$	●	115			95			dB
Output Voltage Swing	$R_L = 10\text{k}$, $V_S = \pm 8\text{V}$	●	-7.4		7.4	-7.4		7.4	V
	$R_L = 2\text{k}$, $V_S = \pm 8\text{V}$	●	-7.0		6.0	-7.0		6.0	V
Supply Current		●		2.4			2.4	3.3	mA
					4.2			4.6	mA
Internal Sampling Frequency				2.8			2.8		kHz
Bandwidth				18			18		kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 5\text{V}$, $R_L = 10\text{k}$, $C_C = 1000\text{pF}$, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1100ACS			LTC1100CSW			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Gain Error	$T_A = 25^\circ\text{C}$, $A_V = 100$	●		0.01	0.05		0.01	0.075	$\pm\%$
	$A_V = 100$				0.10			0.150	$\pm\%$
	$A_V = 10$	●		0.01	0.04		0.01	0.060	$\pm\%$
	$A_V = 10$	●			0.10			0.150	$\pm\%$
Gain Nonlinearity	$T_A = 25^\circ\text{C}$, $A_V = 100$	●		3	8		3	20	ppm
	$A_V = 100$			12	30		12	60	ppm
	$A_V = 10$	●		1	8		1	10	ppm
	$A_V = 10$	●			25			40	ppm
Input Offset Voltage	(Note 2)			± 1	± 10		± 1	± 10	μV
Input Offset Voltage Drift	(Note 2)	●		± 5	± 100		± 5	± 100	$\text{nV}/^\circ\text{C}$
Input Noise Voltage	DC to 10Hz, $T_A = 25^\circ\text{C}$			1.9			1.9		$\mu\text{V}_{\text{P-P}}$
Input Bias Current		●		2.5	50 120		2.5	65 135	pA pA
Input Offset Current		●		10	50		10	65	pA
Common Mode Rejection Ratio	$V_{\text{CM}} = -4.7\text{V}$ to 2.3V , $A_V = 100$	●	104	115		90	110		dB
	$A_V = 10$	●	95			85			dB
Power Supply Rejection Ratio	$V_S = \pm 2.375\text{V}$ to $\pm 8\text{V}$	●	120			105			dB

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 5\text{V}$, $R_L = 10\text{k}$, $C_C = 1000\text{pF}$, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1100ACS			LTC1100CSW			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Swing	$R_L = 10\text{k}$, $V_S = \pm 8\text{V}$ $R_L = 2\text{k}$, $V_S = \pm 8\text{V}$	●	-7.2		6.2	-7.2		6.2	V
		●	-7.7		7.5	-7.7		7.5	V
Supply Current		●		2.4	2.8		2.4	3.3	mA
				3.4	4.0		3.4	4.5	mA
Internal Sampling Frequency				2.8			2.8		kHz
Bandwidth	$G = 100$			18			18		kHz
	$G = 10$			180			180		kHz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

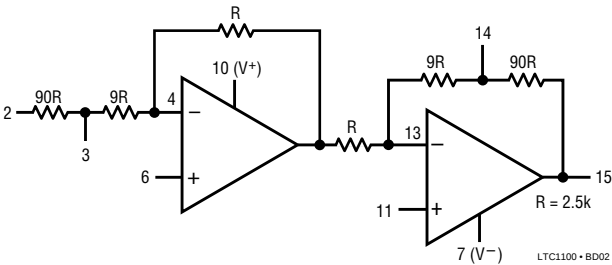
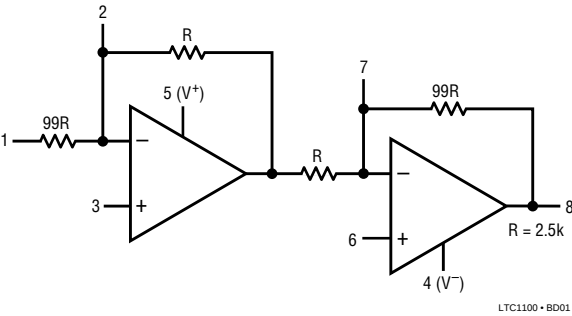
Note 2: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test

systems. V_{OS} is measured to a limit determined by test equipment capability.

Note 3: See Applications Information, Single Supply Operation.

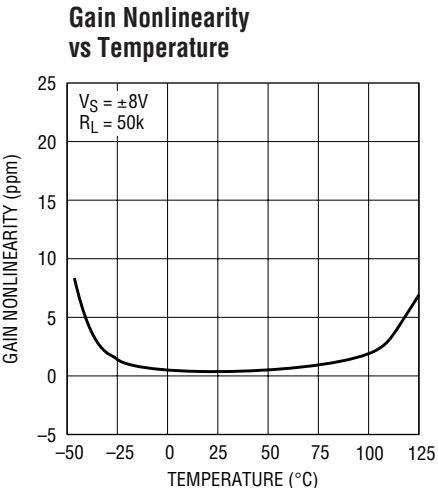
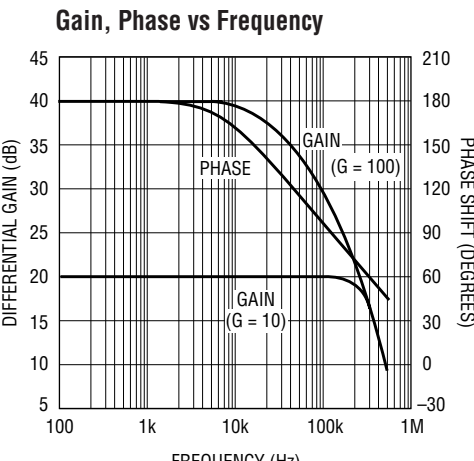
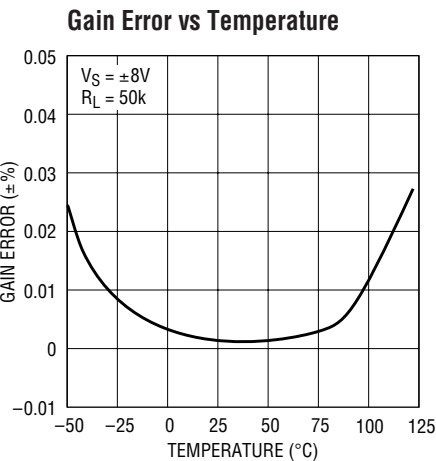
Note 4: Please consult Linear Technology Marketing.

BLOCK DIAGRAMS



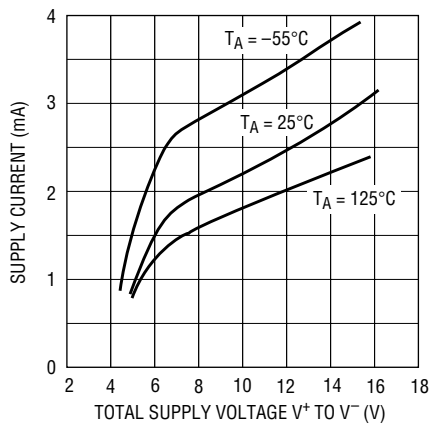
NOTE: FOR A VOLTAGE GAIN OF 10V/V SHORT PIN 2 TO 3, AND PIN 14 TO 15.

TYPICAL PERFORMANCE CHARACTERISTICS



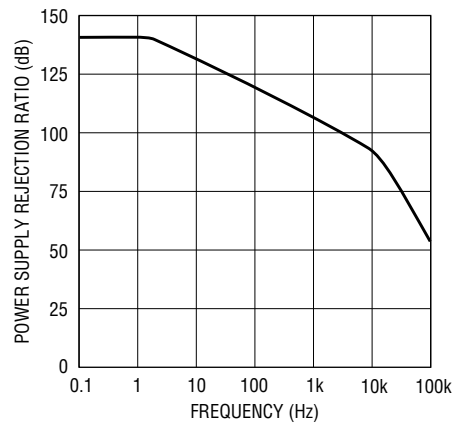
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



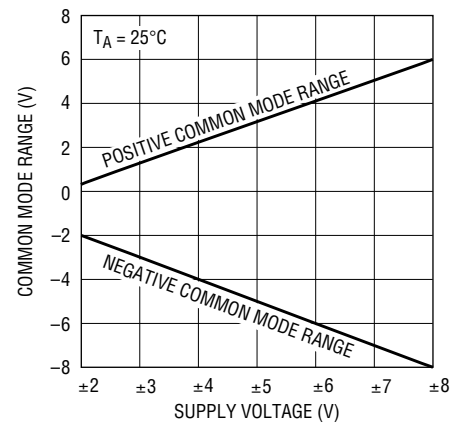
LTC1100 • TPC04

Power Supply Rejection Ratio vs Frequency



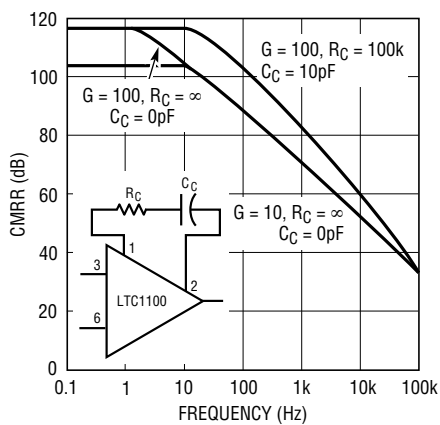
LTC1100 • TPC05

Common Mode Range vs Supply Voltage



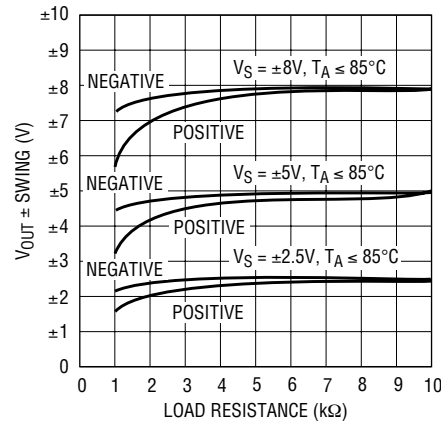
LTC1100 • TPC06

CMRR vs Frequency



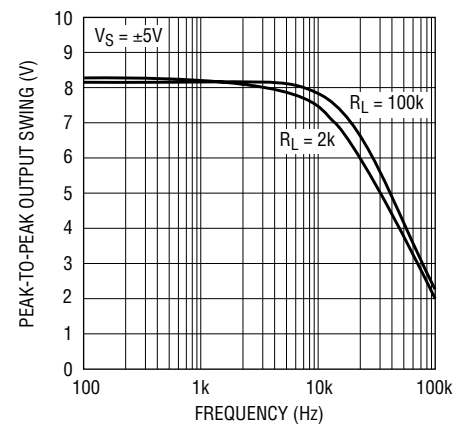
LTC1100 • TPC07

Output Voltage Swing vs Load



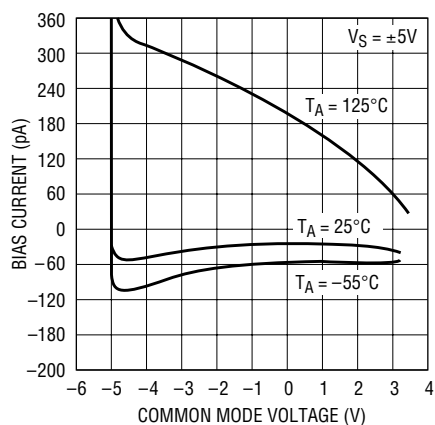
LTC1100 • TPC08

Undistorted Output Swing vs Frequency



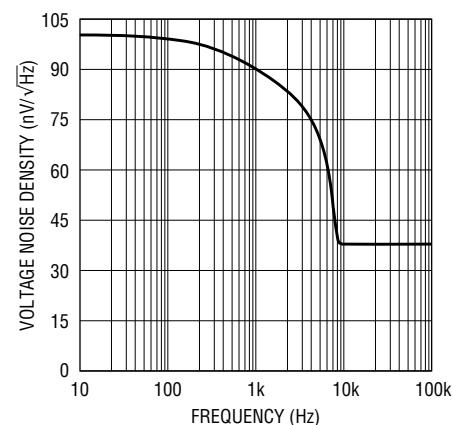
LTC1100 • TPC09

Bias Current vs Common Mode Voltage



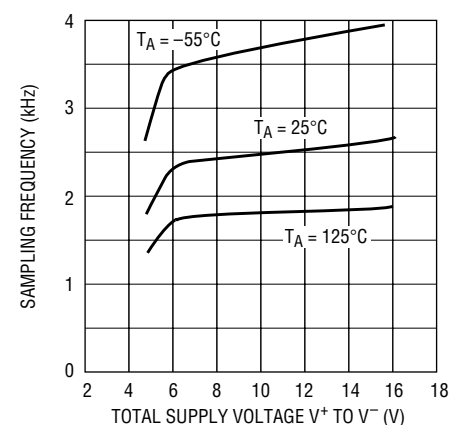
LTC1100 • TPC10

Voltage Noise vs Frequency



LTC1100 • TPC11

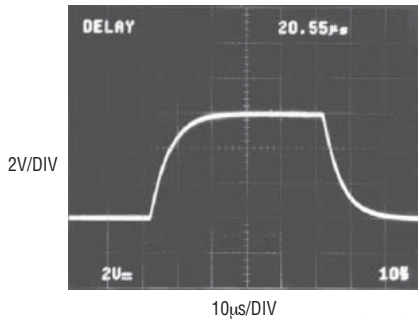
Internal Sampling Frequency vs Supply Voltage



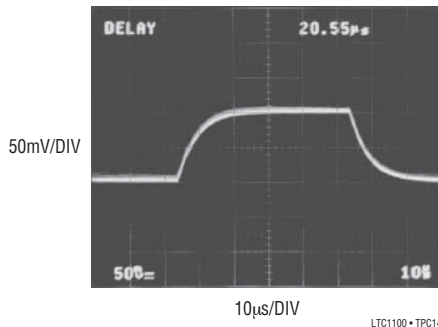
LTC1100 • TPC12

TYPICAL PERFORMANCE CHARACTERISTICS

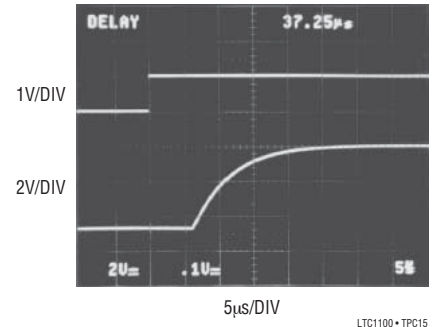
Large-Signal Transient Response
 $G = 100$, $V_S = \pm 5V$



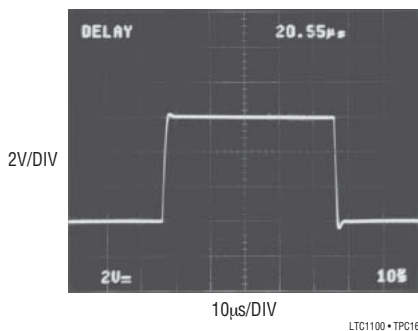
Small-Signal Transient Response
 $G = 100$, $V_S = \pm 5V$



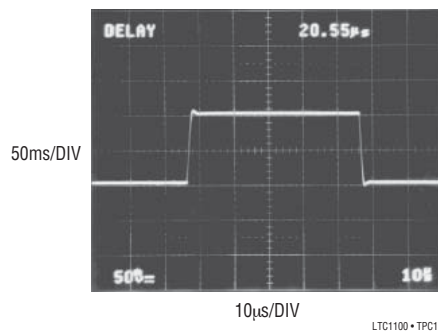
Overload Recovery
 $G = 100$, $V_S = \pm 5V$



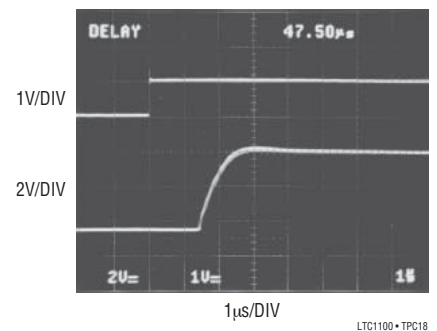
Large-Signal Transient Response
 $G = 10$ (LTC1100CS Only), $V_S = \pm 5V$



Small-Signal Transient Response
 $G = 10$ (LTC1100CS Only), $V_S = \pm 5V$



Overload Recovery
 $G = 10$ (LTC1100CS Only), $V_S = \pm 5V$



PIN FUNCTIONS

8-Pin DIP (16-Pin SO)

Pin 1 (2) GND REF: Connect to system ground. This sets the zero reference for the internal op amps.

Pin 2 (4) CMRR: This pin tailors the gain of the internal amplifiers to maximize AC CMRR. For applications which emphasize CMRR requirements, connect a 100k resistor and a 10pF capacitor in series from CMRR to ground. See the Applications section.

Pin 3 (6) $-V_{IN}$: Inverting Input.

Pin 4 (7) V^- : Negative Supply.

Pin 5 (10) V^+ : Positive Supply.

Pin 6 (11) V_{IN} : Noninverting Input.

Pin 7 (13) COMP: This pin reduces the bandwidth of the internal amplifiers for applications at or near DC. Clock feedthrough from the internal sampling clock can also be

suppressed by using the COMP pin. The standard compensation circuit is a capacitor from COMP to V_{OUT} , sized to provide an RC pole with the internal 247k resistor (22.5k for LTC1100CS in gain-of-10 mode). See the Applications section.

Pin 8 (15) V_{OUT} : Signal Output.

16-Pin SO Package Only

(3) $G = 10$: Short to pin (2) for gain of 10. Leave disconnected for gain of 100.

(14) $G = 10$: Short to pin (15) for gain of 10. Leave disconnected for gain of 100.

NOTE: Both pins must be shorted or open to provide correct gain.

(1),(5),(8),(9),(12),(16) NC: No Internal Connection.

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APPLICATIONS INFORMATION

Common Mode Rejection

Due to very precise matching of the internal resistors, no trims are required to obtain a DC CMRR of better than 100dB; however, things change as frequency rises. The inverting amplifier is in a gain of 1.01 (1.1 for gain of 10), while the noninverting amplifier is in a gain of 99 (9 for gain of 10). As frequency rises, the higher gain amplifier hits its gain-bandwidth limit long before the low gain amplifier, degrading CMRR. The solution is straightforward—slow down the inverting amplifier to match the noninverting amp. Figure 1 shows the recommended circuit. The problem is less pronounced in the LTC1100CS in gain-of-10 mode; no CMRR trims are necessary.

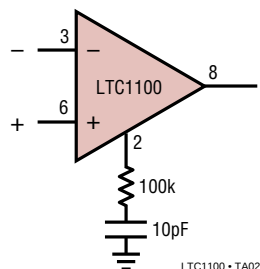


Figure 1. Improving AC CMRR

Overcompensation

Many instrumentation amplifier applications process DC or low frequency signals only; consequently, the 18kHz (180kHz for $G = 10$) bandwidth of the LTC1100 can be reduced to minimize system errors or reduce transmitted clock noise by using the COMP pin. A feedback cap from COMP to V_{OUT} will react with the 247k internal resistor (22.5k for $G = 10$) to limit the bandwidth, as in Figure 2.

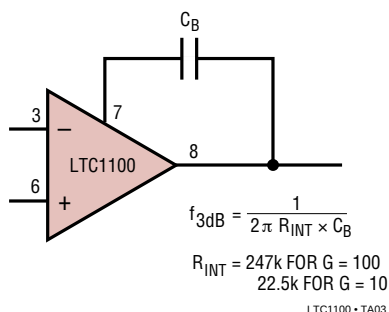


Figure 2. Overcompensation to Reduce System Bandwidth

Aliasing

The LTC1100 is a chopper-stabilized instrumentation amplifier; like all sampled systems it exhibits aliasing behavior for input frequencies at or near the internal sampling frequency. The LTC1100 incorporates specialized anti-aliasing circuitry which typically attenuates aliasing products by ≥ 60 dB; however, extremely sensitive systems may still have to take precautions to avoid aliasing errors. For more information, see the LTC1051/LTC1053 data sheet.

Single Supply Operation

The LTC1100 will operate on a single 5V supply, and the common mode range of the internal op amps includes ground; single supply operation is limited only by the output swing of the op amps. The internal inverting amplifier has a negative saturation limit of 5mV typically, setting the minimum common mode limit at 5mV/1.01 (or 1.1 for gain of 10). The inputs can be biased above ground, as shown in Figure 3. Low cost biasing components can be used since any errors appear as a common mode term and are rejected.

The minimum differential input voltage is limited by the swing of the output op amp. Lightly loaded, it will swing down to 5mV, allowing differential input voltages as low as 50 μ V (450 μ V for gain of 10). Single supply operation limits the LTC1100 to positive differential inputs only; negative inputs will give a saturated zero output.

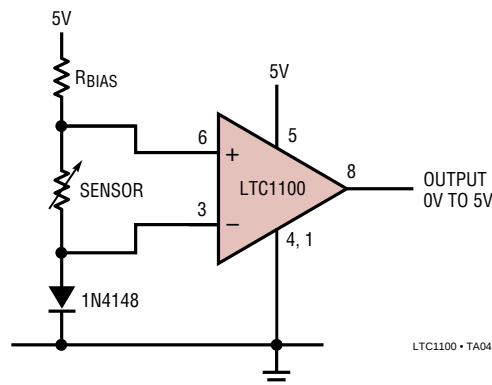
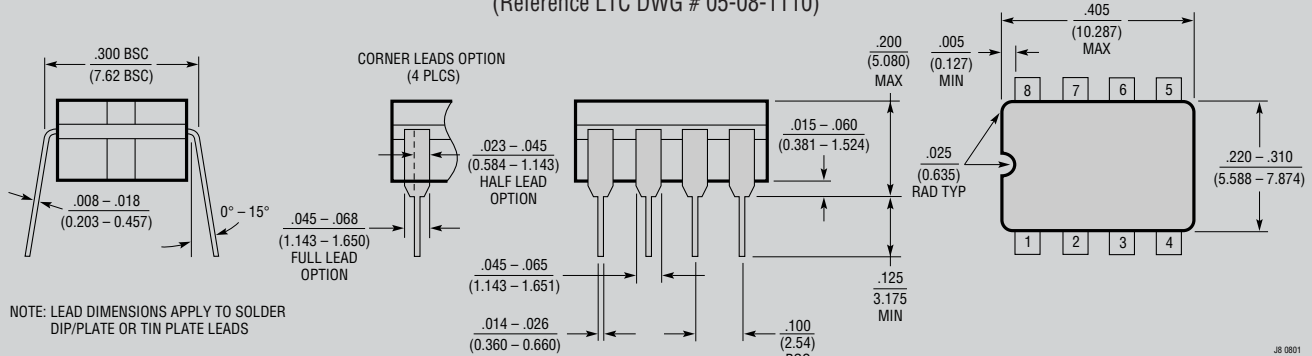


Figure 3

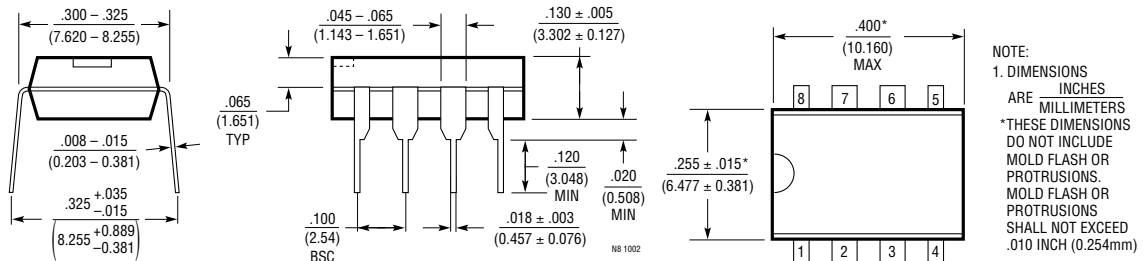
PACKAGE DESCRIPTION

J8 Package 8-Lead Cerdip (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)

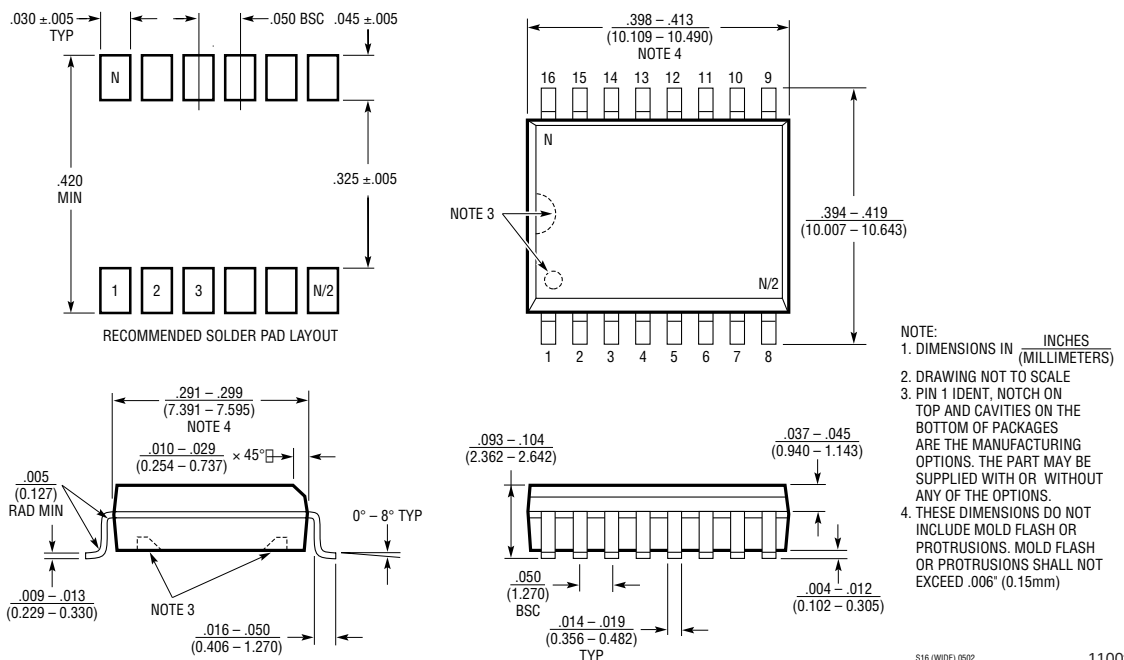


OBsolete PACKAGE

N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



SW Package 16-Lead Plastic Small Outline (Wide .300 Inch) (Reference LTC DWG # 05-08-1620)



S16 (WIDE) 0502

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