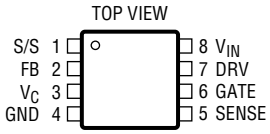
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage (V_{IN}) ..... –0.3V to 20V
Gate Drive Supply Voltage (DRV) ..... –0.3V to 20V
Shutdown/Synch Voltage (S/S) ..... –0.3V to 20V
Feedback Voltage (FB) ..... V_{IN}
Compensation Voltage (V_C) 3V
Gate Drive Output Current (GATE) ..... ±1.5A
Current Sense Voltage (SENSE) .....–0.5V to V_{IN}
Operating Temperature Range (Note 2) .. –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

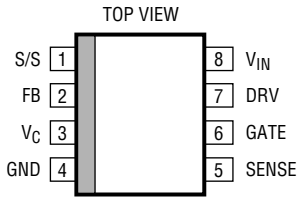
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LT1619EMS8
MS8 PART MARKING
LTHC



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LT1619ES8
S8 PART MARKING
1619

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{DRV} = 2.5V, $V_{S/S}$ = V_{IN}, COMP open, V_{SENSE} = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	Measured at the FB Pin	●	1.22	1.24	1.26	V
Reference Line Regulation	1.9V ≤ V_{IN} ≤ 18V			0.004	0.05	%/V
FB Input Bias Current	V_{FB} = V_{REF}			10	25	nA
Error Amplifier Transconductance			80	170	260	$\mu\Omega^{-1}$
Error Amplifier Output Source Current	V_{FB} = 1V, V_{COMP} = 1V		4	8.7	14	µA
Error Amplifier Output Sink Current	V_{FB} = 1.5V, V_{COMP} = 1V		4	8.7	14	µA
Error Amplifier Clamp Voltage	V_{FB} = 1V		1.6		2.2	V
Undervoltage Lockout Threshold			1.65		1.85	V
Input Voltage Range		●	1.9		18	V
Switching Frequency	1.9V ≤ V_{IN} ≤ 18V	●	220	300	360	kHz
Synchronization Frequency Range			370		500	kHz
Maximum Duty Cycle		●	88	92		%
Current Limit Threshold		●	40	53	66	mV
Burst Mode Operation Current Limit				10		mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{DRV} = 2.5V, $V_{S/S}$ = V_{IN}, COMP open, V_{SENSE} = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Sense Input Current	V_{SENSE} = 0V	●	–90	–120	–150	µA
Current Limit Delay				150		ns
Driver Output Rise Time	C_L = 3300pF			30		ns
Driver Output Fall Time	C_L = 3300pF			35		ns
Driver Output High Level	I_{OUT} = –20mA I_{OUT} = –200mA		V_{DRV} – 0.6 V_{DRV} – 1.6	V_{DRV} – 0.35 V_{DRV} – 1.2		V V
Driver Output Low Level	I_{OUT} = 20mA I_{OUT} = 200mA			100 0.5	200 0.7	mV V
Shutdown Driver Output Level	$V_{S/S}$ = 0V, I_{OUT} = 20mA			100	200	mV
Idle Mode Driver Output Level	$V_{S/S}$ = V_{IN}, V_{FB} = 1.5V, I_{OUT} = 20mA			100	200	mV
S/S Pin Current	$V_{S/S}$ = V_{IN} $V_{S/S}$ = 0V				4 –2	µA µA
Operating Supply Current	V_{FB} = 1V			9		mA
Quiescent Supply Current	$V_{S/S}$ = V_{IN}, V_{FB} = 1.5V	●		140	220	µA
Shutdown Supply Current	$V_{S/S}$ = 0V $V_{S/S}$ = 0V, V_{IN} = 18V, T_A = 85°C			15 40	19	µA µA
Shutdown Threshold			0.45		1.2	V
Shutdown Delay			12	17	33	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

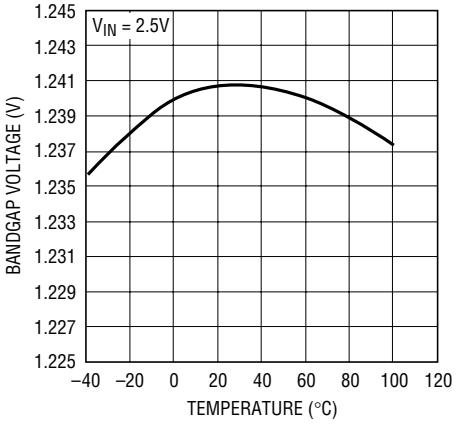
Note 2: The LT1619E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A, the power dissipation P_D and the thermal resistance θ_{JA} of the package according to the formula:

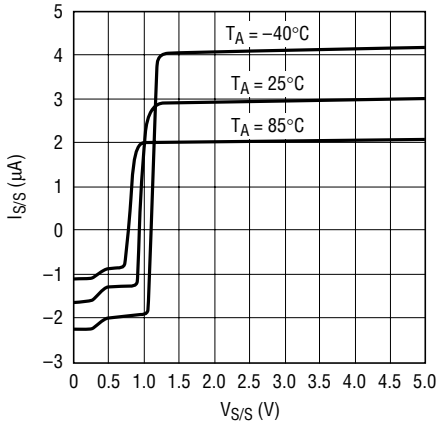
$$T_J = T_A + P_D \bullet \theta_{JA}$$

TYPICAL PERFORMANCE CHARACTERISTICS

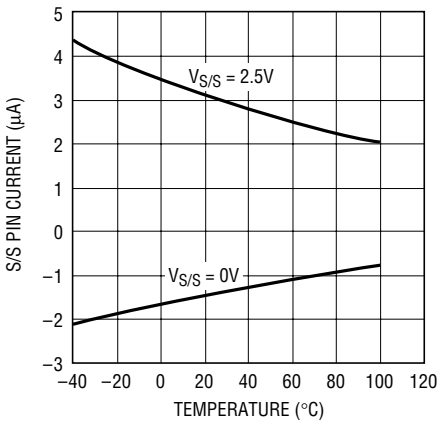
Bandgap Voltage vs Temperature



$I_{S/S}$ vs $V_{S/S}$

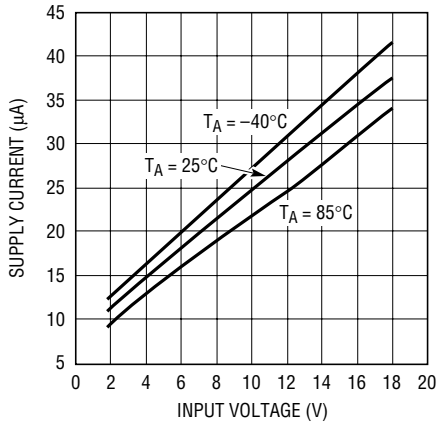


S/S Pin Current vs Temperature

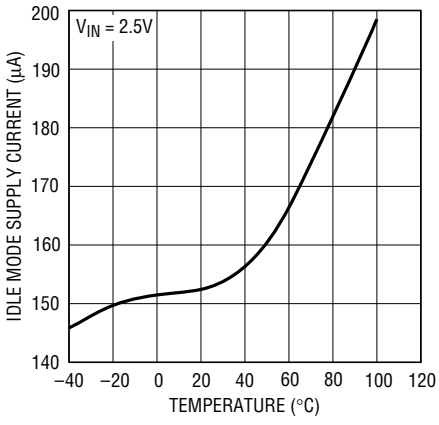


TYPICAL PERFORMANCE CHARACTERISTICS

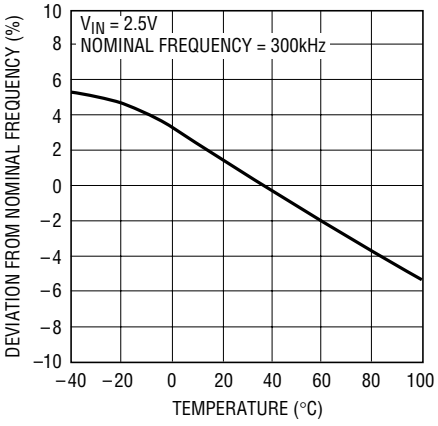
Shutdown Supply Current vs Input Voltage



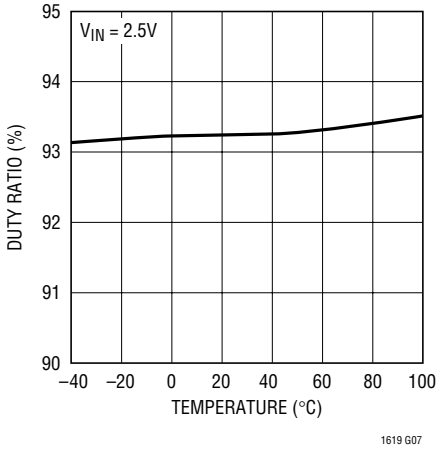
Idle Mode Supply Current vs Temperature



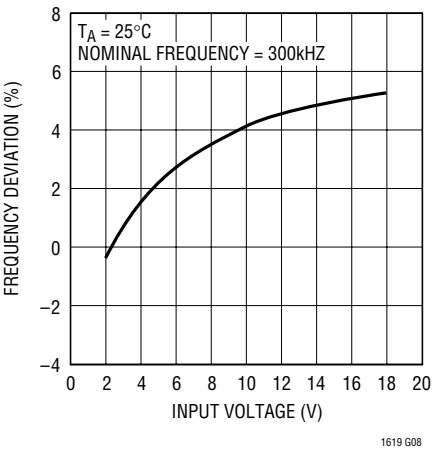
Frequency Deviation from Nominal vs Temperature



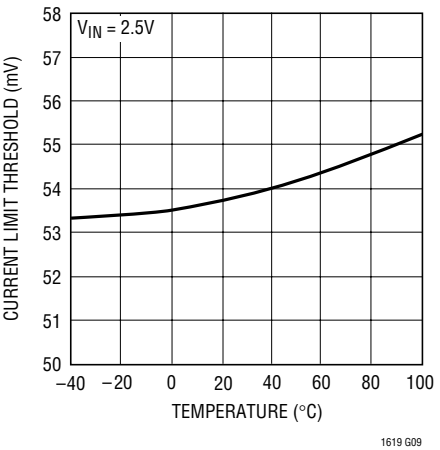
Maximum Duty Ratio vs Temperature



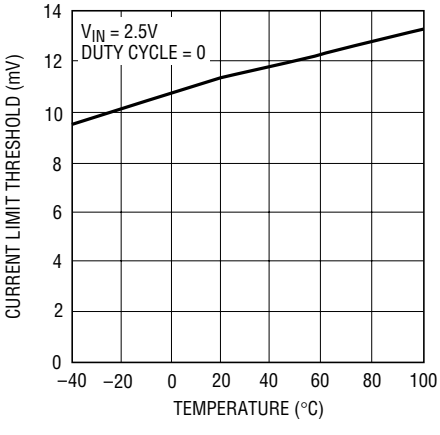
Deviation from Nominal Frequency vs Input Voltage



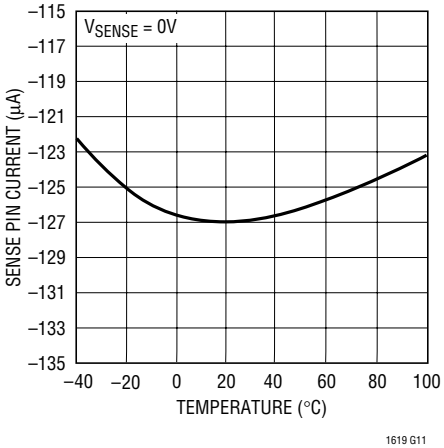
Current Limit Threshold vs Temperature



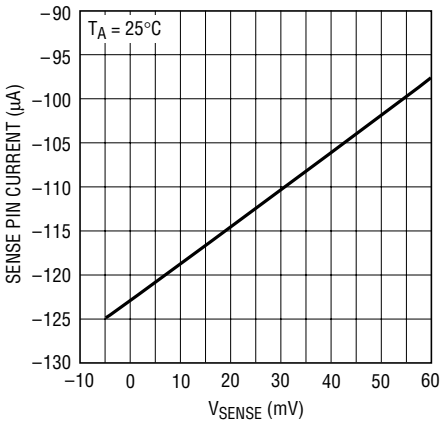
Burst Mode Operation Current Limit Threshold vs Temperature



SENSE Pin Input Bias Current vs Temperature



SENSE Pin Input Bias Current vs Sense Voltage



PIN FUNCTIONS

S/S (Pin 1): Shutdown and Synchronization. Shutdown is active low with a typical threshold voltage of 0.9V. For normal operation, the S/S pin is tied to V_{IN}. To externally synchronize the controller, drive the S/S pin with pulses.

FB (Pin 2): The inverting Input of the Error Amplifier. Connect the resistor divider tap here. Set V_{OUT} according to $V_{OUT} = 1.24(1 + R1/R2)$. See Figure 1.

V_C (Pin 3): Compensation Pin for the Error Amplifier. V_C is the output of the transconductance amplifier. Overall loop is compensated with an RC network from this pin to the ground.

GND (Pin 4): Ground. Connect to local ground plane.

SENSE (Pin 5): The Input of the Current Sense Amplifier. The SENSE pin is connected to the source of the N-channel MOSFET and to a sense resistor to the ground. The current limit threshold is internally set at 53mV, giving a maximum switch current of $53mV/R_{SENSE}$.

GATE (Pin 6): The Output of the MOSFET Driver.

DRV (Pin 7): The Pull-Up Supply of the MOSFET Driver. Tie this pin to V_{IN} (Pin 8) for nonbootstrapped operation or to the converter output for bootstrapped operation.

V_{IN} (Pin 8): Supply or Battery Input. Must be closely bypassed to the ground plane.

BLOCK DIAGRAM

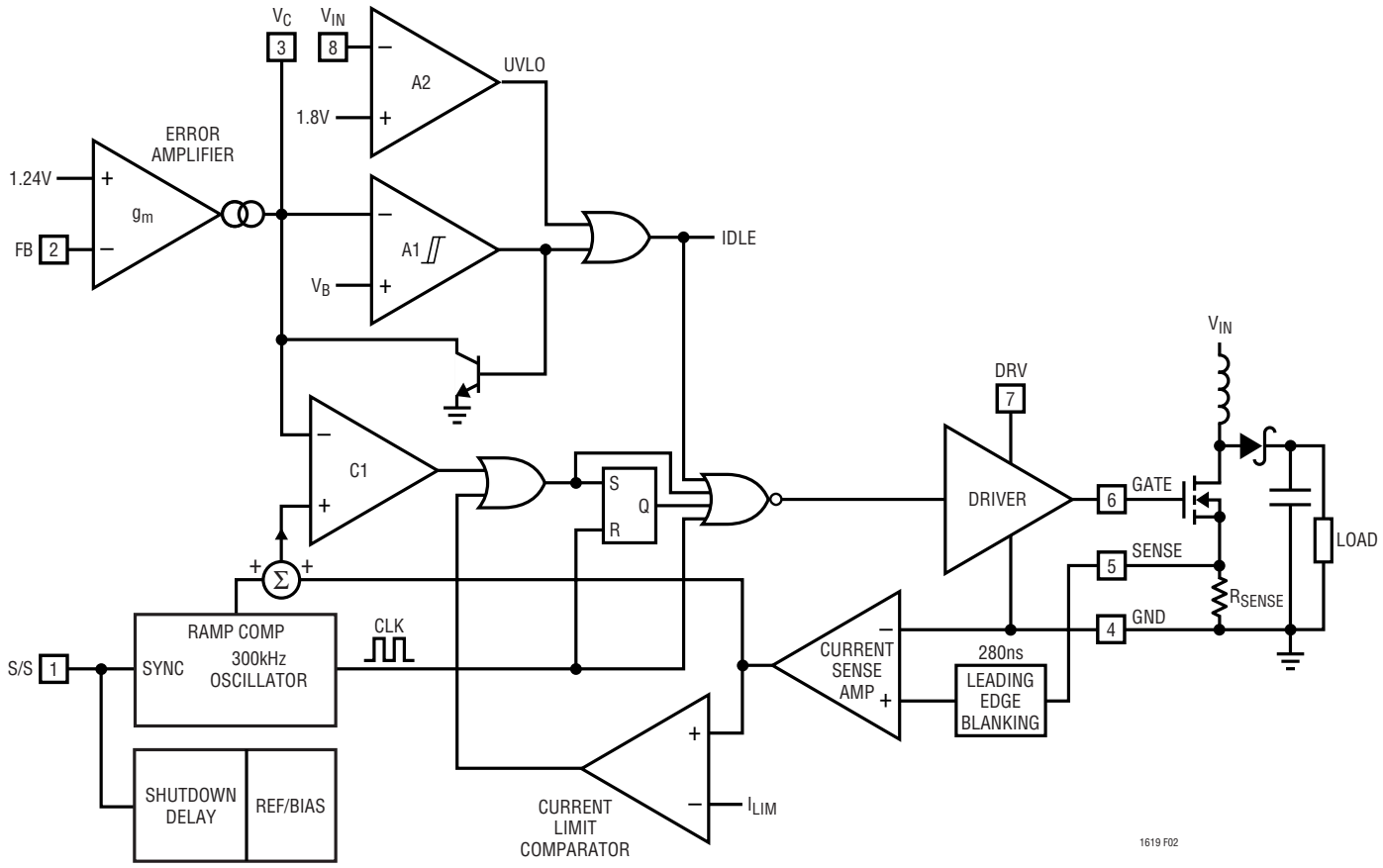


Figure 2. LT1619 Block Diagram

OPERATION

The LT1619 is a fixed frequency current mode switching regulator PWM controller that can be used in boost, SEPIC or flyback modes. The device operates from an input supply range of 1.9V to 18V, and has a separate supply pin (DRV) for the gate driver. The DRV pin can be bootstrapped to V_{OUT} for additional gate enhancement in low voltage applications like 3.3V to 5V boost converters, or connected to the input supply for higher voltage inputs.

To best understand operation of the LT1619, please refer to Figure 2, the Block Diagram. The gate drive circuit turns on the external MOSFET at the trailing edge of oscillator output signal CLK. MOSFET current is sensed with an external resistor (R_{SENSE} of Figure 1). A leading edge blanking circuit disables the current sense amplifier for 280ns immediately following switch turn-on, preventing gate charging current from prematurely tripping the PWM comparator. A slope compensating ramp, derived from the oscillator, is added to the current sense output. The driver turns off the MOSFET when this sum exceeds the error amplifier output V_C. The switch current is limited with a separate comparator. The compensating ramp is a progressive nonlinear function of the operating duty ratio whereas the current limit does not vary with the duty ratio.

Error amplifier output V_C determines the peak switch current required to regulate the output voltage. V_C can be considered a measure of output current. At heavy loads, V_C is in its upper range. Average and peak inductor currents are high. In this range, the inductor tends to run in continuous conduction mode (CCM), where current is always flowing in the inductor. As load current decreases, average and peak inductor current decreases. When the average inductor current falls below 1/2 of the peak-to-peak inductor current ripple, the converter enters discontinuous conduction mode (DCM), where current in the inductor reaches zero sometime during the discharge phase.

Further reduction in output current moves V_C towards its lower operating range, decreasing inductor current. Hysteretic comparator A1 determines if V_C is too low for the LT1619 to operate efficiently. As V_C falls below the trip voltage VB, A1's output goes high, turning off all blocks except the error amplifier, A1 and A2. The LT1619 enters the idle state and switching stops. The device draws just 140µA from the input in the idle state. Output load current discharges the output capacitor, causing the output voltage to decrease. As V_{OUT} decreases, V_C increases. As V_C increases above V_B, switching action begins, delivering power to the output. The switch current sense threshold is about 10mV in this V_C region. If the output load remains light, the output voltage will rise and V_C will fall, causing the converter to idle again. This is known as Burst Mode operation. The burst frequency depends on input voltage, output voltage, inductance and output capacitance. Output voltage ripple during Burst Mode operation is usually higher than when the converter is switching continuously. Burst Mode operation increases light load efficiency because it delivers more energy per clock cycle than possible with discontinuous mode operation and extremely low peak switch current, allowing fewer switching cycles to maintain a given output. IC supply current therefore becomes a small fraction of the total input current.

Setting Output Voltage

The output voltage of the LT1619 is set with resistive divider R1 and R2 connected from the output to ground as detailed in Figure 3. The divider tap is tied to the device FB pin. Current through R2 should be significantly higher than the FB pin bias current of 25nA. With R2 = 10k, the input bias current of the error amplifier is 0.02% of the current in R2.

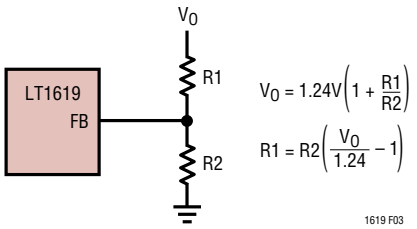


Figure 3. Feedback Resistive Divider

Synchronization and Shutdown

The S/S pin (Pin 1) can be used to synchronize the oscillator to an external source. The S/S pin is tied to the input (V_{IN} > 1.9V) for normal operation. The oscillator in the LT1619 can be externally synchronized by driving the S/S pin with a pulse train with an amplitude of at least 1V. The maximum allowable rise time is a function of the pulse amplitude, as shown in Table 1. Rise times equal to

OPERATION

or less than the number specified in Table 1 are acceptable. The maximum duty cycle is essentially unaffected by synchronization.

The device will go into shutdown mode if the S/S pin voltage stays below the shutdown threshold of 0.45V for more than 33µs. This shutdown delay is reset whenever the S/S pin voltage rises above the shutdown threshold.

Applying a logic low signal at the S/S pin causes the gate drive output to go low. Although all circuits in the LT1619 are disabled, the pull-down circuit in the MOSFET buffer is still biased on. It is capable of shunting any leakage or transient current at the GATE pin to ground, eliminating the need for an external bleed resistor. The LT1619 consumes 15µA in shutdown.

The LT1619 is guaranteed to start with a minimum V_{IN} of 1.85V. Comparator A2 senses the input voltage and generates an undervoltage lockout (UVLO) signal if V_{IN} falls below this minimum. While in undervoltage lockout, V_C is pulled low and the LT1619 stops switching. The supply current drawn by the device falls to 140µA.

Table 1. Maximum Allowable Rise Time of Synchronization Pulse. Rise Time Can Be Slower if Clock Amplitude is Higher

SYNCHRONIZATION AMPLITUDE (V)	MAXIMUM ALLOWABLE RISE TIME (ns)
1.2	120
1.5	220
2.0	350
2.5	470
3.0	530

APPLICATIONS INFORMATION

Inductor

The value of the inductor is usually selected so that the peak-to-peak ripple current is less than 30% of the maximum inductor current. The inductor should be able to handle the maximum inductor current at full load without saturation. Powder iron cores are not suitable for high frequency switch mode power supply applications because of their high core losses. Ferrite cores have very low core losses and are the material of choice for high frequency DC/DC converters.

Power MOSFET Driver

The LT1619 is capable of driving a low side N-channel power MOSFET with up to 60nC of total gate charge (Q_g). An external driver is recommended for MOSFETs with greater than 80nC of total gate charge. The peak gate drive current varies from 0.5A with V_{DRV} = 2.5V to 1.2A with V_{DRV} = 10V. The MOSFET driver is capable of charging the gate of the power MOSFET to within 350mV of the upper gate drive supply rail (DRV). It can also pull the gate of the MOSFET to within 100mV of ground during turnoff. The upper supply rail of the gate drive is brought out as a device pin (DRV) for design flexibility. In a boost converter design, the DRV pin can be tied to the converter output if the minimum input voltage is insufficient to fully enhance the power MOSFET. During start-up, the MOSFET is driven with a gate voltage starting from $V_{IN} - V_D$ (V_D is the forward voltage of the rectifying diode). As the output voltage rises, the gate drive also increases until steady state is reached. If the steady-state converter output voltage exceeds the maximum allowable gate source voltage and the input voltage is sufficient to enhance the MOSFET, the DRV pin is tied to the input supply. For a SEPIC converter, the DRV pin can be tied to the input or diode OR'ed from the input and the output (Figure 4).

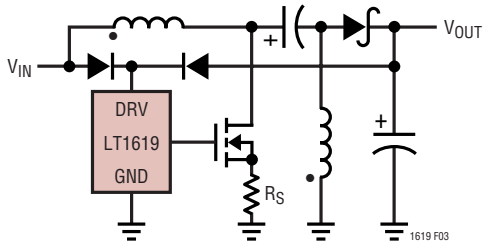


Figure 4. SEPIC Converter with Diode OR'ed Gate Drive Supply

APPLICATIONS INFORMATION

Power MOSFET

MOSFET power dissipation can be separated into frequency independent and frequency dependent components. The $R_{DS(ON)}$ loss in the switch is the product of the mean square switch current and switch $R_{DS(ON)}$ and it does not vary with the operating frequency.

The frequency-dependent switching losses consist of 1) switch transition loss due to finite rise and fall times of the drain source voltage and the drain current 2) gate switching loss, i.e., a packet of charge Q_g (the total gate charge) which is moved from the gate drive power supply to ground in every switch cycle, and 3) the drain switching loss, charge stored on the parasitic drain capacitance, C_{OSS} is dumped to ground as the switch is turned on. The transistor loss can be expressed as:

$$P_{LOSS} = I_{DRMS}^2 R_{DS(ON)} + \text{transition loss} + Q_g V_G f_S + 1/2 C_{OSS} V_{DS(OFF)}^2 f_S$$

where the transition loss can be estimated with:

$$\text{Transition Loss} = I_D \frac{C_{RSS} V_{DS(OFF)}^2 f_S}{I_{G(AVG)}}$$

Q_g = The total gate charge

V_G = Gate drive voltage $\approx V_{DRV}$

$I_{G(AVG)}$ = The average MOSFET buffer output current

f_S = Operating frequency

C_{RSS} = The average C_{GD} between V_{DS} = 0V and $V_{DS} = V_{DS(OFF)}$

At low $V_{DS(OFF)}$ (≤12V) and operating frequencies below 500kHz, the ohmic losses often dominate. For high voltage converters, the transition loss and C_{OSS} charge dumping loss can dramatically impact the converter efficiency. MOSFETs with lower parasitic capacitances but higher $R_{DS(ON)}$ may actually provide better efficiency in these situations.

Capacitors

In a switch mode DC/DC converter, output ripple voltage is the product of the equivalent series resistance (ESR) of the output capacitor and the peak-to-peak capacitor current. Depending on topology, current feeding the output capacitor can be continuous or discontinuous. The input current can also be continuous or discontinuous even if the inductor current itself is continuous. In boost topology, the inductor is in series with the input source so the input current is continuous and the output current is discontinuous. In buck-boost or flyback converters, the inductor is not in series with the input source nor the output, so neither the input current nor output current is continuous.

Whenever a terminal current is discontinuous, the capacitor at that terminal should be chosen to handle the ripple current. Capacitor reliability will be adversely affected if the ripple current exceeds the maximum allowable ratings. This maximum rating is specified as the RMS ripple current. Several capacitors may be mounted in parallel to meet the size and ripple current requirements.

Besides the ripple voltage requirements, the output capacitor also needs to be sized for acceptable output voltage variation under load transients.

Current Sensing Resistor R_{SENSE}

The LT1619 drives a low side N-channel MOSFET switch. The switch current is sensed with an external resistor R_{SENSE} connected between the source of the MOSFET and ground. The internal blanking circuit blocks the voltage spike developed across R_{SENSE} for 280ns at switch turn-on. The switch is turned off when the instantaneous voltage across R_{SENSE} exceeds the current limit threshold, V_{SENSE}. Allowing variations in V_{SENSE} yields:

$$R_{SENSE} = \frac{V_{SENSE(MIN)}}{I_{L(MAX)}}$$

The current limit threshold is constant and does not vary with duty ratio.

Due to low signal level of the sense voltage, low inductance sense resistors are required to reduce switching noise. Low TC resistors maintain constant current limit over temperature. Dale WSL and IRC series sense resistors meet these criteria.

APPLICATIONS INFORMATION

Diode

Schottky diodes are recommended for low output voltage applications because of their low forward voltage. Since Schottky diodes have negligible stored charge, charge dumping loss is also reduced. The reverse breakdown voltage of the diode should exceed the maximum reverse voltage stress of the topology used. The diode should also be able to carry the peak diode current with acceptable foward voltage. For the boost converter in Figure 1, the peak inductor current is approximately 5A. A Motorola MBRD835 is used due to its low forward voltage.

Lowering Burst Mode Operation Current Limit

The LT1619 automatically enters Burst Mode operation as V_C voltage falls below V_B. The corresponding switch current is the Burst Mode operation switch current threshold, $I_{D(BURST)}$.

The effective Burst Mode operation current threshold can be lowered by adding an offset to the input of the current sense amplifier so that the switch current appears higher to the PWM comparator. This has the effect of shifting the V_C operating range above V_B. Although Burst Mode operation is not entirely disabled, the peak switch current before entering Burst Mode operation is greatly reduced due to the offset of the current sense amplifier. The peak switch current is also determined by the current sense amplifier blanking.

To lower the Burst Mode operation current sense threshold, a resistor R_{OS} is added between the SENSE pin and the sense resistor R_{SENSE} (Figure 5). The input bias current I_{BIAS} of the current sense amplifier, which has a tolerance of ±25% and is temperature stable, develops an offset voltage at the sense input. The value of R_{OS} required for non-Burst Mode operation can be obtained with the expression:

$$I_{BIAS}R_{OS} \geq V_{SENSE(BURST)}$$

where

$V_{SENSE(BURST)}$ = (Burst Mode operation peak switch current, $I_{D(BURST)}$) • R_{SENSE}

For example, if I_{BIAS} = 120µA and $V_{SENSE(BURST)}$ = 10mV:

$$R_{OS} \geq \frac{10mV}{120\mu A} = 83\Omega$$

Allowing for 25% and 30% variations in I_{BAIS} and $V_{SENSE(BURST)}$ respectively:

$$R_{OS} = (1.25)(1.3)(83\Omega)$$

Choose R_{OS} = 137Ω to completely disable Burst Mode operation. Lower values of R_{OS} (for example, 50Ω to 100Ω) can be used to lower the effective Burst Mode current limit.

The value of the sense resistor is then adjusted to compensate for the reduced full-scale sense voltage.

$$I_{BIAS}R_{OS} + I_{L(MAX)}R_{SENSE} = 40mV$$

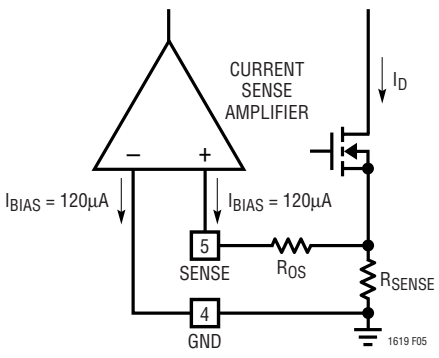


Figure 5. Lowering Burst Mode Operation Current Limit

Filtering Current Sense Signal

In a current mode converter, the current sense circuit senses the switch current and terminates the switch conduction. In the LT1619, the current sense amplifier has a full-scale input voltage range from the ground to the current limit threshold (53mV). Due to high speed switching transients and parasitic trace inductances, the current sense signal V_{SENSE} tends to be noisy. If the V_{SENSE} switching transient is excessive, the current sense amplifier will amplify the spurious transient instead, resulting in jittery operation. In situations where the internal leading edge blanking is inadequate, a lowpass filter (Figure 6) with corner frequency about 5 times the switching frequency can be used to further attenuate high speed switching transients. In Figure 6 the lowpass filter R_{OS} and C_S has a corner frequency of:

APPLICATIONS INFORMATION

$$f_{CORNER} = \frac{1}{2\pi R_{OS} C_S} \approx 5 f_S$$

(The input impedance of the sense amplifier at the SENSE pin is 2500Ω and R_{OS} is typically less than 137Ω.) Typical values for R_{OS} and C_S are 100Ω and 1nF. The 100Ω value for R_{OS} reduces Burst Mode threshold; use 10Ω and 10nF when this is not desireable.

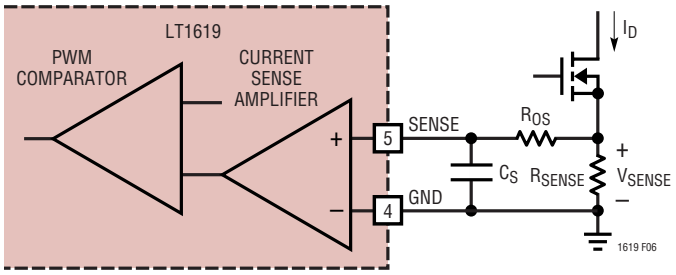


Figure 6. Current Sense Filter for Improving Jitter Performance

Use of Shutdown Function to Modify Undervoltage Lockout

The LT1619 is designed to operate from an input supply with voltage as low as 1.85V. Shutdown is activated when the S/S pin is pulled below 0.45V. The shutdown threshold is slightly greater than one junction diode forward voltage and has the temperature characteristics of a junction diode. The S/S pin is normally tied to the input when operating from a low voltage input source.

Consider the 12V to –65V isolated flyback converter (see Typical Applications). The converter draws 3A at low line while delivering 0.4A to the output. If the S/S pin is tied to the input, then the LT1619 will start switching as soon as V_{IN} exceeds the internal UVLO threshold. With full load, the converter can draw much higher than the steady-state 3A from the input source during start-up. If the input source is current limited, the input voltage will collapse and latch low.

The start-up problem can be prevented by adding a zener diode and a resistor to the S/S pin (Figure 7). This is equivalent to increasing undervoltage lockout voltage of the controller. Before V_{IN} exceeds the zener voltage V_Z, the S/S pin current is shunted to the ground through the resistor R3. The voltage developed across R3 due to $I_{S/S}$ should be less than the shutdown threshold. The LT1619 remains off until V_{IN} exceeds the sum of V_Z and the shutdown threshold. True zener diodes (BV < 5V) and higher voltage avalanche diodes have different I-V characteristics (Figure 8). They need to be biased appropriately (value of R3) in order to obtain correct UVLO threshold.

When implementing UVLO with converters with high input ripple voltages (such as flyback and forward), the circuit in Figure 7 is modified and shown in Figure 9.

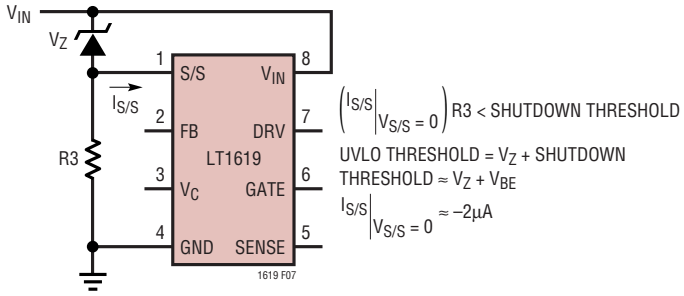


Figure 7. Implementing Undervoltage Lockout

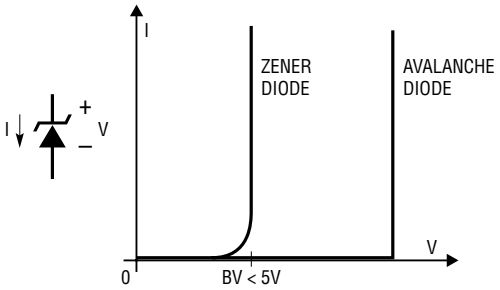


Figure 8. I-V Characteristics of Zener and Avalanche Breakdown Diodes

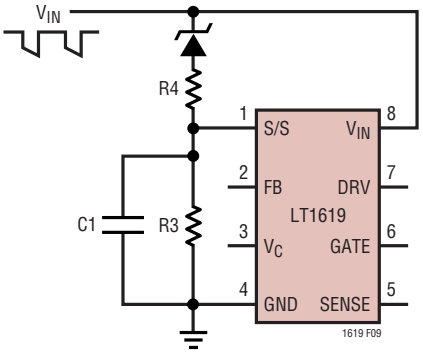


Figure 9. Filtering Input Voltage Ripple in UVLO Circuit

APPLICATIONS INFORMATION

Here the input voltage ripple is filtered with R3, R4 and C1 so as to prevent the input ripple from falsely tripping the LT1619 synchronization circuit. It is recommended that:

$$R4 \approx \frac{1}{5}R3$$

$$\text{and } \frac{1}{2\pi(R3 \,||\, R4)C1} << f_{OSC}$$

Implementation of Hysteretic UVLO with External Synchronization

The UVLO circuit shown in Figure 10 operates down to 0.9V supply voltage. Algebraically the UVLO trip points are:

$$V_{INH} = V_Z + V_{BE}\left(1 + \frac{R5}{R6 \,||\, R7}\right)$$

and

$$V_{INL} = \frac{R5 \,||\, (R7 + R9)}{R5} V_Z + V_{BE}\left(\frac{R5 \,||\, (R7 + R9)}{R5 \,||\, R6 \,||\, (R7 + R9)}\right)$$

$$\text{UVLO Hysteresis} = V_{INH} - V_{INL} = \left(\frac{R5}{R5 + R7 + R9}\right)V_Z + V_{BE}\left(\frac{R5}{R6 \,||\, R7} - \frac{R5 \,||\, (R7 + R9)}{R6}\right)$$

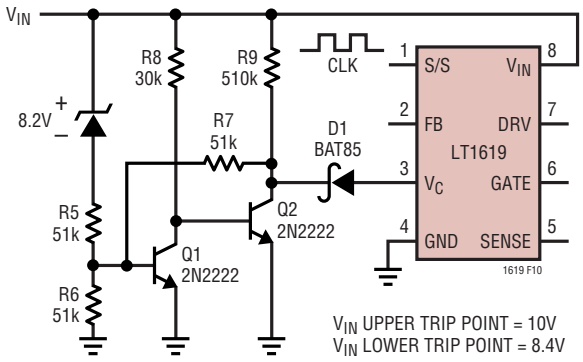


Figure 10. Addition of Hysteresis UVLO While Synchronizing the LT1619. Component Values Shown are for the Upper and the Lower V_{IN} Trip Points of 10V and 8.4V. In UVLO, the Gate Drive is Disabled by Pulling the V_C Pin Low. Disabling the Clock Shuts Down the LT1619. If Not Synchronized, the Collector of Q2 Can Be Tied to the S/S Pin and the Diode D1 Can Be Eliminated

The collector votage of Q2 is made about 1.4V at the V_{IN} lower trip voltage. This is necessary to prevent the UVLO circuit from interfering with the feedback amplifier in the LT1619.

Trickle Current Start from High Voltage Supplies

The low shutdown and idle mode quiescent supply currents of the LT1619 can be utilized to implement trickle current start from high voltage input sources (such as a 36V to 72V telecom bus). The trickle current start-up circuit in Figure 11 is modified from the UVLO circuit of Figure 10. R10 is a high value resistor that charges the storage capacitor C2 during start-up. Before V_{CC} reaches the upper UVLO trip point, Q2 holds the S/S pin low. The LT1619 draws shutdown mode current (≈15μA) from V_{CC}. Q2 collector can also be tied to the V_C pin through a diode as in Figure 10. The LT1619 will then draw idle mode quiescent current (≈140μA) from V_{CC}. R10 should be able to charge C2 while supplying current to the UVLO circuit and the LT1619. Maximizing R5 to R9 values reduces power dissipation in R10.

When V_{CC} crosses the upper UVLO threshold, the LT1619 starts switching and its current consumption increases. Before the bootstrap takes over, the LT1619 draws its current from C2. V_{CC} ramps towards the lower UVLO threshold. Increasing the value of C2 allows more time for the bootstrap circuit to establish itself before the converter enters undervoltage lockout.

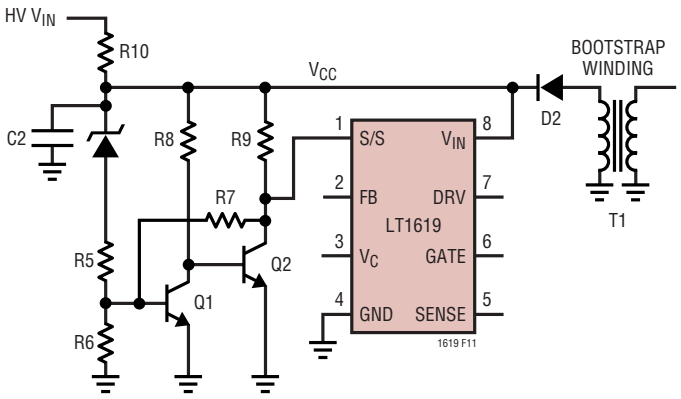


Figure 11. Trickle Current Start-Up with Bootstrapped V_{CC}

APPLICATIONS INFORMATION

Increasing Ramp Compensation While Synchronizing

The LT1619 is synchronized by forced discharge of the internal timing ramp. The timing ramp amplitude decreases as the synchronization frequency increases. Since the internal compensation ramp is derived from the timing ramp, reduced timing ramp results in diminished compensating ramp. If the LT1619 is synchronized at frequencies 20% to 30% higher than the free-running frequency, external ramp compensation will be required. Figures 12 and 13 show two such schemes.

In both figures the compensating ramps are kept linear by making R11-C1 and R14-C2 products substantially higher than the synchronizing period. The compensation ramps, whose peak amplitudes are made between 1/4 to 1/3 of the current limit threshold, are developed across R13. As a result, the effective current limit threshold is reduced by the sum of the compensating ramp and the offset voltage developed across R13 due to the SENSE pin input bias current (see Figure 5). Moreover, the current limit threshold becomes duty cycle dependent.

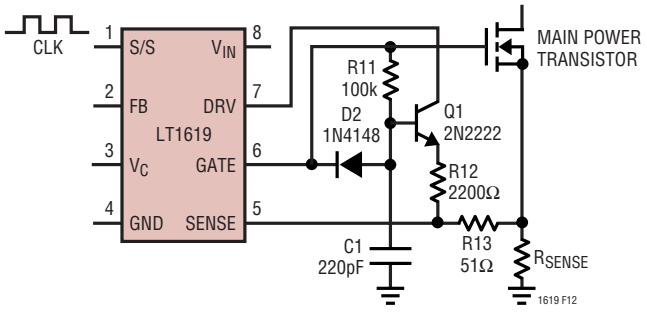


Figure 12. Increasing Ramp Compensation. Q1 Buffers the C1 Ramp. D2 Discharges C1. Values Shown are for 10V Gate Drive and 15mV Ramp Across R13 at 90% Duty Cycle and 500kHz

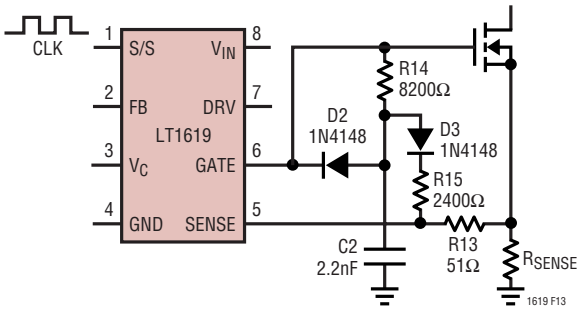


Figure 13. Externally Increasing Ramp Compensation. Similar to Figure 12 Except That C2 is Not Buffered with Transistor

PC Board Layout and Other Practical Considerations

The following is recommended for PC board layout:

1. Trace lengths of the branches carrying switched current should be kept short. For example, in the boost converter of Figure 1, the circuit loop formed by M1, R_{SENSE}, D1 and C_{OUT} carries switched current. The size of this loop must be minimized. R_{SENSE} and C_{OUT} should be grounded to a single point on a large ground plane. This reduces switching noise and overall converter jitter. It is also preferable to ground the input capacitor C1 close to the common point between C_{OUT} and R_{SENSE} although this is less important.
2. Keep the trace between the sense resistor and the SENSE pin short. When sensing high switch current, Kelvin connection to R_{SENSE} is necessary.
3. Bypass both the V_{IN} and DRV pins with ceramic capacitors next to the IC and the ground plane.
4. Keep high voltage switching nodes, such as the drain and gate of the MOSFET, away from the FB and V_C pins.
5. Use inductor so that its ripple current is between 1/4 and 1/3 of its peak current. Steeper inductor current ramp results in sharper PWM comparator switching, hence less jitter.
6. In most cases, filtering the current sense signal is not necessary for jitter-free operation.

Figure 14 is the PC board layout for the 5V/8A and 12V/5A boost converters shown in Figures 15a and 16a.

APPLICATIONS INFORMATION

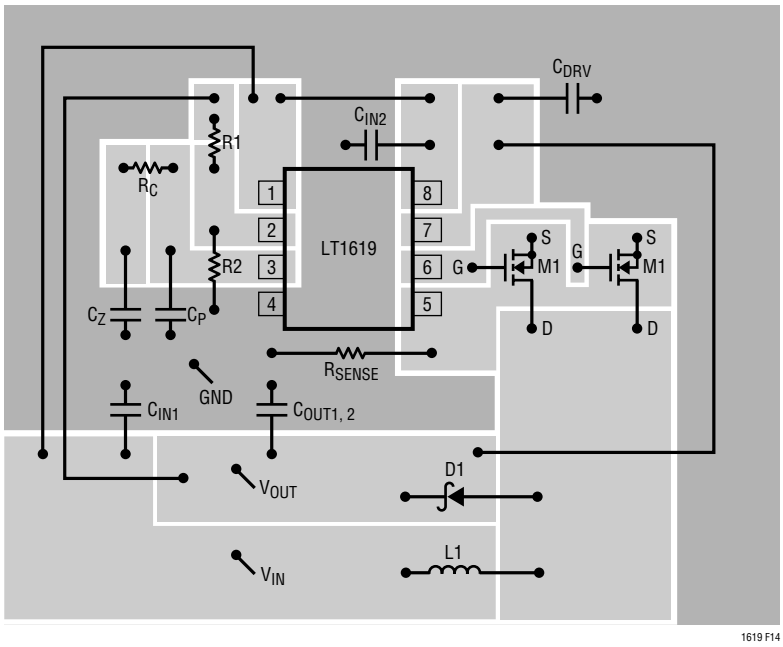
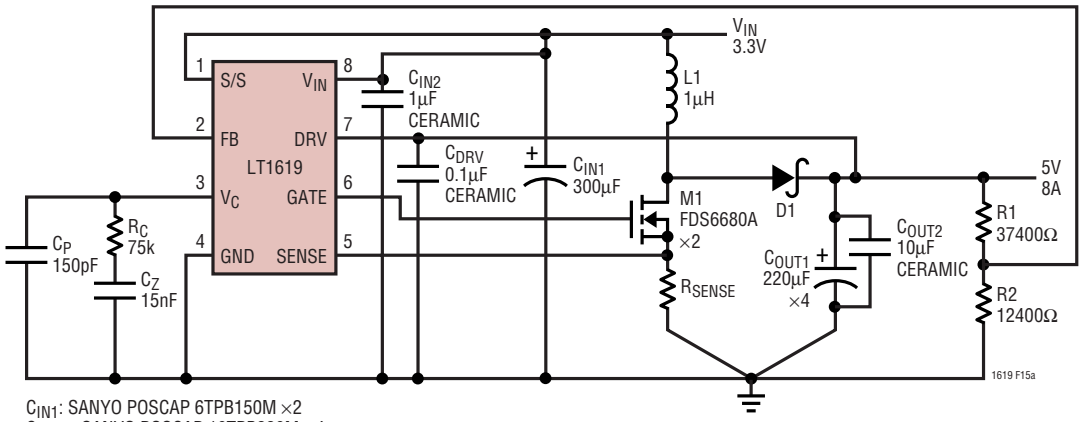


Figure 14. Recommended Component Placement for the Boost Converters in Figures 15a and 16a

APPLICATIONS INFORMATION



C_{IN1}: SANYO POSCAP 6TPB150M ×2
C_{OUT1}: SANYO POSCAP 10TPB220M ×4
D1: MOTOROLA MBRB1545CT
L1: SUMIDA CEPH149-1R0
R_{SENSE}: PANASONIC 0.002Ω 1W

Figure 15a. 3.3V to 5V/8A Boost Converter

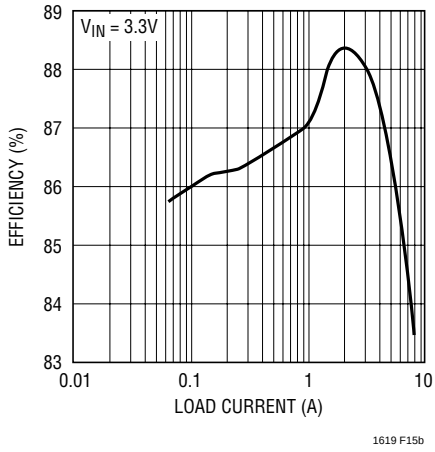
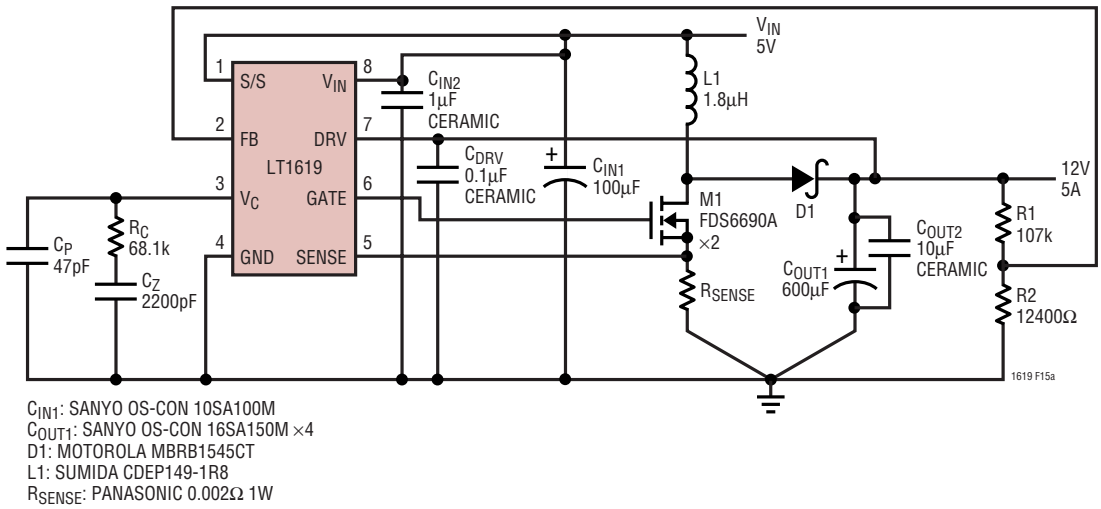


Figure 15b. Efficiency of the 5V/8A Boost Converter

APPLICATIONS INFORMATION



CIN1: SANYO OS-CON 10SA100M
COUT1: SANYO OS-CON 16SA150M ×4
D1: MOTOROLA MBRB1545CT
L1: SUMIDA CDEP149-1R8
RSENSE: PANASONIC 0.002Ω 1W

Figure 16a. 5V to 12V/5A Boost Converter

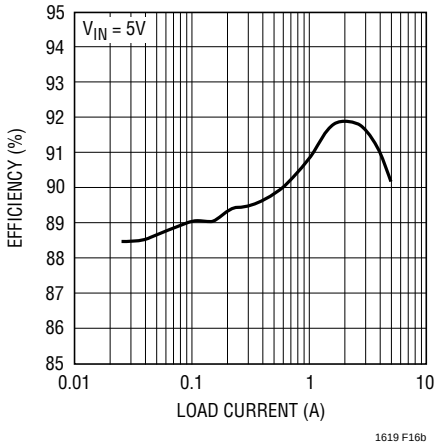


Figure 16b. Efficiency of the 12V/5A Boost Converter

TYPICAL APPLICATIONS

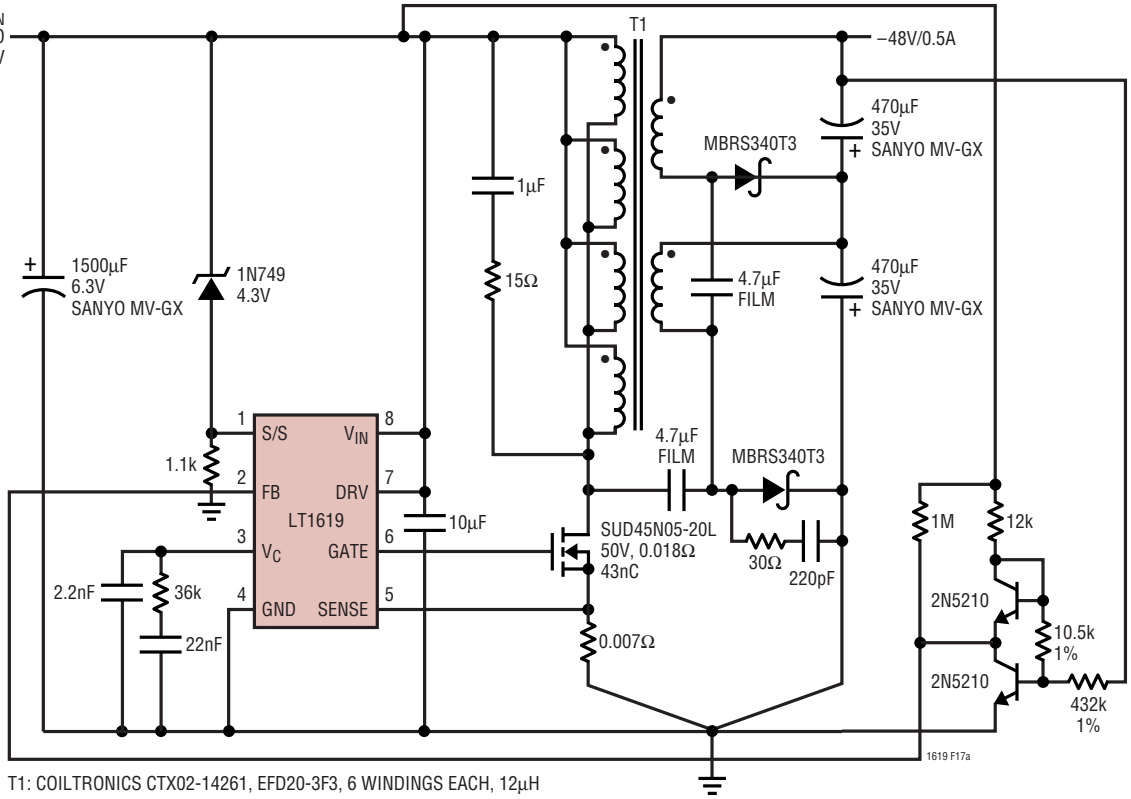


Figure 17a. 5V to –48V Cuk Converter

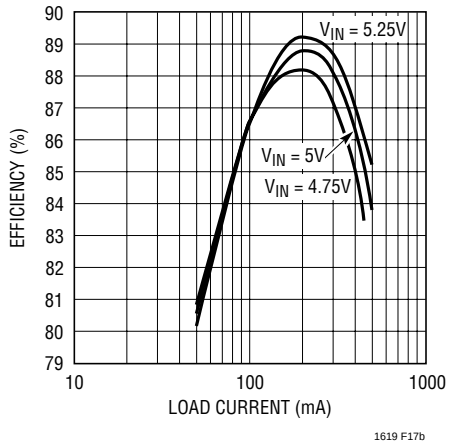


Figure 17b. Efficiency of the 5V to –48V Cuk

TYPICAL APPLICATIONS

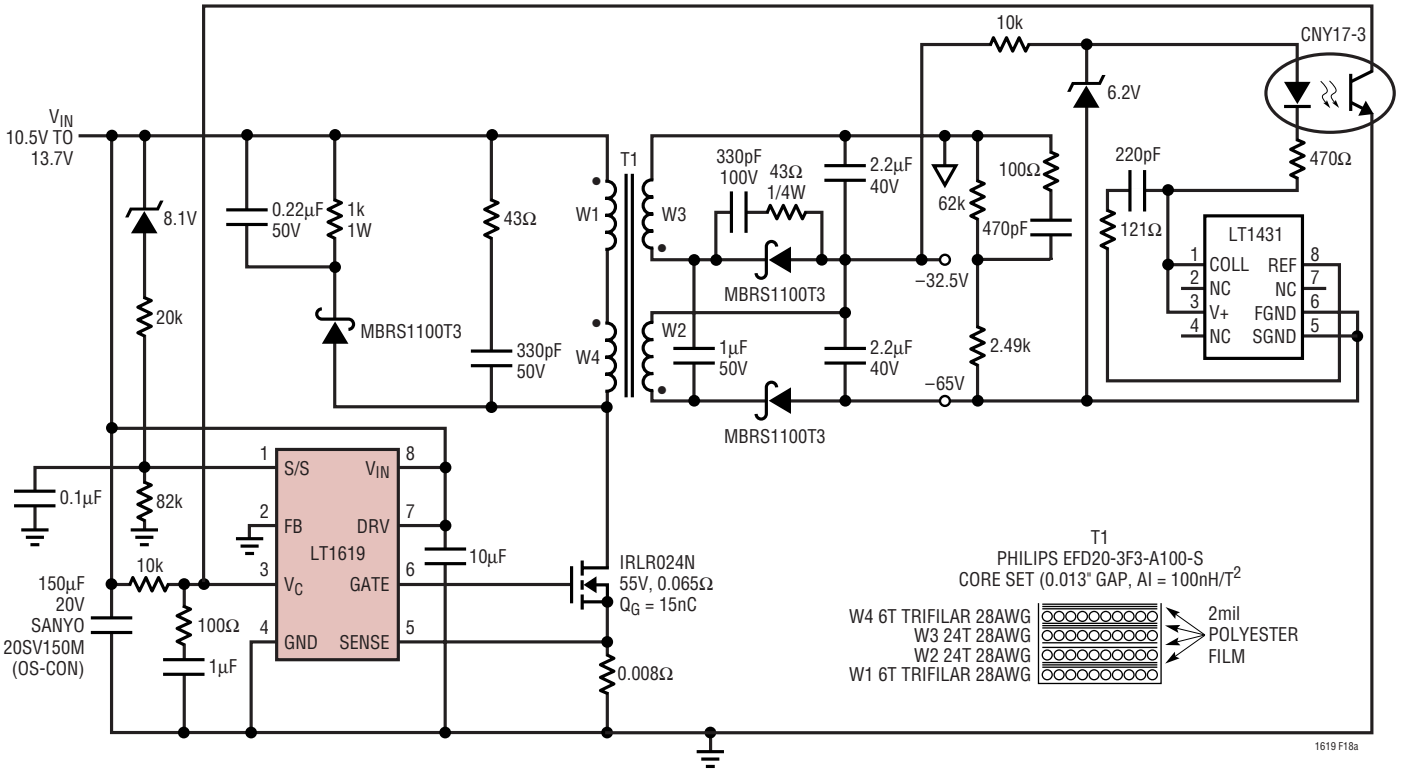


Figure 18a. Isolated Local SLIC Power Supply (Flyback) 20W Total Output Power (65V/0.3A or 32.5V/0.6A)

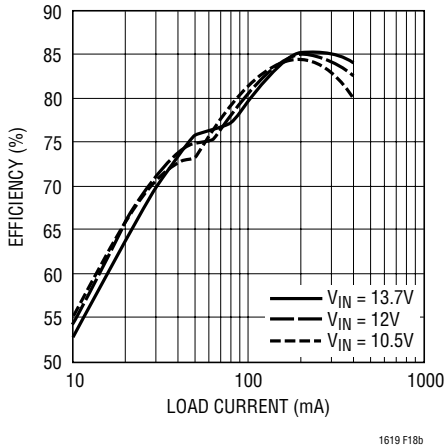
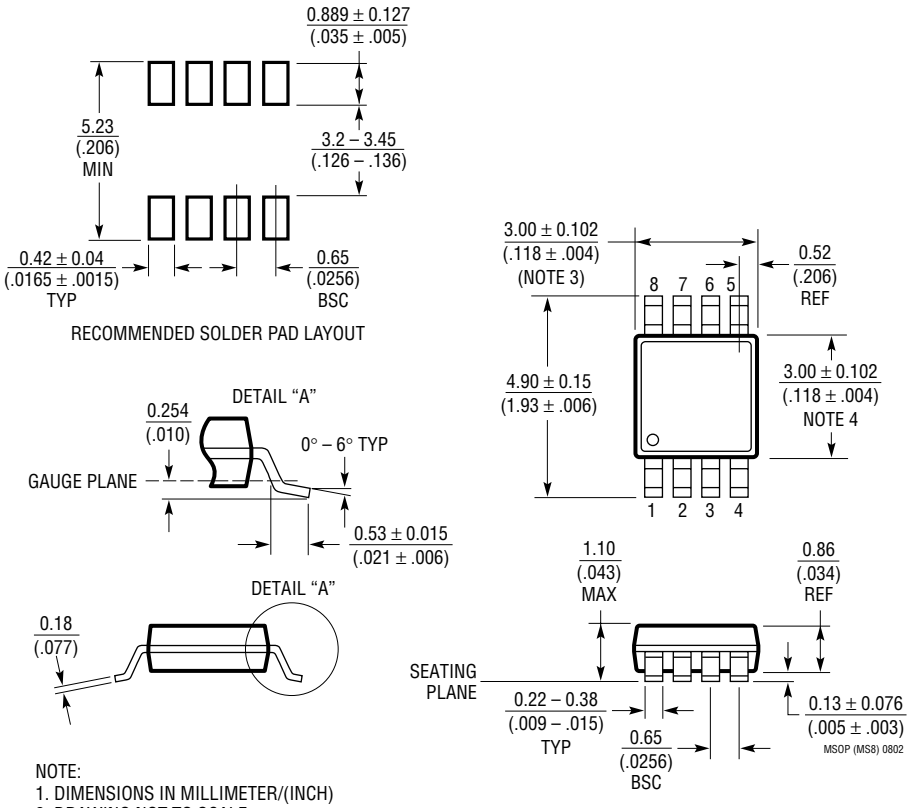


Figure 18b. Efficiency of the Isolated Local SLIC (Flyback)

PACKAGE DESCRIPTION

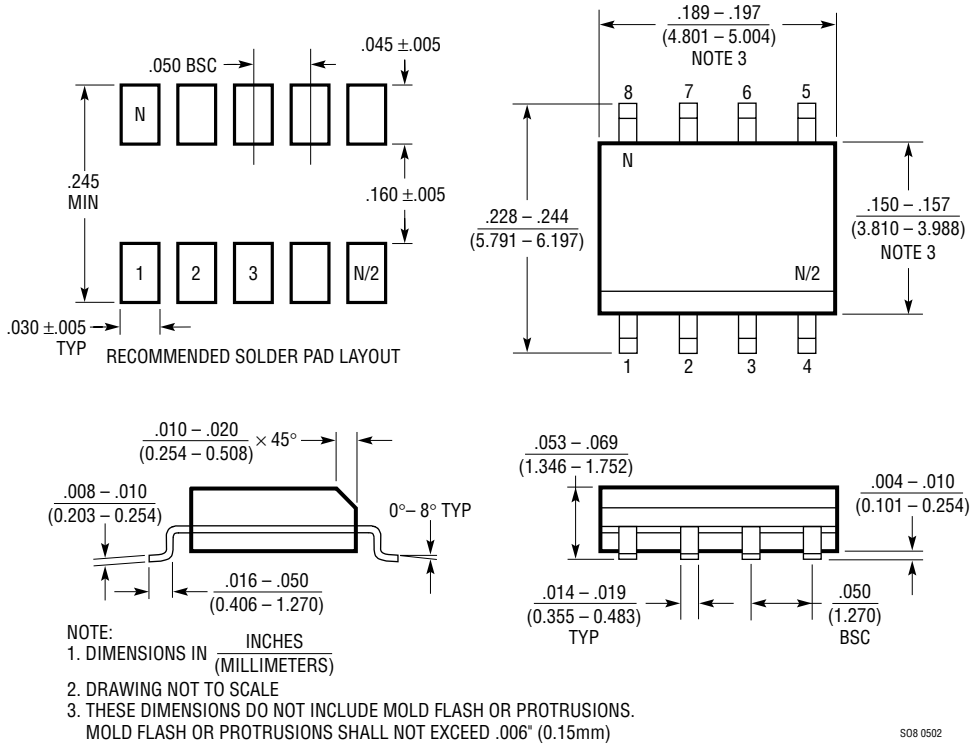
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

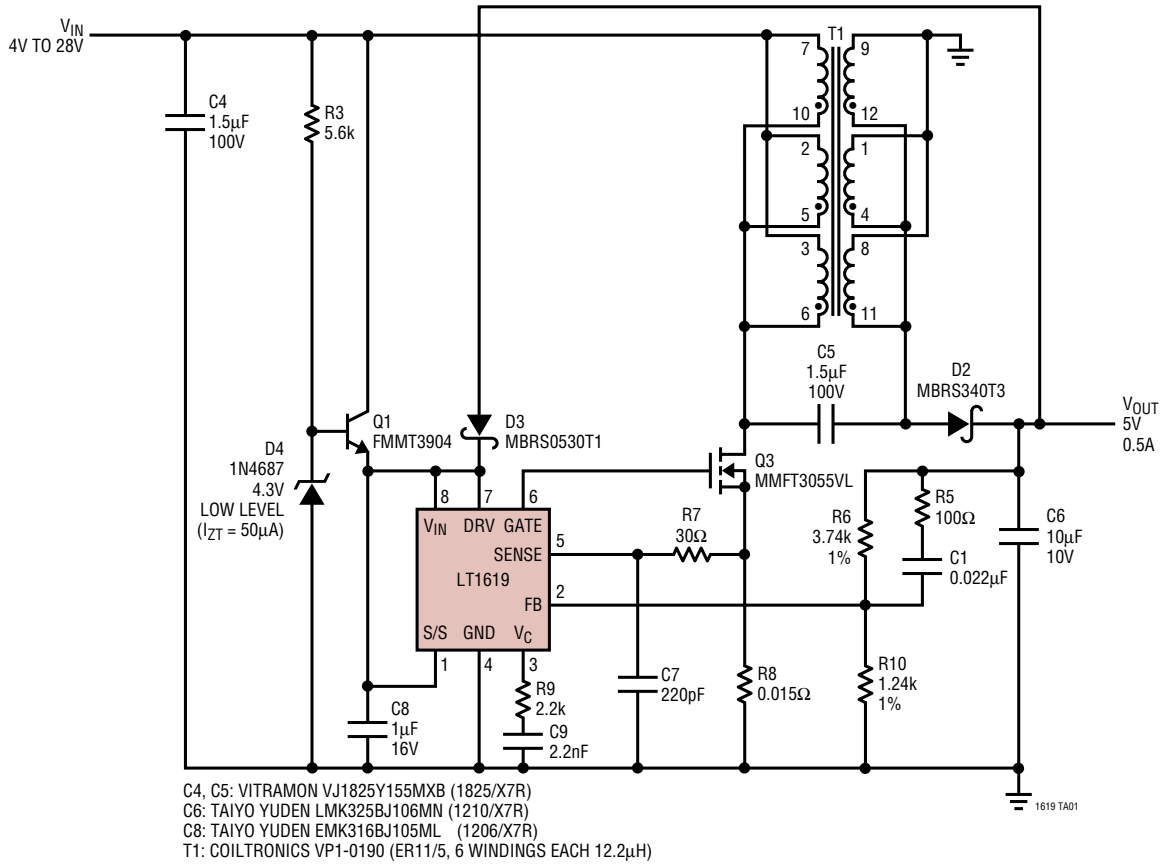
S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0502

TYPICAL APPLICATION



C4, C5: VITRAMON VJ1825Y155MXB (1825/X7R)
C6: TAIYO YUDEN LMK325BJ106MN (1210/X7R)
C8: TAIYO YUDEN EMK316BJ105ML (1206/X7R)
T1: COILTRONICS VP1-0190 (ER11/5, 6 WINDINGS EACH 12.2µH)

Figure 19. 2.5W, $4V_{IN}$-$28V_{IN}$ to 5V/0.5A Nonisolated Supply

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1370	500kHz, 6A Switching Regulator	Boost, Buck, Flyback, Forward, Inverting; 42V Switch Voltage
LT1372	500kHz, 1.5A Switching Regulator	SO-8, 2.7V ≤ V_{IN} ≤ 30V, 42V Switch Voltage
LT1613	1.4MHz, SOT-23 DC/DC Converter	Fixed Frequency, 0.9V ≤ V_{IN} ≤ 10V, 36V Switch Voltage
LTC1624	Switching Regulator Controller	SO-8, Drives N-Ch MOSFET, 3.5V ≤ V_{IN} ≤ 36V
LT1680	Synchronous Boost Controller	Synchronous Operation for High Current/High Efficiency
LT1698	Isolated or Nonisolated 10W to 100W Power Supply Solution with Multiple Outputs	50% Lower Cost than Quarter Brick and Half Brick Modules Fits the Foot Print
LTC1871	No R_{SENSE} Boost, Flyback, SEPIC Controller	2.5V ≤ V_{IN} ≤ 36V, Current Mode Control, 50kHz to 1MHz Adjustabe Frequency, MSOP-10
LTC1872	SOT-23 Boost Controller	550kHz Fixed Frequency, Current Mode
LT1946	1.2MHz, 65A DC/DC Converter	MSOP-8, 5V to 12V/400mA
LT3710/LT3781	Isolated or Nonisolated 10W to 100W Power Supply Solution with Multiple Outputs	50% Lower Cost than Quarter Brick and Half Brick Modules Fits the Foot Print

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