

# LT1180A/LT1181A

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ( $V_{CC}$ ) .....	6V	Short-Circuit Duration	
$V^+$ .....	13.2V	$V^+$ .....	30 sec
$V^-$ .....	-13.2V	$V^-$ .....	30 sec
Input Voltage		Driver Output .....	Indefinite
Driver .....	$V^-$ to $V^+$	Receiver Output .....	Indefinite
Receiver .....	-30V to 30V	Operating Temperature Range	
ON/OFF .....	-0.3V to 12V	LT1180AI/LT1181AI .....	-40°C to 85°C
Output Voltage		LT1180AC/LT1181AC .....	0°C to 70°C
Driver .....	$V^+ - 30V$ to $V^- + 30V$	Storage Temperature Range .....	-65°C to 150°C
Receiver .....	-0.3V to $V_{CC} + 0.3V$	Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>NC 1, 18 ON/OFF  C1+ 2, 17 <math>V_{CC}</math>  <math>V^+</math> 3, 16 GND  C1- 4, 15 TR1 OUT  C2+ 5, 14 REC1 IN  C2- 6, 13 REC1 OUT  <math>V^-</math> 7, 12 TR1 IN  TR2 OUT 8, 11 TR2 IN  REC2 IN 9, 10 REC2 OUT</p> <p>N PACKAGE 18-LEAD PDIP  SW PACKAGE 18-LEAD PLASTIC SO (WIDE)  <math>T_{JMAX} = 125^\circ\text{C}</math>, <math>\theta_{JA} = 80^\circ\text{C/W}</math>, <math>\theta_{JC} = 36^\circ\text{C/W}</math> (N)  <math>T_{JMAX} = 125^\circ\text{C}</math>, <math>\theta_{JA} = 90^\circ\text{C/W}</math>, <math>\theta_{JC} = 26^\circ\text{C/W}</math> (SW)</p>	<p>ORDER PART NUMBER</p> <p>LT1180ACN  LT1180ACSW  LT1180AIN  LT1180AISW</p>	<p>TOP VIEW</p> <p>C1+ 1, 16 <math>V_{CC}</math>  <math>V^+</math> 2, 15 GND  C1- 3, 14 TR1 OUT  C2+ 4, 13 REC1 IN  C2- 5, 12 REC1 OUT  <math>V^-</math> 6, 11 TR1 IN  TR2 OUT 7, 10 TR2 IN  REC2 IN 8, 9 REC2 OUT</p> <p>N PACKAGE 16-LEAD PDIP  SW PACKAGE 16-LEAD PLASTIC SO (WIDE)  <math>T_{JMAX} = 125^\circ\text{C}</math>, <math>\theta_{JA} = 90^\circ\text{C/W}</math>, <math>\theta_{JC} = 46^\circ\text{C/W}</math> (N)  <math>T_{JMAX} = 125^\circ\text{C}</math>, <math>\theta_{JA} = 95^\circ\text{C/W}</math>, <math>\theta_{JC} = 27^\circ\text{C/W}</math> (SW)</p>	<p>ORDER PART NUMBER</p> <p>LT1181ACN  LT1181ACSW  LT1181AIN  LT1181AISW</p>
<p>J PACKAGE 18-LEAD CERDIP  <math>T_{JMAX} = 150^\circ\text{C}</math>, <math>\theta_{JA} = 100^\circ\text{C/W}</math>, <math>\theta_{JC} = 40^\circ\text{C/W}</math> (J)</p> <p><b>OBSELETE PACKAGE</b>  Consider N Package for Alternate Source</p>	<p>LT1180AMJ</p>	<p>J PACKAGE 16-LEAD CERDIP  <math>T_{JMAX} = 150^\circ\text{C}</math>, <math>\theta_{JA} = 100^\circ\text{C/W}</math>, <math>\theta_{JC} = 40^\circ\text{C/W}</math> (J)</p> <p><b>OBSELETE PACKAGE</b>  Consider N Package for Alternate Source</p>	<p>LT1181AMJ</p>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the operating temperature range  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$  for commercial grade, and  $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$  for industrial grade. (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Power Supply Generator</b>					
$V^+$ Output			7.9		V
$V^-$ Output			-7.0		V
Supply Current ( $V_{CC}$ )	(Note 3), $T_A = 25^\circ\text{C}$		9	13	mA
		●		16	mA
Supply Current When OFF ( $V_{CC}$ )	Shutdown (Note 4) LT1180A Only		1	10	$\mu\text{A}$
		●			
Supply Rise Time	$C1 = C2 = C3 = C4 = 0.1\mu\text{F}$		0.2		ms
Shutdown to Turn-On	LT1180A Only		0.2		ms
ON/OFF Pin Thresholds	Input Low Level (Device Shutdown)	●	0.8	1.2	V
	Input High Level (Device Enabled)	●	1.6	2.4	V

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**ELECTRICAL CHARACTERISTICS** The ● denotes specifications which apply over the operating temperature range ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$  for commercial grade, and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  for industrial grade. (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
ON/OFF Pin Current	$0\text{V} \leq V_{\text{ON/OFF}} \leq 5\text{V}$		●	-15		80	$\mu\text{A}$
Oscillator Frequency					130		kHz
<b>Driver</b>							
Output Voltage Swing	Load = 3k to GND	Positive Negative	●	5.0	7.5 -6.3	-5.0	V V
Logic Input Voltage Level	Input Low Level ( $V_{\text{OUT}} = \text{High}$ )		●		1.4	0.8	V
Input High Level ( $V_{\text{OUT}} = \text{Low}$ )			●	2.0	1.4		V
Logic Input Current	$0.8\text{V} \leq V_{\text{IN}} \leq 2.0\text{V}$		●		5	20	$\mu\text{A}$
Output Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$			$\pm 9$	17		mA
Output Leakage Current	Shutdown $V_{\text{OUT}} = \pm 30\text{V}$ (Note 4)		●		10	100	$\mu\text{A}$
Date Rate (Note 7)	$R_L = 3\text{k}, C_L = 2500\text{pF}$ $R_L = 3\text{k}, C_L = 1000\text{pF}$			120 250			kBaud kBaud
Slew Rate	$R_L = 3\text{k}, C_L = 51\text{pF}$				15	30	V/ $\mu\text{s}$
$R_L = 3\text{k}, C_L = 2500\text{pF}$				4	7		V/ $\mu\text{s}$
Propagation Delay	Output Transition $t_{\text{HL}}$ High-to-Low (Note 5) Output Transition $t_{\text{LH}}$ Low-to-High				0.6 0.5	1.3 1.3	$\mu\text{s}$ $\mu\text{s}$
<b>Receiver</b>							
Input Voltage Thresholds	Input Low Threshold ( $V_{\text{OUT}} = \text{High}$ )	C Grade	●	0.8	1.3		V
	Input High Threshold ( $V_{\text{OUT}} = \text{Low}$ )	C Grade	●		1.7	2.4	V
	Input LowI,	M Grade	●	0.2	1.3		V
	Input HighI,	M Grade	●		1.7	3.0	V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance	$V_{\text{IN}} = \pm 10\text{V}$			3	5	7	k $\Omega$
Output Leakage Current	Shutdown (Note 4) $0 \leq V_{\text{OUT}} \leq V_{\text{CC}}$		●		1	10	$\mu\text{A}$
Output Voltage	Output Low, $I_{\text{OUT}} = -1.6\text{mA}$		●		0.2	0.4	V
	Output High, $I_{\text{OUT}} = 160\mu\text{A}$ ( $V_{\text{CC}} = 5\text{V}$ )		●	3.5	4.2		V
Output Short-Circuit Current	Sinking Current, $V_{\text{OUT}} = V_{\text{CC}}$ Sourcing Current, $V_{\text{OUT}} = 0\text{V}$			10	-20 20	-10 mA	mA
Propagation Delay	Output Transition $t_{\text{HL}}$ High-to-Low (Note 6)				250	600	ns
	Output Transition $t_{\text{LH}}$ Low-to-High				350	600	ns

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

**Note 2:** Testing done at  $V_{\text{CC}} = 5\text{V}$  and  $V_{\text{ON/OFF}} = 3\text{V}$ , unless otherwise specified.

**Note 3:** Supply current is measured as the average over several charge pump cycles.  $C^+ = C^- = C_1 = C_2 = 0.1\mu\text{F}$ . All outputs are open, with all driver inputs tied high.

**Note 4:** Supply current measurements in SHUTDOWN are performed with  $V_{\text{ON/OFF}} \leq 0.1\text{V}$ .

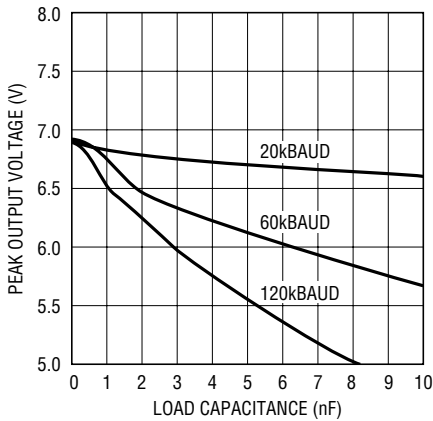
**Note 5:** For driver delay measurements,  $R_L = 3\text{k}$  and  $C_L = 51\text{pF}$ . Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing ( $t_{\text{HL}} = 1.4\text{V}$  to  $0\text{V}$  and  $t_{\text{LH}} = 1.4\text{V}$  to  $0\text{V}$ ).

**Note 6:** For receiver delay measurements,  $C_L = 51\text{pF}$ . Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold ( $t_{\text{HL}} = 1.3\text{V}$  to  $2.4\text{V}$  and  $t_{\text{LH}} = 1.7\text{V}$  to  $0.8\text{V}$ ).

**Note 7:** Data rate operation guaranteed by slew rate, short-circuit current and propagation delay tests.

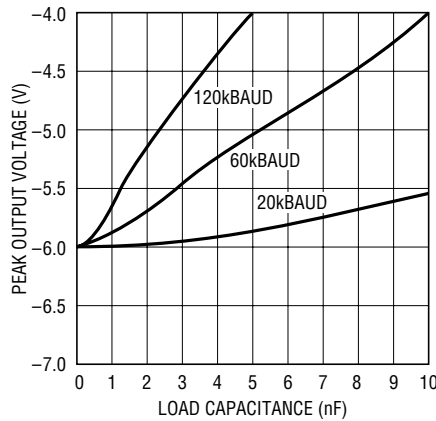
## TYPICAL PERFORMANCE CHARACTERISTICS

**Driver Maximum Output Voltage vs Load Capacitance**



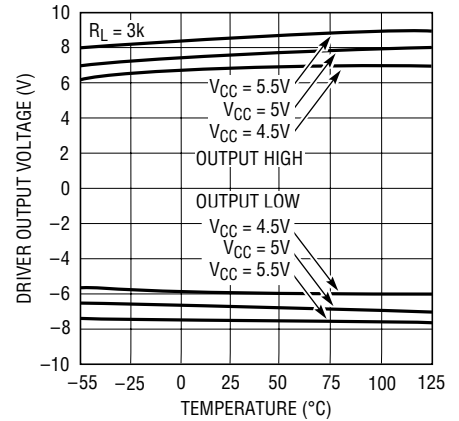
LT1180A • TPC01

**Driver Minimum Output Voltage vs Load Capacitance**



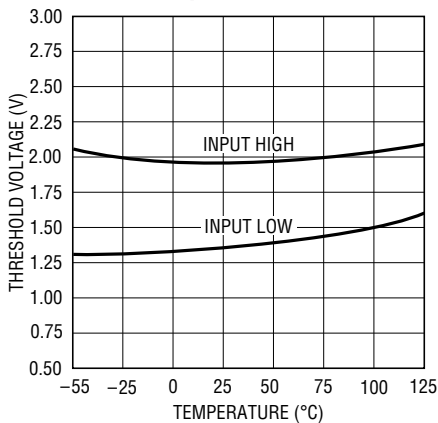
LT1180A • TPC02

**Driver Output Voltage**



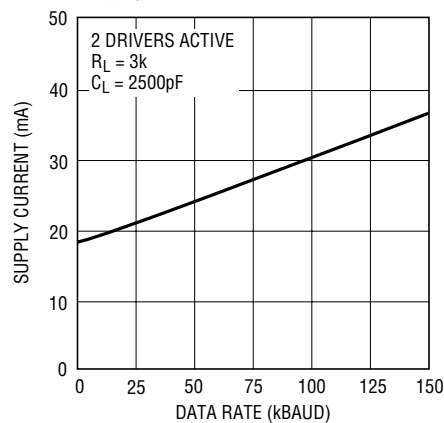
LT1180A • TPC03

**Receiver Input Thresholds**



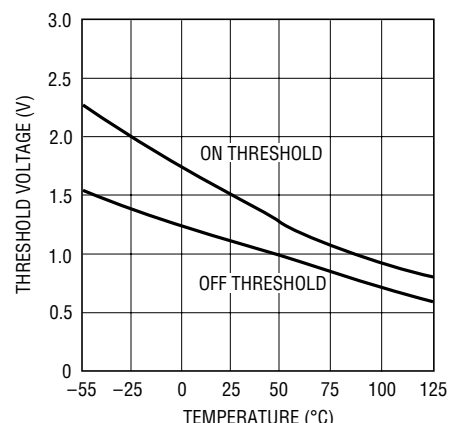
LT1180A • TPC04

**Supply Current vs Data Rate**



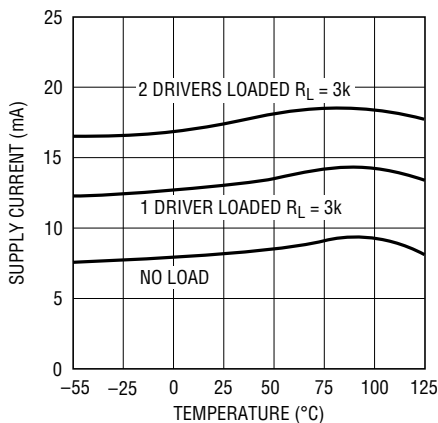
LT1180A • TPC05

**ON/OFF Thresholds**



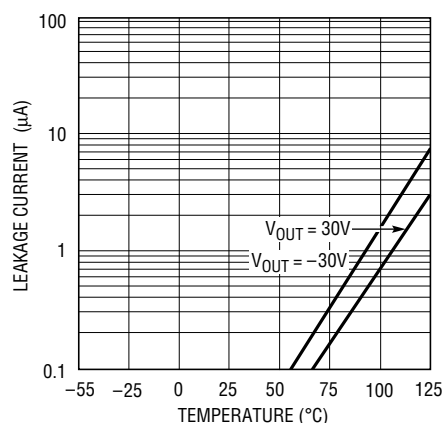
LT1180A • TPC06

**Supply Current**



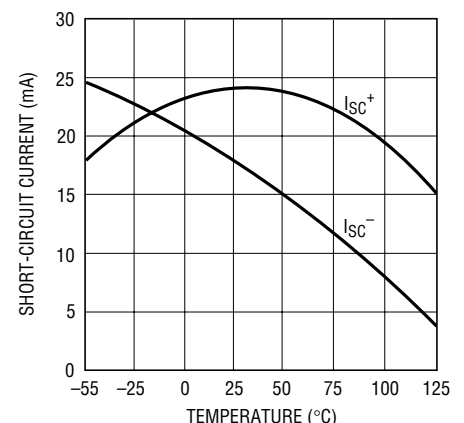
LT1180A • TPC07

**Driver Leakage in Shutdown**



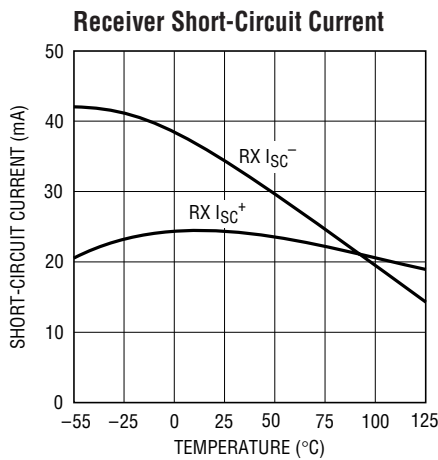
LT1180A • TPC08

**Driver Short-Circuit Current**

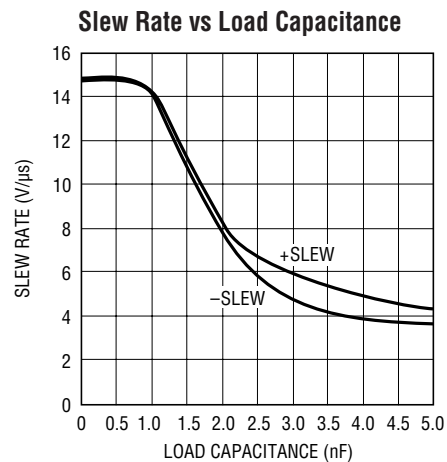


LT1180A • TPC09

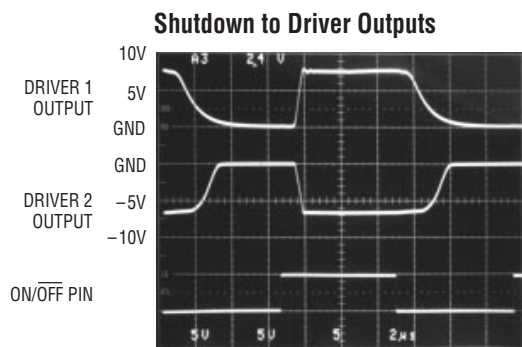
## TYPICAL PERFORMANCE CHARACTERISTICS



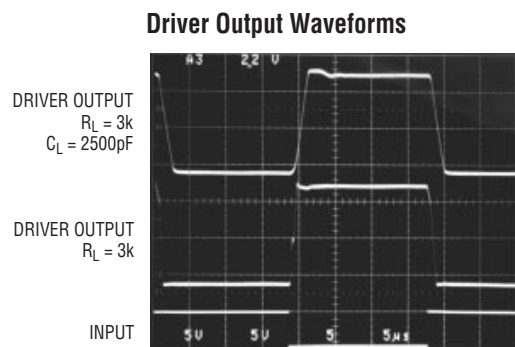
LT1180A • TPC10



LT1180A • TPC11



LT1180A • TPC12



LT1180A • TPC13

## PIN FUNCTIONS

**$V_{CC}$ :** 5V Input Supply Pin. This pin should be decoupled with a 0.1μF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

**GND:** Ground Pin.

**ON/OFF:** A TTL/CMOS Compatible Operating Mode Control. A logic low puts the LT1180A in shutdown mode. Supply current drops to zero and both driver and receiver outputs assume a high impedance state. A logic high fully enables the device.

**$V^+$ :** Positive Supply Output (RS232 Drivers).  $V^+ \approx 2V_{CC} - 1.5V$ . This pin requires an external charge storage capacitor  $C \geq 0.1\mu F$ , tied to ground or  $V_{CC}$ . Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the  $V^+$  and  $V^-$  pins may be paralleled into common capacitors.

**$V^-$ :** Negative Supply Output (RS232 Drivers).  $V^- \approx -(2V_{CC} - 2.5V)$ . This pin requires an external charge storage capacitor  $C \geq 0.1\mu F$ . Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the  $V^+$  and  $V^-$  pins may be paralleled into common capacitors.

## PIN FUNCTIONS

**TR1 IN, TR2 IN:** RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to  $V_{CC}$ .

**TR1 OUT, TR2 OUT:** Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when in shutdown mode,  $V_{CC} = 0V$ , or when the driver disable pin is active. Outputs are fully short-circuit protected from  $V^- + 30V$  to  $V^+ - 30V$ . Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to  $\pm 10kV$  for human body model discharges.

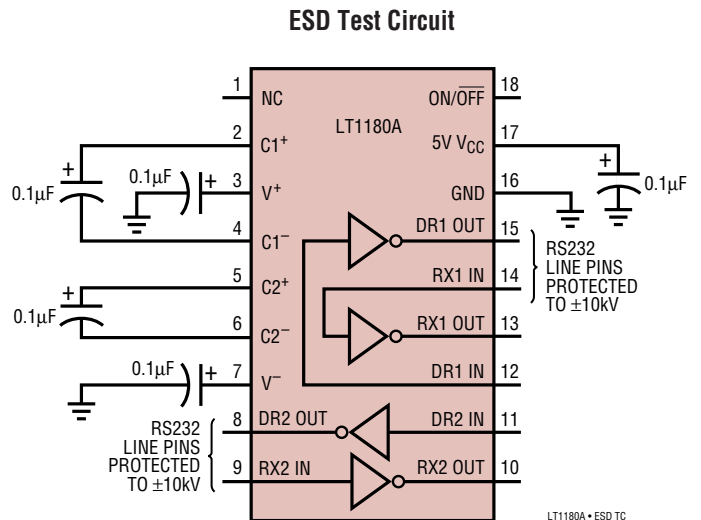
**REC1 IN, REC2 IN:** Receiver Inputs. These pins accept RS232 level signals ( $\pm 30V$ ) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to  $\pm 10kV$  for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

**REC1 OUT, REC2 OUT:** Receiver outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in shutdown mode to allow data line sharing. Outputs are fully short-circuit protected to ground or  $V_{CC}$  with the power on, off or in the shutdown mode.

**C1+, C1-, C2+, C2-:** Commutating Capacitor Inputs. These pins require two external capacitors  $C \geq 0.1\mu F$ : one from  $C1^+$  to  $C1^-$  and another from  $C2^+$  to  $C2^-$ .  $C1$  should be deleted if a separate 12V supply is available and connected to pin  $C1^+$ . Similarly,  $C2$  should be deleted if a separate  $-12V$  supply is connected to pin  $V^-$ .

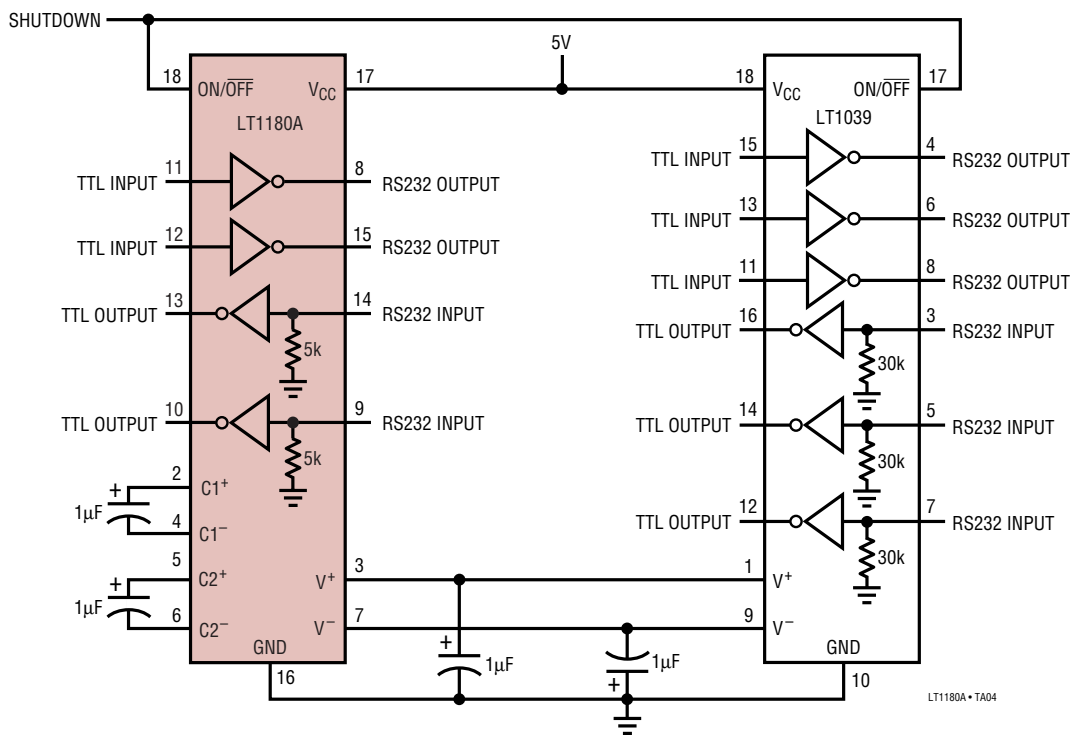
## ESD PROTECTION

The RS232 line inputs of the LT1180A/LT1181A have on-chip protection from ESD transients up to  $\pm 10kV$ . The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the circuit must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins  $V_{CC}$ ,  $V_L$ ,  $V^+$ ,  $V^-$ , and GND shorted to ground or connected with low ESR capacitors.



TYPICAL APPLICATION

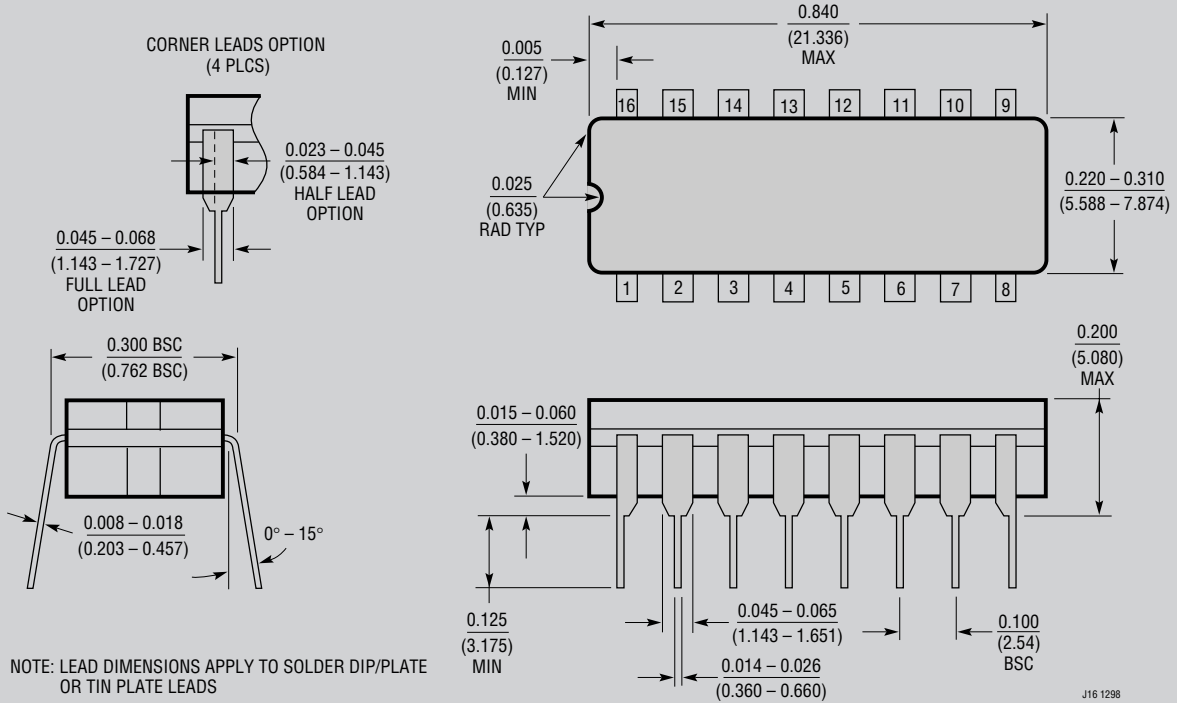
Supporting an LT1039 (Triple Driver/Receiver)



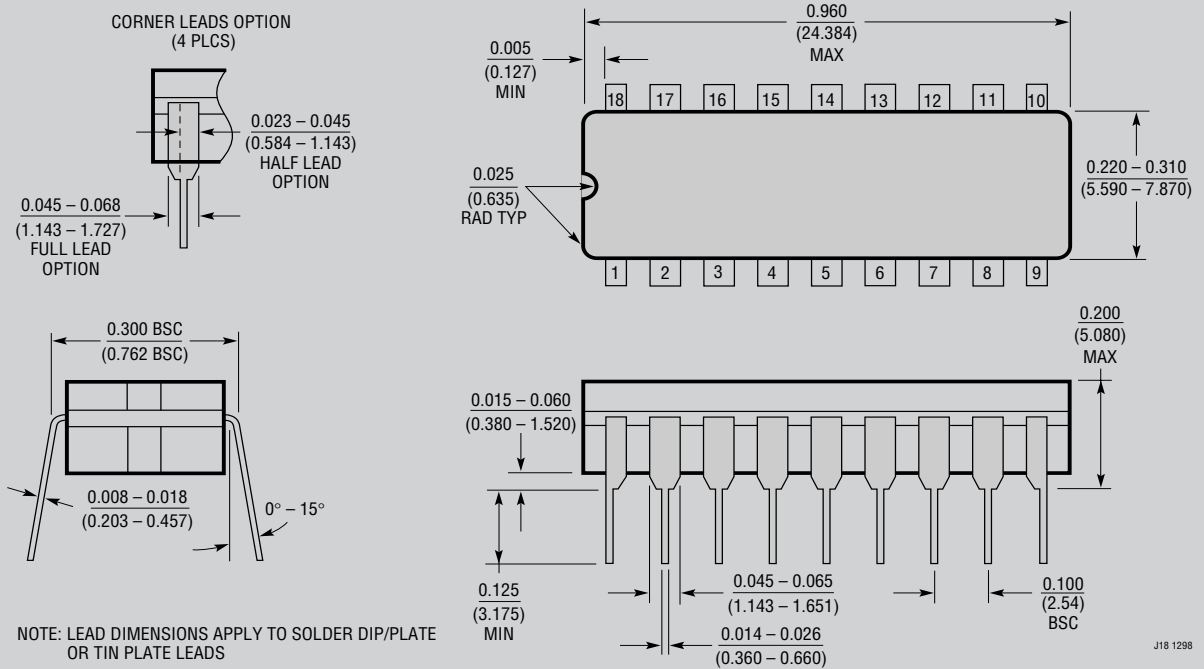
LT1180A • TA04

**PACKAGE DESCRIPTION**

**J Package**  
**16-Lead CERDIP (Narrow .300 Inch, Hermetic)**  
 (Reference LTC DWG # 05-08-1110)



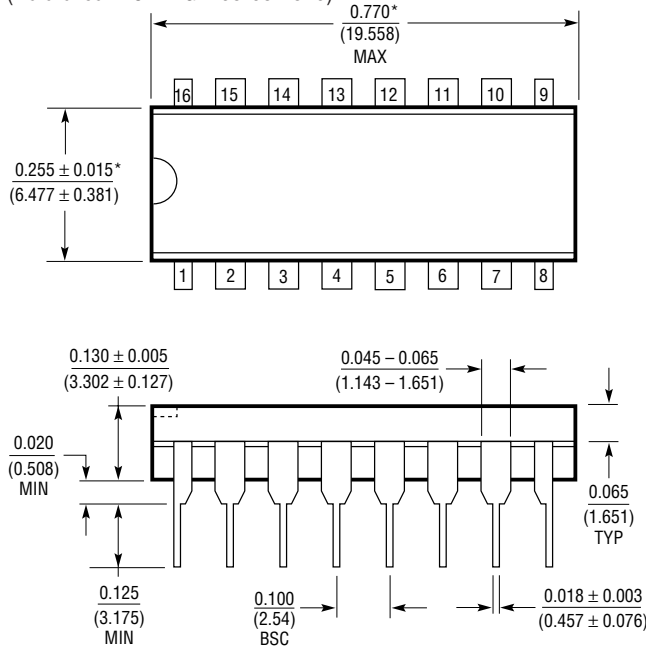
**J Package**  
**18-Lead CERDIP (Narrow .300 Inch, Hermetic)**  
 (Reference LTC DWG # 05-08-1110)



**OBSOLETE PACKAGES**

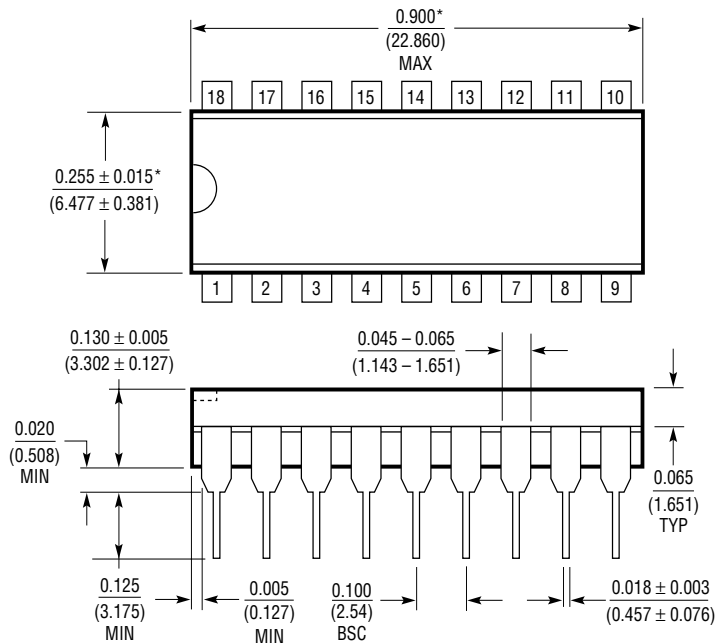
**PACKAGE DESCRIPTION**

**N Package**  
**16-Lead PDIP (Narrow .300 Inch)**  
 (Reference LTC DWG # 05-08-1510)



N16 1098

**N Package**  
**18-Lead PDIP (Narrow .300 Inch)**  
 (Reference LTC DWG # 05-08-1510)

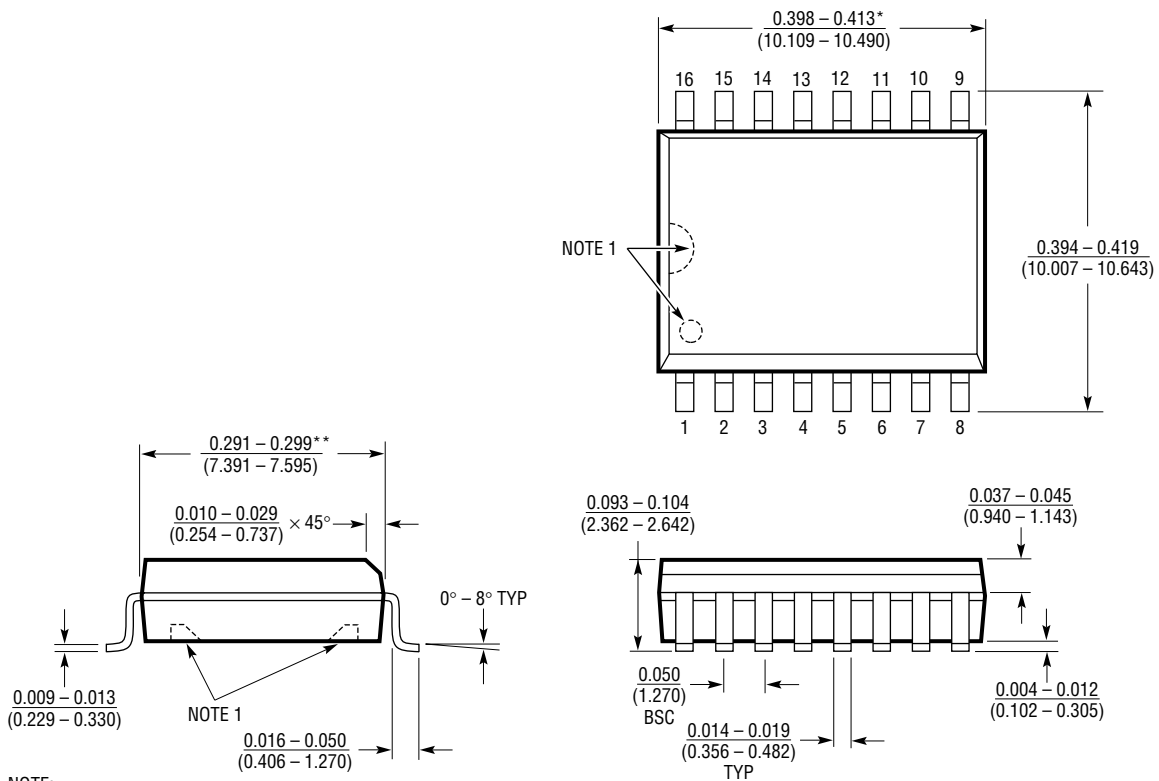


N18 1098



**PACKAGE DESCRIPTION**

**SW Package**  
**16-Lead Plastic Small Outline (Wide .300 Inch)**  
 (Reference LTC DWG # 05-08-1620)

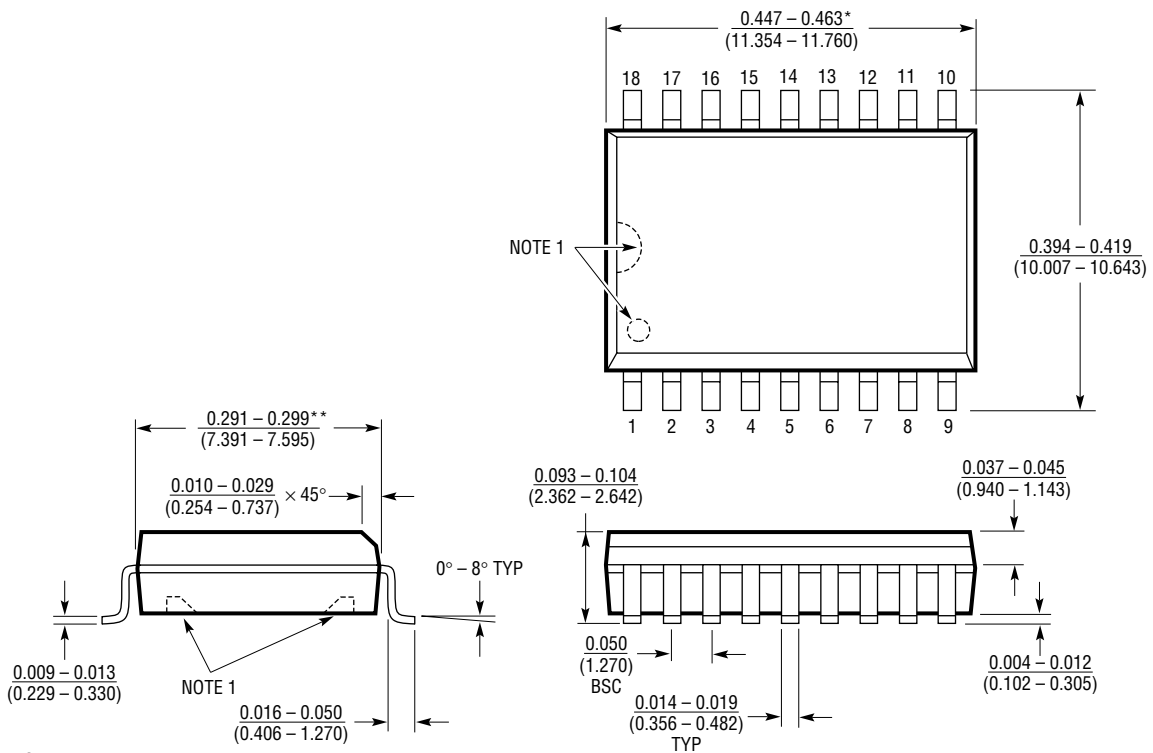


NOTE:  
 1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.  
 THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS  
 \*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S16 (WIDE) 1098

**PACKAGE DESCRIPTION**

**SW Package**  
**18-Lead Plastic Small Outline (Wide .300 Inch)**  
 (Reference LTC DWG # 05-08-1620)



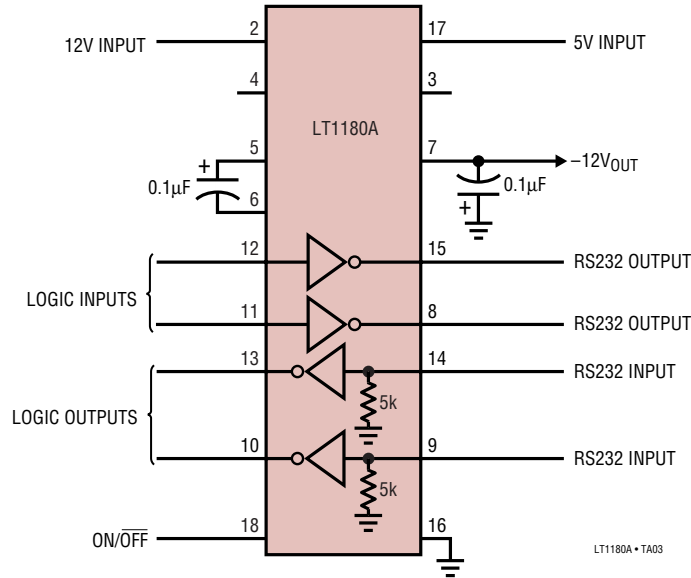
NOTE:  
 1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS  
 \*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S18 (WIDE) 1098

# LT1180A/LT1181A

## TYPICAL APPLICATION

Operation Using 5V and 12V Power Supplies



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1280A/LT1281A	5V 2-Driver/2-Receiver RS232 Transceivers	Pin Compatible with LT1180A/LT1181A, I <sub>CC</sub> = 10mA Max
LT1381	5V 2-Driver/2-Receiver RS232 Transceiver	Narrow 16-Pin SO Package
LT1780/LT1781	5V 2-Driver/2-Receiver RS232 Transceivers	IEC 1000-4-2 Level 4 Compliance