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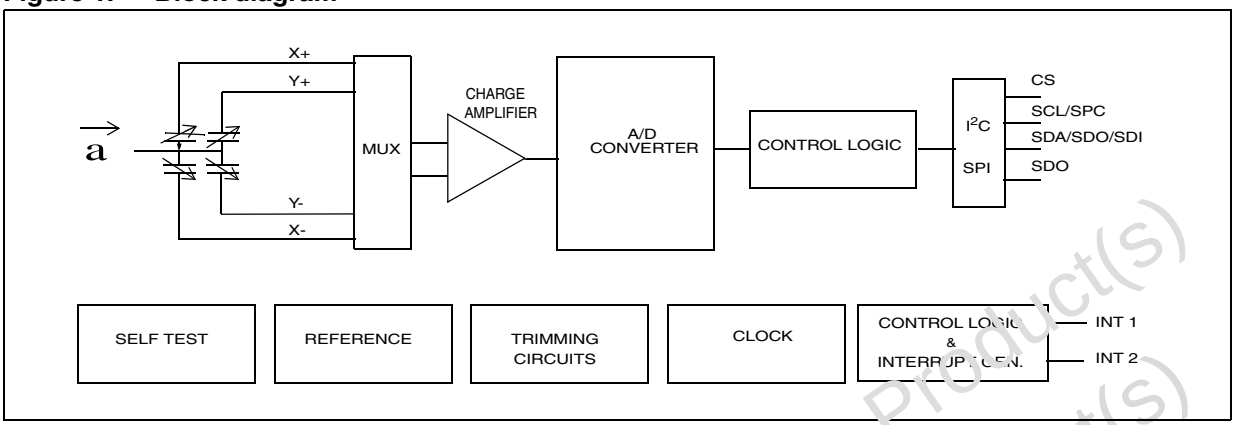
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection

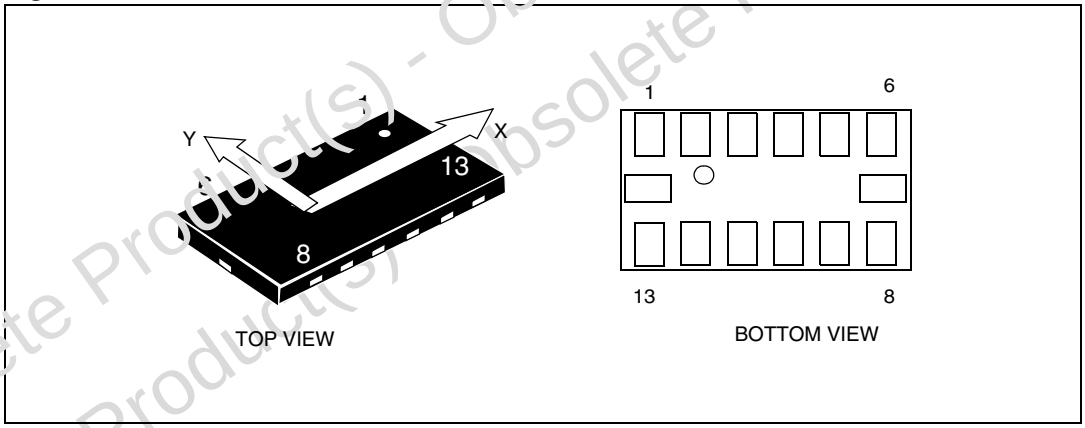


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	GND	0V supply
3	Reserved	Connect to Vdd
4	GND	0V supply
5	GND	0V supply
6	Vdd	Power supply
7	CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
8	INT 1	Inertial interrupt 1
9	INT 2	Inertial interrupt 2
10	GND	0V supply
11	Reserved	Connect to Gnd
12	SDO	SPI Serial Data Output I^2C less significant bit of the device address
13	SDA SDI SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
14	SCL SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

(All the parameters are specified @ Vdd=2.5 V, T = 25°C unless otherwise noted)

Table 3. Mechanical characteristics(1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range(3)	FS bit set to 0	±2.0	±2.3		g
		FS bit set to 1	±8.0	±9.2		
So	Sensitivity	FS bit set to 0	16.2	18	19.8	mg/digit
		FS bit set to 1	64.8	72	79.2	
TCSO	Sensitivity change vs temperature	FS bit set to 0		±0.01		%/°C
TyOff	Typical zero-g level offset accuracy(4),(5)	FS bit set to 0		±40		mg
		FS bit set to 1		±60		mg
TCOff	Zero-g level change vs temperature	Max delta from 25°C		±0.5		mg/°C
Vst	Self test output change(6),(7),(8)	FS bit set to 0 STP bit used X axis Vdd=2.16V to 3.6V	-32		-3	LSb
		FS bit set to 0 STP bit used Y axis Vdd=2.16V to 3.6V	3		32	LSb
BW	System bandwidth(9)			ODR/2		Hz
Top	Operating temperature range		-40		+85	°C
Wt	Product weight			30		mgram

1. The product is factory calibrated at 2.5V. The device can be used from 2.16 V to 3.6 V
2. Typical specifications are not guaranteed
3. Verified by wafer level test and measurement of initial offset and sensitivity
4. Typical zero-g level offset value after MSL3 preconditioning
5. Offset can be eliminated by enabling the built-in high pass filter
6. If STM bit is used values change in sign for all axes
7. Self Test output changes with the power supply. Self test “output change” is defined as $OUTPUT[LSb]_{(Self\text{-}test\ bit\ on\ ctrl\_reg1=1)}$ $-OUTPUT[LSb]_{(Self\text{-}test\ bit\ on\ ctrl\_reg1=0)}$. 1LSb=4.6g/256 at 8bit representation, ±2.3g Full-Scale
8. Output data reach 99% of final value after 3/ODR when enabling Self-Test mode due to device filtering
9. ODR is output data rate. Refer to table 3 for specifications

2.2 Electrical characteristics

(All the parameters are specified @ Vdd=2.5V, T= 25°C unless otherwise noted)

Table 4. Electrical characteristics(1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		2.16	2.5	3.6	V
Vdd_IO	I/O pins Supply voltage(3)		1.71		Vdd+0.1	V
Idd	Supply current	T = 25°C, ODR=100 Hz		0.3	0.4	mA
IddPdn	Current consumption in power-down mode	T = 25°C		1	5	µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
VOH	High level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
ODR	Output data rate	DR=0		100		Hz
		DR=1		400		
BW	System bandwidth(4)			ODR/2		Hz
Ton	Turn-on time(5)			3/ODR		s
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5 V. The device can be used from 2.16V to 3.6V
2. Typical specification are not guaranteed
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
4. Filter cut-off frequency
5. Time to obtain valid data after exiting Power-Down mode

2.3 Communication interface characteristics

2.3.1 SPI - Serial Peripheral Interface

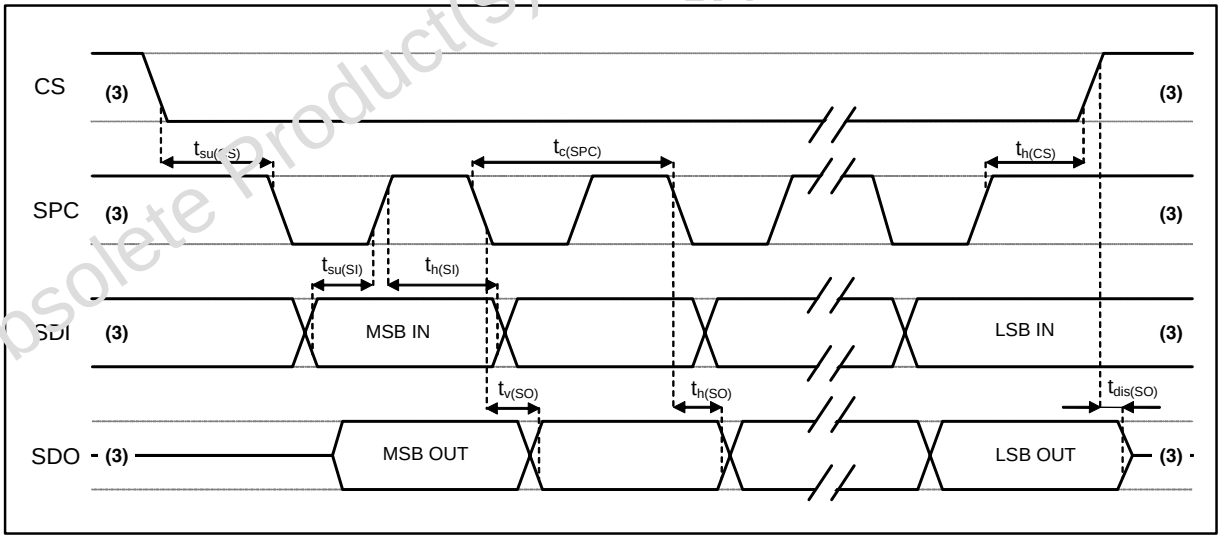
Subject to general operating conditions for Vdd and top.

Table 5. SPI Slave Timing Values

Symbol	Parameter	Value (1)		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	6		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI Slave Timing Diagram(a)



3. When no communication is on-going, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors

a. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both Input and Output port

2.3.2 I²C - Inter IC control interface

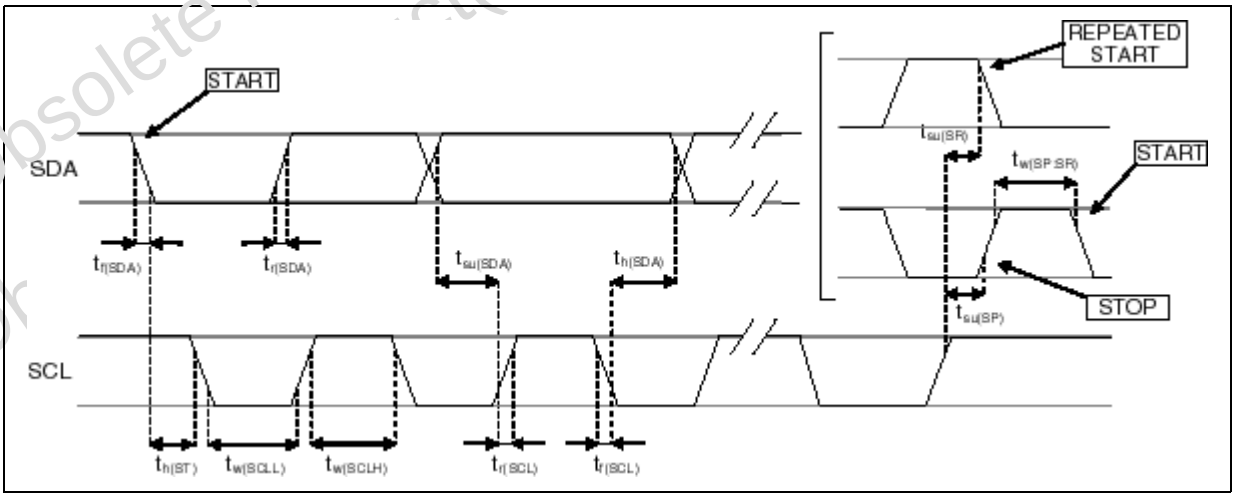
Subject to general operating conditions for Vdd and Top.

Table 6. I²C Slave Timing Values

Symbol	Parameter	I²C Standard mode (1)		I²C Fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	KHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45(2)	0	0.9(2)	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (3)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (3)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I2C protocol requirement, not tested in production
2. A device must internally provide an hold time of at least 300 ns for the SDA signal (referred to VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL
3. Cb = total capacitance of one bus line, in pF

Figure 4. I²C Slave Timing Diagram (b)



b. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both port

2.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum Value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vdd_IO	I/O pins supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd=2.5 V)	3000g for 0.5 ms	
		10000g for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)	3000g for 0.5 ms	
		10000g for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	4.0 (HBM)	kV
		200 (MM)	V
		1500 (CDM)	V

Note: Supply voltage on any pin should never exceed 6.0 V

	This is a Mechanical Shock sensitive device, improper handling can cause permanent damages to the part
	This is an ESD sensitive device, improper handling can cause permanent damages to the part

2.5 Terminology

2.5.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1g acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one and dividing the result by 2 leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The Sensitivity Tolerance describes the range of Sensitivities of a large population of sensors.

2.5.2 Zero-g level

Zero-g level Offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0g in X axis and 0g in Y axis. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-g offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-g level change vs. temperature". The Zero-g level tolerance (TyOff) describes the Standard Deviation of the range of Zero-g levels of a population of sensors.

2.5.3 Self test

Self Test allows to check the sensor functionality without moving it. The Self Test function is off when the self-test bit of ctrl_reg1 (control register 1) is programmed to '0'. When the self-test bit of ctrl_reg1 is programmed to '1' an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When Self Test is activated, the device output level is given by the algebric sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

2.5.4 Click and double click recognition

The click and double click recognition functions help to create man-machine interface with little software overload. The device can be configured to output an interrupt signal on dedicated pin when tapped in any direction.

For additional information contact your sales office.

3 Functionality

The LIS202DL is an ultracompact, low-power, digital output 2-axis linear accelerometer packaged in a LGA package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide a signal to the external world through an I^2C/SPI serial interface.

3.1 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady state the nominal value of the capacitors are few pF and when an acceleration is applied the maximum variation of the capacitive load is in pF range.

3.2 IC interface

The complete measurement chain is composed by a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage that is finally available to the user by analog-to-digital converters.

The acceleration data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS202DL features a Data-Ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in the digital system that uses the device.

The LIS202DL may also be configured to generate an inertial Wake-Up interrupt signal accordingly to a programmed acceleration event along the enabled axes.

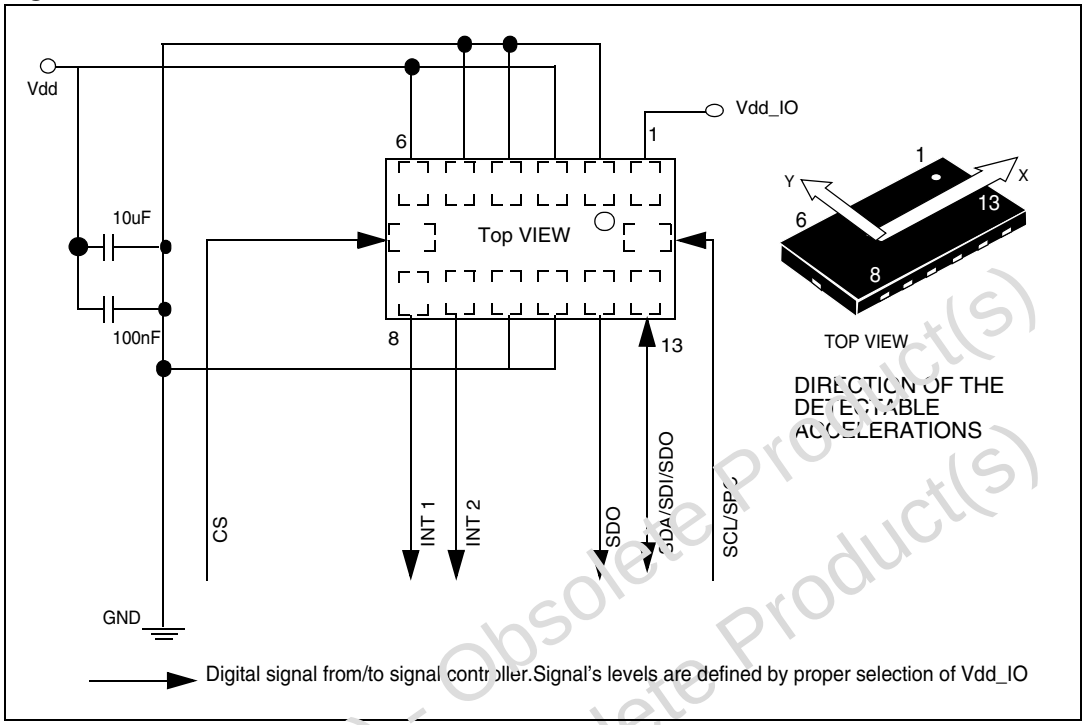
3.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-g level (TyOff).

The trimming values are stored inside the device in a non volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the normal operation. This allows to use the device without further calibration.

4 Application hints

Figure 5. LIS202DL electrical connection



The device core is supplied through Vdd line while the I/O pads are supplied through Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF Al) should be placed as near as possible to the pin 6 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (*Figure 5*). It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the I^2C/SPI interface.When using the I^2C, CS must be tied high while SDO must be left floating.

The functions, the threshold an the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user though the I^2C/SPI interface.

4.1 Soldering information

The LGA package is compliant with the ECOPACK, RoHS and "green" sta. Leave pin 1 indicator unconnected during soldering. Land pattern and soldering recommendation are available at www.st.com

5 Digital interfaces

The registers embedded inside the LIS202DL may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, CS line must be tied high (i.e connected to Vdd_IO).

Table 8. Serial interface pin description

PIn name	PIn description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO	SPI Serial Data Output (SDO)

5.1 I^2C serial interface

The LIS202DL I^2C is a bus slave. The I^2C is employed to write the data into the registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 9 Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the Serial Clock Line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd_IO through a pull-up resistor embedded inside the LIS202DL. When the bus is free both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as the normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated to the LIS202DL is 001110xb. **SDO** pad can be used to modify less significant bit of the device address. If SDO pad is connected to voltage supply LSb is '1' (address 0011101b) else if SDO pad is connected to ground LSb value is '0' (address 0011100b). This solution permits to connect and address two different accelerometer to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received.

The I²C embedded inside the LIS202DL behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a salve address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address will be transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is '0' (Write) the Master will transmit to the slave with direction unchanged. *Table 10* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	001110	0	1	00111001 (39h)
Write	001110	0	0	00111000 (38h)
Read	001110	1	1	00111011 (3Bh)
Write	001110	1	0	00111010 (3Ah)

Table 11. Transfer when master is writing one byte to slave:

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave:

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave:

Master	ST	SAD+W		SUB		SR	SAD+R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave:

Master	ST	SAD + W		SUB		SR	SAD + R			MAK
Slave			SAK		SAK			SAK	DATA	

Master		MAK		NMAK	SP
Slave	DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to read.

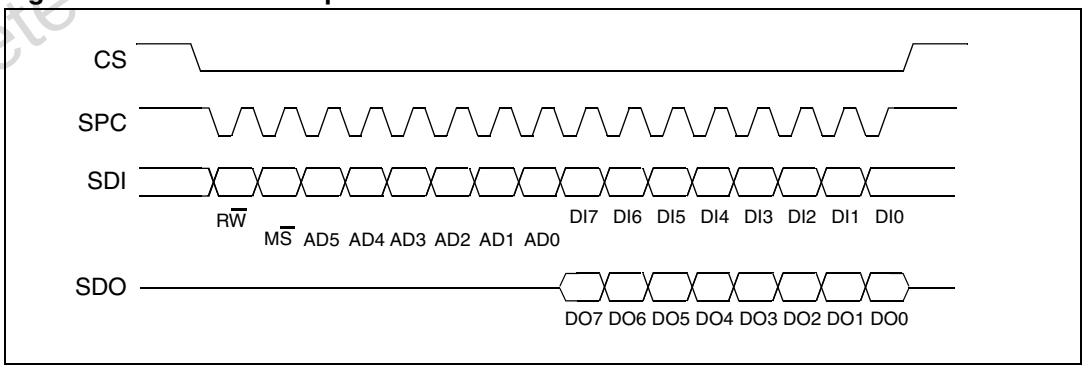
In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

5.2 SPI bus interface

The LIS202DL SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read & write protocol



CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple byte read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).

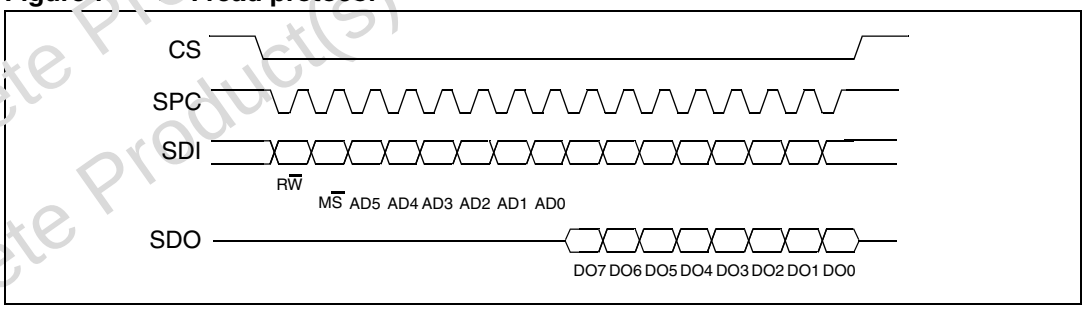
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When M$\overline{S}$ bit is 0 the address used to read/write data remains the same for every block. When M$\overline{S}$ bit is 1 the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 7. SPI read protocol



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

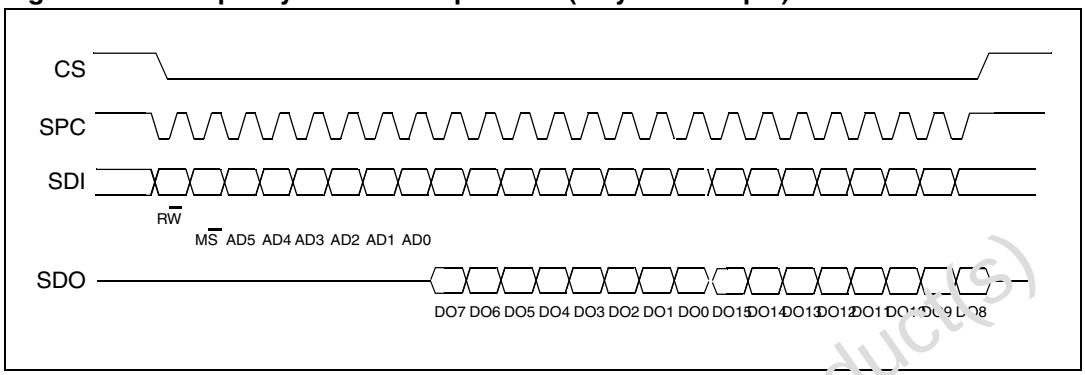
bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

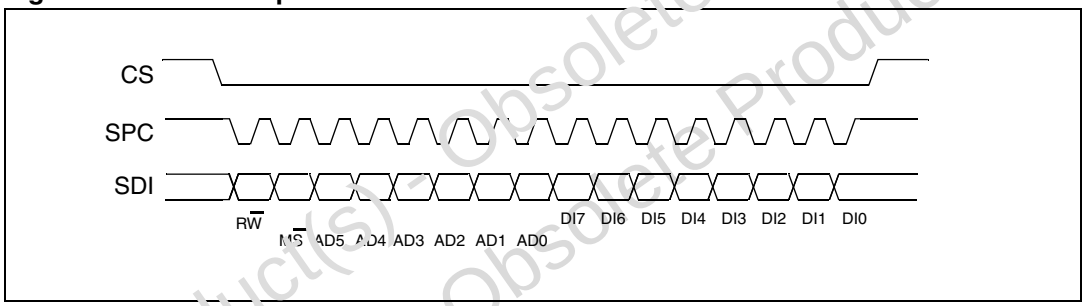
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 8. Multiple bytes SPI read protocol (2 bytes example)



5.2.2 SPI write

Figure 9. SPI write protocol



The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

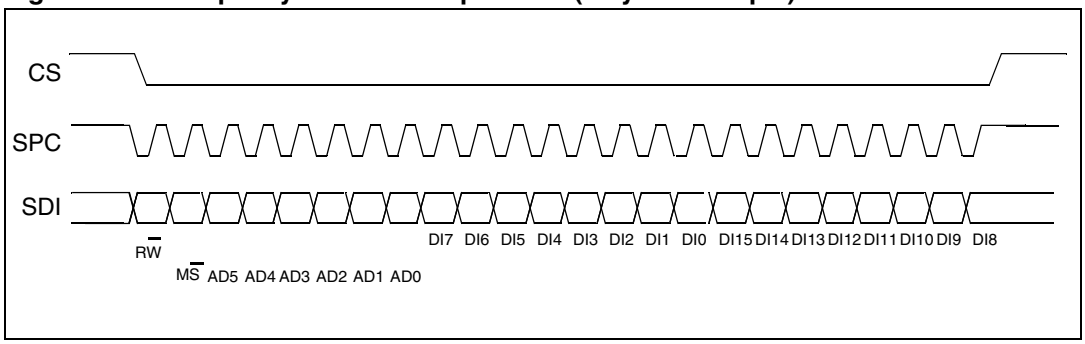
bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writing.

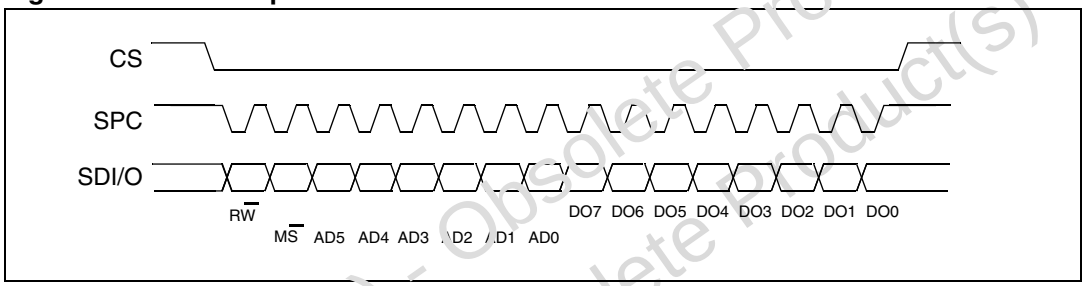
Figure 10. Multiple bytes SPI write protocol (2 bytes example)



5.2.3 SPI read in 3-wires mode

3-wires mode is entered by setting to 1 bit SIM (SPI Serial Interface Mode selection) in CTRL_REG2.

Figure 11. SPI read protocoin 3-wires model



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

6 Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related address:

Table 15. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)		00-0E			Reserved
Who_Am_I	r	0F	000 1111	00111011	Dummy register
Reserved (do not modify)		10-1F			Reserved
Ctrl_Reg1	rw	20	010 0000	00000111	
Ctrl_Reg2	rw	21	010 0001	00000000	
Ctrl_Reg3	rw	22	010 0010	00000000	
HP_filter_reset	r	23	010 0011	dummy	Dummy register
Reserved (do not modify)		24-26			Reserved
Status_Reg	r	27	010 0111	00000000	
--	r	28	010 1000		Not used
OutX	r	29	010 1001	output	
--	r	2A	010 1010		Not used
OutY	r	2B	010 1011	output	
--	r	2C	010 1100		Not used
--	r	2D	010 1101		Not used
Reserved (do not modify)		2E-2F			Reserved
WU_CFG_1	rw	30	011 0000	00000000	
WU_SRC_1(ack1)	r	31	011 0001	00000000	
WU_THS_1	rw	32	011 0010	00000000	
WU_DURATION_1	rw	33	011 0011	00000000	
WU_CFG_2	rw	34	011 0100	00000000	
WU_SRC_2 (ack2)	r	35	011 0101	00000000	
WU_THS_2	rw	36	011 0110	00000000	
WU_DURATION_2	rw	37	011 0111	00000000	
Reserved (do not modify)		38-3F			Reserved

Registers marked as Reserved must not be changed. The writing to those registers may cause permanent damages to the device. The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

7.1 WHO_AM_I (0Fh)

Table 16. Register (0Fh)

0	0	1	1	1	0	1	1

Device identification register.

This register contains the device identifier that for LIS202DL is set to 3Bh.

7.2 CTRL_REG1 (20h)

Table 17. Register (20h)

DR	PD	FS	STP	STM	0(1)	Yen	Xen

1. Bit to be set to "0" for correct device functionality

Table 18. Register description (20h)

DR	Data rate selection. Default value: 0 (0: 100 Hz output data rate; 1: 400 Hz output data rate)
PD	Power Down Control. Default value: 0 (0: power down mode; 1: active mode)
FS	Full scale selection. Default value: 0 (refer to *Table 3* for typical full scale value)
STP, STM	Self Test Enable. Default value: 00 (0: normal mode; 1: self test P, M enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR bit allows to select the data rate at which acceleration samples are produced. The default value is 0 which corresponds to a data-rate of 100 Hz. By changing the content of DR to "1" the selected data-rate will be set equal to 400 Hz.

PD bit allows to turn on the turn the device out of power-down mode. The device is in power-down mode when PD= "0" (default value after boot). The device is in normal mode when PD is set to 1.

STP, STM bits are used to activate the self test function. When the bit is set to one, an output change will occur to the device outputs (refer to *Table 3* and *Table 4* for specification) thus allowing to check the functionality of the whole measurement chain.

Yen bit enables the generation of Data Ready signal for Y-axis measurement channel when set to 1. The default value is 1.

Xen bit enables the generation of Data Ready signal for X-axis measurement channel when set to 1. The default value is 1.

7.3 CTRL_REG2 (21h)

Table 19. Register (21h)

SIM	BOOT	--	FDS	HP WU2	HP WU1	HP_coeff2	HP_coeff1

Table 20. Register description (21h)

SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FDS	Filtered Data Selection. Default value: 0 (0: internal filter bypassed, data from internal filter sent to output register)
HP WU2	High Pass filter enabled for WakeUp # 2. Default value: 0 (0: filter bypassed; 1: filter enabled)
HP WU1	High Pass filter enabled for Wake-Up #1. Default value: 0 (0: filter bypassed; 1: filter enabled)
HP coeff2 HP coeff1	High pass filter cut-off frequency configuration. Default value: 00 (See table below)

SIM bit selects the SPI Serial Interface Mode. When SIM is '0' (default value) the 4-wire interface mode is selected. The data coming from the device are sent to SDO pad. In 3-wire interface mode output data are sent to SDA_SDI pad.

BOOT bit is used to refresh the content of internal registers stored in the flash memory block. At the device power up the content of the flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason the content of trimming registers was changed it is sufficient to use this bit to restore correct values. When BOOT bit is set to '1' the content of internal flash is copied inside corresponding internal registers and it is used to calibrate the device. These values are factory trimmed and they are different for every accelerometer. They permit a good behavior of the device and normally they have not to be changed. At the end of the boot process the BOOT bit is set again to '0'.

FDS bit enables (FDS=1) or bypass (FDS=0) the high pass filter in the signal chain of the sensor

HP_coeff[2:1]. These bits are used to configure high-pass filter cut-off frequency ft.

Table 21. Truth table (21h)

HPcoeff2,1	ft (Hz) (ODR=100 Hz)	ft (Hz) (ODR=400 Hz)
00	2	8
01	1	4
10	0.5	2
11	0.25	1

7.4 CTRL_REG3 [Interrupt CTRL register] (22h)

Table 22. Register (22h)

IHL	PP_OD	I2CFG2	I2CFG1	I2CFG0	I1CFG2	I1CFG1	I1CFG0

Table 23. Register description (22h)

IHL	Interrupt active high, low. Default value 0. (0: active high; 1: active low)
PP_OD	Push-pull/Open Drain selection on interrupt pad. Default value 0. (0: push-pull; 1: open drain)
I2CFG2 I2CFG1 I2CFG0	Data Signal on Int2 pad control bits. Default value 000. (see table below)
I1CFG2 I1CFG1 I1CFG0	Data Signal on Int1 pad control bits. Default value 000. (see table below)

Table 24. Truth table (22h)(1)

I1(2)_CFG2	I1(2)_CFG1	I1(2)_CFG0	Int1(2) Pad
0	0	0	GND
0	0	1	WU_1
0	1	0	WU_2
0	1	1	WU_1 or WU_2
1	0	0	Data ready

1. These are the allowed bit configurations. Each other configuration may cause incorrect device functionality

7.5 HP_FILTER_RESET (23h)

Dummy register. Reading at this address zeroes instantaneously the content of the internal high pass-filter. If the high pass filter is enabled all two axes are instantaneously set to 0g. This allows to overcome the settling time of the high pass filter.

7.6 STATUS_REG (27h)

Table 25. Register (27h)

XYOR	--	YOR	XOR	YXDA	--	YDA	XDA

Table 26. Register description (27h)

YXOR	X, Y axis Data Overrun. Default value: 0 (0: no overrun has occurred; 1: new data has over written the previous one before it was read)
YOR	Y axis Data Overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)
XOR	X axis Data Overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)
YXDA	X, Y axis new Data Available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
YDA	Y axis new Data Available. Default value: 0 (0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available)
XDA	X axis new Data Available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

7.7 OUT_X (29h)

Table 27. Register (29h)

XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

X axis output data.

7.8 OUT_Y (2Bh)

Table 28. Register (2Bh)

YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0

Y axis output data.

7.9 WU_CFG_1 (30h)

Table 29. Register (30h)

AOI	LIR	res_1	res_2	YHIE	YLIE	XHIE	XLIE

Table 30. Register description (30h)

AOI	And/Or combination of Interrupt events. Default value: 0 (0: OR combination of interrupt events; 1: AND combination of interrupt events)
LIR	Latch Interrupt request into WU_SRC_1 reg with the WU_SRC_1 reg cleared by reading WU_SRC_1 reg. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
res_1	Reserved at Value: 0. Value should not be changed.
res_2	Reserved at Value: 0. Value should not be changed.
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

7.10 WU_SRC_1 (31h)

Table 31. Register (31h)

--	IA	--	--	YH	YL	XH	XL

Table 32. Register description (31h)

IA	Interrupt Active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
YH	Y High. Default value: 0 (0: no interrupt, 1: YH event has occurred)
YL	Y Low. Default value: 0 (0: no interrupt, 1: YL event has occurred)

Table 32. Register description (31h)

XH	X High. Default value: 0 (0: no interrupt, 1: XH event has occurred)
XL	X Low. Default value: 0 (0: no interrupt, 1: XL event has occurred)

Wake-up source register. Read only register.

Reading at this address clears WU_SRC_1 register and the WU 1 interrupt and allows the refreshment of data in the SRC_1 register if the latched option was chosen.

7.11 WU_THS_1 (32h)

Table 33. Register (32h)

DCRM	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 34. Register description (32h)

DCRM	Resetting mode selection. Default value: 0 (0: counter reset; 1: counter decremented)
THS6, THS0	Wake-up Threshold: default value: 000 0000

Most significant bit (DCRM) is used to select the resetting mode of the duration counter. If DCRM=0 counter is reset when the interrupt is no more active else if DCRM=1 duration counter is decremented.

7.12 WU_DURATION_1 (33h)

Table 35. Register (33h)

D7	D6	D5	D4	D3	D2	D1	D0

Table 36. Register description (33h)

D7-D0	Duration value. Default value: 0000 0000

Duration register for Wake-Up interrupt 1. Duration step and maximum value depend on the ODR chosen. Step 2.5 msec, from 0 to 637.5 msec if ODR=400 Hz, else step 10 msec, from 0 to 2.55 sec when ODR=100 Hz. The counter used to implement duration function is blocked when LIR=1 in configuration register and the interrupt event is verified

7.13 WU_CFG_2 (34h)

Table 37. Register (34h)

AOI	LIR	res_1	res_2	YHIE	YLIE	XHIE	XLIE

Table 38. Register description (34h)

AOI	And/Or combination of Interrupt events. Default value: 0 (0: OR combination of interrupt events; 1: AND combination of interrupt events)
LIR	Latch Interrupt request into WU_SRC_2 reg with the WU_SRC_2 reg cleared by reading WU_SRC_2 reg. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
res_1	Reserved at Value: 0. Value should not be changed.
res_2	Reserved at Value: 0. Value should not be changed.
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

7.14 WU_SRC_2 (35h)

Table 39. Register (35h)

--	IA	--	--	YH	YL	XH	XL

Table 40. Register description (35h)

IA	Interrupt Active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
YH	Y High. Default value: 0 (0: no interrupt; 1: YH event has occurred)
YL	Y Low. Default value: 0 (0: no interrupt; 1: YL event has occurred)
XH	X High. Default value: 0 (0: no interrupt; 1: XH event has occurred)
XL	X Low. Default value: 0 (0: no interrupt; 1: XL event has occurred)

Wake-up source register. Read only register.

Reading at this address clears WU_SRC_2 register and the WU_2 interrupt and allows the refreshment of data in the WU_SRC_2 register if the latched option was chosen.

7.15 WU_THS_2 (36h)

Table 41. Register (36h)

DCRM	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 42. Register description (36h)

DCRM	Resetting mode selection. Default value: 0 (0: counter reset; 1: counter decrements)
THS6, THS0	Wake-up Threshold. Default value: 000 0000

Most significant bit (DCRM) is used to select the resetting mode of the duration counter. If DCRM=0 counter is reset when the interrupt is no more active else if DCRM=1 duration counter is decremented.

7.16 WU_DURATION_2 (37h)

Table 43. Register (37h)

D7	D6	D5	D4	D3	D2	D1	D0

Table 44. Register description (37h)

D7-D0	Duration value. Default value: 0000 0000

Duration register for Wake-Up interrupt 2. Duration step and maximum value depend on the ODR chosen. Step 2.5 msec, from 0 to 637.5 msec if ODR=400 Hz, else step 10 msec, from 0 to 2.55 sec when ODR=100 Hz. The counter used to implement duration function is blocked when LIR=1 in configuration register and the interrupt event is verified.

8 Typical performance characteristics

8.1 Mechanical characteristics at 25°C

Figure 12. X axis Zero-g level at 2.5 V

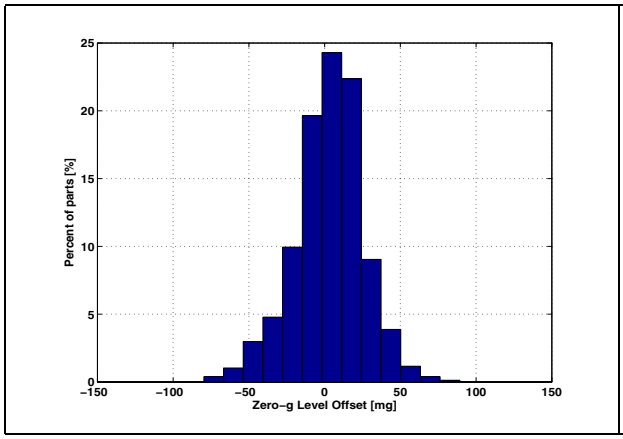


Figure 13. X axis sensitivity at 2.5 V

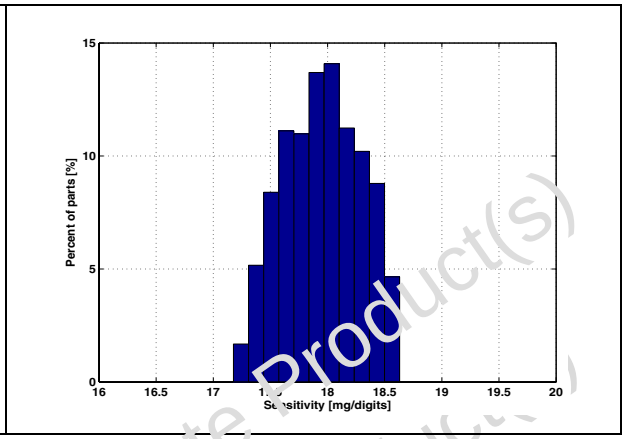


Figure 14. Y axis Zero-g level at 2.5 V

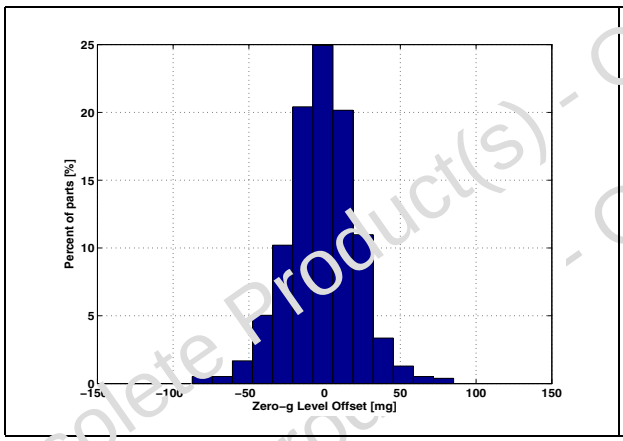
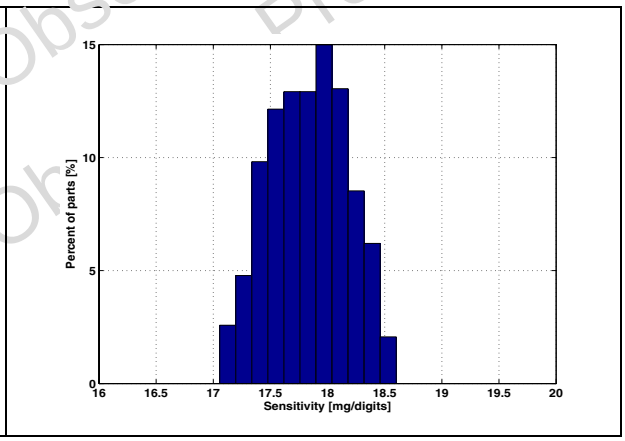


Figure 15. Y axis sensitivity at 2.5 V



8.2 Mechanical characteristics derived from measurement in the -40°C to +85°C temperature range

Figure 16. X axis Zero-g level change vs. temperature at 2.5 V

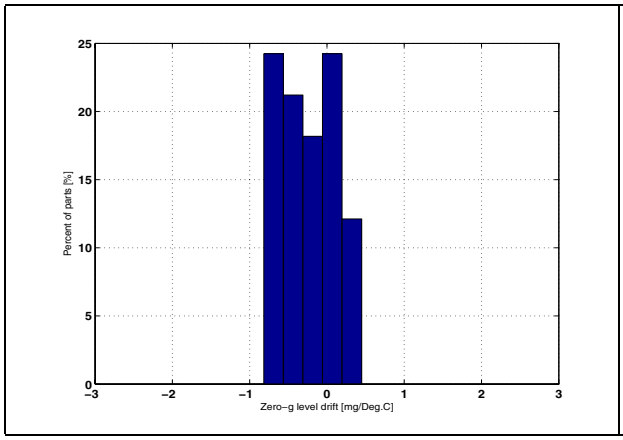


Figure 17. X axis sensitivity change vs. temperature at 2.5 V

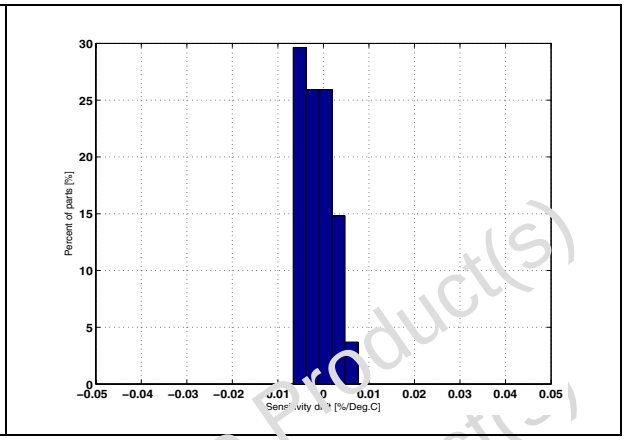


Figure 18. Y axis Zero-g level change vs. temperature at 2.5 V

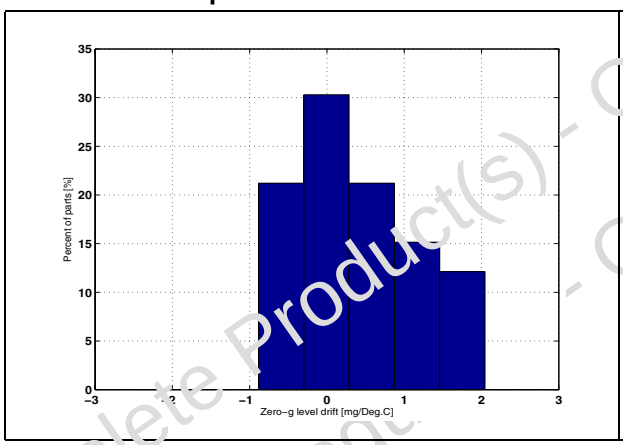
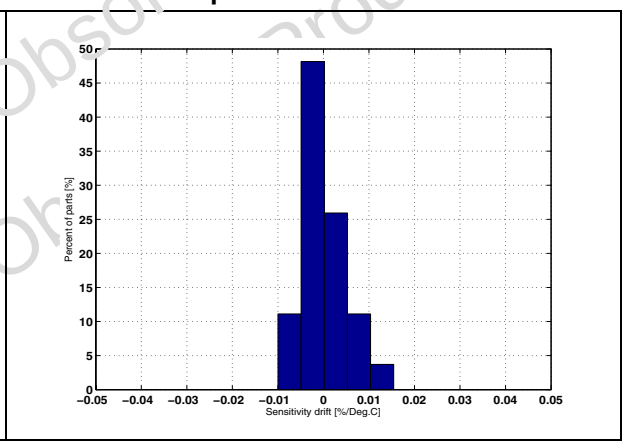


Figure 19. Y axis sensitivity change vs. temperature at 2.5 V



8.3 Electro-mechanical characteristics at 25°C

Figure 20. Current consumption in normal mode at 2.5 V

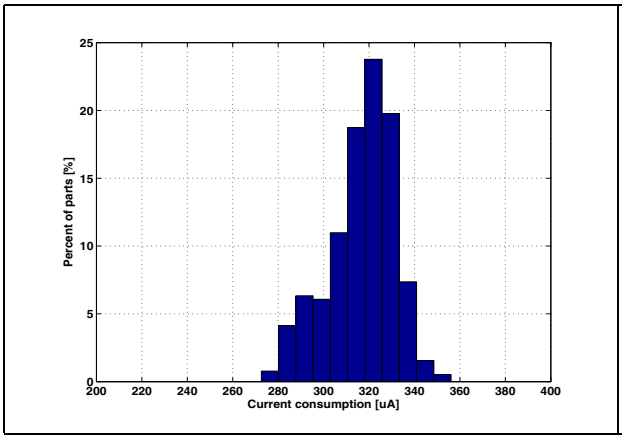
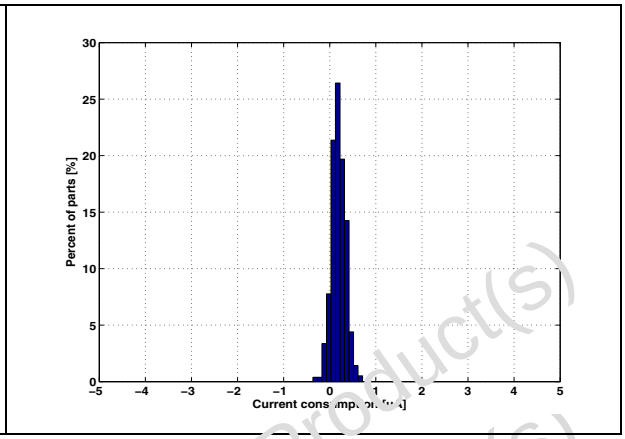


Figure 21. Current consumption in power down mode at 2.5 V



9 Package information

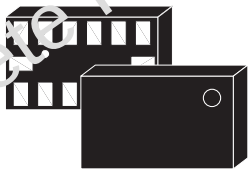
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

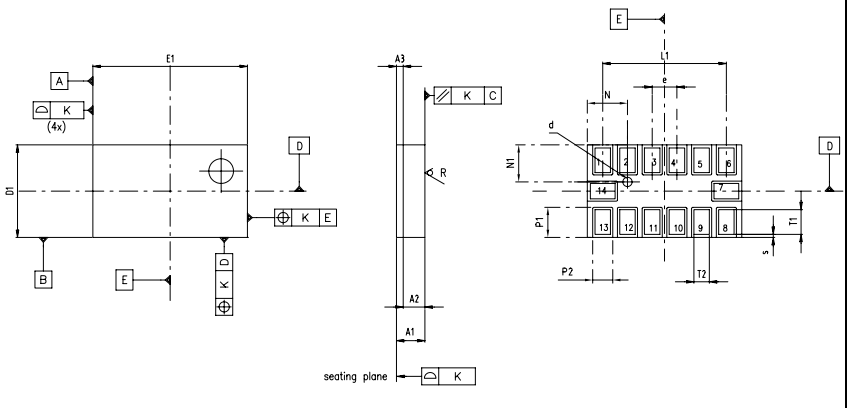
Figure 22. LGA 14: mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1		0.920	1.000		0.0362	0.0394
A2			0.700			0.0275
A3	0.180	0.220	0.260	0.0071	0.0087	0.0102
D1	2.850	3.000	3.150	0.1122	0.1181	0.1240
E1	4.850	5.000	5.150	0.1909	0.1968	0.2027
e		0.800			0.0315	
d		0.300			0.0118	
L1		4.000			0.1575	
N		1.360			0.0535	
N1		1.200			0.0472	
P1	0.965	0.975	0.985	0.0380	0.0384	0.0386
P2	0.640	0.650	0.660	0.0252	0.0256	0.0260
T1	0.750	0.800	0.850	0.0295	0.0315	0.0335
T2	0.450	0.500	0.550	0.0177	0.0197	0.0217
R	1.200		1.600	0.0472		0.0630
h		0.150			0.0059	
k		0.050			0.0020	
i		0.100			0.0039	
s		0.100			0.0039	

OUTLINE AND MECHANICAL DATA



LGA14 (3x5x0.92mm) Pitch 0.8mm
Land **G**rid **A**rray **P**ackage



10 Revision history

Table 45. Document revision history

Date	Revision	Changes
11-Jun-2007	1	Initial release.
13-Dec-2007	2	Inserted new *Section 2.3: Communication interface characteristics* Content reworked to improve readability.

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