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PRODUCT DESCRIPTION

The Le9500 device is optimized to provide battery feed, ringing, and supervision on short Plain Old Telephone Service (POTS) loops. This device provides power ringing to the subscriber loop through amplification of a low-voltage input. It also provides forward and reverse battery feed states, on-hook transmission, a low-power scan state, ground start (tip open), and a forward disconnect state.

The Le9500 device requires a 3.3V V_{CC} and battery to operate eight operating states. A battery switch is included to allow for use of a lower-voltage battery in the off-hook condition, thus minimizing short-loop off-hook power.

The following two batteries are used:

1. A high-voltage operation and ringing battery (V_{BAT1}):
   V_{BAT1} is used for scan, on-hook transmission, ground start, and power ringing. It can be a maximum of –75 V for Le9500A, –85 V for Le9500B, or –100V for Le9500C and Le9500D.

   For Le9500D during ringing only this voltage may be extended to –145 V. The supply has to be externally adjustable. It has to be adjusted back to no more than -100 V for other operation states. Further, when –145 V is used for ringing special care should be applied to prevent certain faults from happening such as tip to ring, tip or ring to ground.
2. A lower-voltage talk battery (V_{BAT2}):
   V_{BAT2} is used for active state powering.

Loop closure, ring trip, and ground start detection is available. The loop closure detector has fixed threshold with hysteresis. The ring trip detector requires a single-pole filter, thus minimizing external components required. The ring trip threshold at a given battery voltage is fixed and with hysteresis. Ground start detection also has fixed threshold with hysteresis.

The DC current limit is set and fixed by a logic-controllable pin. Ground or open applied to this pin sets the current limit at the low or high value.

This device is designed for ultra-low power in all operating states.

Forward and reverse battery active states are used for off-hook conditions. Since this device is designed for short-loop applications, the lower-voltage V_{BAT2} is applied during the forward and reverse active states. Battery reversal is quiet, without breaking the AC path. Rate of battery reversal may be ramped to control switching time.

The magnitude of the overhead voltage in the forward and reverse active states has a typical default value of 7.2 V, allowing for an on-hook transmission of an undistorted signal of 3.14 dBm into 900 Ω. Additionally, this allows sufficient overhead for 500 mV of meter pulse if desired. This overhead is fixed. The ring trip detector is turned off during active states to conserve power.

Because on-hook transmission is not allowed in the scan state, an on-hook transmission state is defined. This state is functionally similar to the active state, except the tip ring voltage is derived from the higher V_{BAT1} rather than V_{BAT2}.

In the on-hook transmission states with a primary battery whose magnitude is greater than a nominal 56.5 V, the magnitude of the tip-to-ground and ring-to-ground voltage is clamped at less than 56.5 V.

To minimize on-hook power, a low-power scan state is available. In this state, all functions except off-hook supervision are turned off to conserve power. On-hook transmission is not allowed in the scan state.

In the scan state with a primary battery whose magnitude is greater than a nominal 56.5 V, the magnitude of the tip-to-ground and ring-to-ground voltage is clamped at less than 56.5 V.

A forward disconnect state is provided, where all circuits are turned off and power is denied to the loop.

The device offers a ring state, in which a power ring signal is provided to the tip/ring pair. During the ring state, user-supplied low-voltage ring signals are input to the device's $RING_{INP/N}$ inputs. The input signals can be differential or single-ended, and can either or both include certain DC offset. Both inputs should reference to Vref. The two signals are amplified to produce the power ring signal. The input signal or signals may be a sine wave or filtered square wave to produce a sine wave or trapezoidal output. The Ring Trip detector is active during the ring state. The flexibility makes the device ideal to directly interface to DOCSIS compliant cable modem gateway products.

This feature eliminates the need for a separate external ring relay, associated external circuitry, and a bulk ringing generator.

The device offers a ground start state. In this state, the tip drive amplifier is turned off. The device presents a high impedance (>100 kΩ) to PT and a current-limited battery (V_{BAT1}) to PR. The voltage on PR is clamped to be less than 56.5 V in magnitude. The NSTAT loop current detector is used for ring ground detection. In the ground start state, since the loop current is common state, the loop closure threshold is reduced in half, thus maintaining loop supervision at specified levels.

Upon reaching the thermal shutdown temperature, the device will enter an all off state. Upon cooling, the device will re-enter the state it was in prior to thermal shutdown. Hysteresis is built in to prevent oscillation.

Data control is via a parallel unlatched control scheme.

Circuitry is added to the Le9500 device to minimize the inrush of current from the V_{CC} supply and to the battery supply during an on- to off-hook transition, thus saving in power supply design cost.

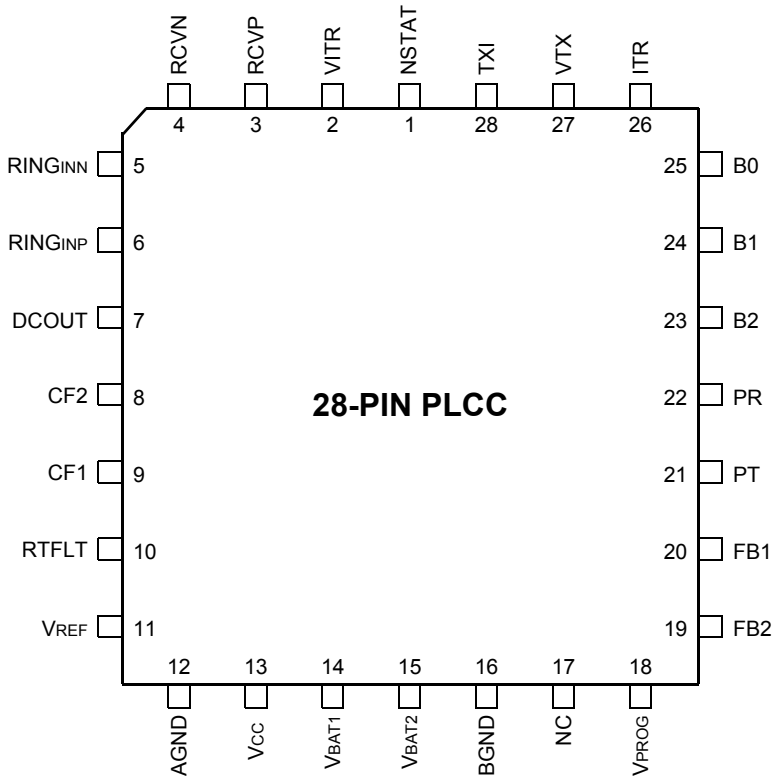
The Le9500 device uses a voltage feed-current sense architecture. The transmit gain is a transimpedance. The Le9500 device transimpedance is set via a single external resistor, and this device is designed for optimal performance with a transimpedance set at 300 V/A. This interface is single ended. The Le9500 device offers a differential receive interface with a gain of 8.

The Le9500 device is internally referenced to 1.5 V. This reference voltage is output at the V_{REF} pin of the device. The VITR output is also referenced to 1.5 V. The RCVP/RCVN receive inputs are floating inputs.

The Le9500 device is available in a 28-pin PLCC package.

CONNECTION DIAGRAM

Figure 1. Le9500 28-Pin PLCC Connection Diagram



PIN DESCRIPTIONS

Pin Name	Type	Description
NSTAT	Output	**Loop Closure Detector Output—Ring Trip Detector Output.** When Low, this logic output indicates that an off-hook condition exists or ringing is tripped or a ring ground has occurred.
VITR	Output	**Transmit AC Output Voltage.** Output of internal AAC amplifier. This output is a voltage that is directly proportional to the differential AC tip/ring current.
RCVP	Input	**Receive AC Signal Input (Non inverting).** This high-impedance input controls to AC differential voltage on tip and ring. This node is a floating input.
RCVN	Input	**Receive AC Signal Input (Inverting).** This high-impedance input controls to AC differential voltage on tip and ring. This node is a floating input.
$RING_{INN}$	Input	**Power Ring Signal Input.** Couple to a sine wave or lower crest factor low-voltage ring signal. The input here is amplified to provide the full power ring signal at tip and ring. This signal may be applied continuously, even during nonringing states.
$RING_{INP}$	Input	**Power Ring Signal Input.** Couple to a sine wave or lower crest factor low-voltage ring signal. The input here is amplified to provide the full power ring signal at tip and ring. This signal may be applied continuously, even during nonringing states.
DCOUT	Output	**DC Output Voltage.** This output is a voltage that is directly proportional to the absolute value of the differential tip/ring current. This is used to set ring trip threshold.
CF2	—	**Filter Capacitor.** Connect a capacitor from this node to ground.
CF1	—	**Filter Capacitor.** Connect a capacitor from this node to CF2.
RTFLT	—	**Ring Trip Filter.** Connect this lead to DCOUT via a resistor and to AGND with a capacitor to filter the ring trip circuit to prevent spurious responses. A single-pole filter is needed.
V_{REF}	Output	**SLIC Device Internal Reference Voltage.** Output of internal 1.5 V reference voltage.
AGND	Ground	**Analog Signal Ground**.
V_{CC}	Power	**Analog Power Supply.** 3.3 V typical.
V_{BAT1}	Power	**Battery Supply 1.** High-voltage battery.
V_{BAT2}	Power	**Battery Supply 2.** Lower-voltage battery.
BGND	Ground	**Battery Ground.** Ground return for the battery supplies.
NC	—	**No Connection**.
V_{PROG}	Input	**Current-Limit Program Input.** Connect this pin to ground to set current limit to 25 mA; leave this pin open to set current limit to 40 mA.
FB2	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node for controlling rate of battery reversal. If ramped battery reversal is not desired, leave this pin floating.
FB1	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node for controlling rate of battery reversal. If ramped battery reversal is not desired, leave this pin floating.
PT	I/O	**Protected Tip.** The output drive of the tip amplifier and input to the loop-sensing circuit. Connect to loop through overvoltage and overcurrent protection.
PR	I/O	**Protected Ring.** The output drive of the ring amplifier and input to the loop sensing circuit. Connect to loop through overvoltage and overcurrent protection.
B2	Input	**State Control Input.** These pins have an internal 150 kΩ pull-up.
B1	Input	**State Control Input.** These pins have an internal 150 kΩ pull-up.
B0	Input	**State Control Input.** These pins have an internal 150 kΩ pull-up.
ITR	Input	**Transmit Gain.** Input to AX amplifier. Connect a 4.75 kΩ resistor from this node to VTX to set transmit gain. Gain shaping for termination impedance with a first-generation codec is also achieved with a network from this node to VTX.
VTX	Output	**AC Output Voltage.** Output of internal AX amplifier. The voltage at this pin is directly proportional to the differential tip/ring current.
TXI	Input	**AC/DC Separation.** Input to internal AAC amplifier. Connect a capacitor from this pin to VTX.

ABSOLUTE MAXIMUM RATINGS

(at T_A = 25 °C)

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Unit
DC Supply (V_{CC})	V_{CC}	–0.5	4.0	V
Battery Supply (V_{BAT1}) (Le9500A)	V_{BAT1}	BGND	–80	V
Battery Supply (V_{BAT1}) (Le9500B)	V_{BAT1}	BGND	–90	V
Battery Supply (V_{BAT1}) (Le9500C)	V_{BAT1}	BGND	–110	V
Battery Supply (V_{BAT1}) (Le9500D Non-Ringing)	V_{BAT1}	BGND	–110	V
Battery Supply (V_{BAT1}) (Le9500D Ringing)	V_{BAT1}	BGND	–155 + V_{CC}	V
Battery Supply (V_{BAT2})	V_{BAT2}	BGND	V_{BAT1}	V
Logic Input Voltage	—	–0.5	V_{CC} + 0.5	V
Logic Output Voltage	—	–0.5	V_{CC} + 0.5	V
Operating Temperature Range	—	–40	125	°C
Storage Temperature Range	—	–40	150	°C
Relative Humidity Range	—	5	95	%
PT or PR Fault Voltage (DC)	V_{PT}, V_{PR}	V_{BAT1} – 5	3	V
PT or PR Fault Voltage (10 x 1000 µs)	V_{PT}, V_{PR}	V_{BAT1} – 15	15	V
Ground Potential Difference (BGND to AGND)	—	—	±1	V
ESD Immunity (Human Body Model)	—	—	JESD22 Class 1C compliant	

Note: Continuous operation above 145ºC junction temperature may degrade device reliability.

Package Assembly

Green package devices are assembled with enhanced environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Environmental Ranges

Zarlink guarantees the performance of this device over commercial (0 to 70º C) and industrial (-40 to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Ambient Temperature	–40° C < T_A < +85° C
Ambient Relative Humidity	5 to 95%

Electrical Ranges

Parameter	Min	Typ	Max	Unit
3.3 V DC Supplies (V_{CC})	3.13	3.3	3.47	V
High Office Battery Supply (V_{BAT1}) (Le9500A)	–60	–	–75	V
High Office Battery Supply (V_{BAT1}) (Le9500B)	–60	–	–85	V
High Office Battery Supply (V_{BAT1}) (Le9500C)	–60	–	–100	V
High Office Battery Supply (V_{BAT1}) (Le9500D)	–60	–	–100	V
High Office Battery Supply (V_{BAT1}) (Le9500D) (during ringing only)	–60	–	–145	V
Auxiliary Office Battery Supply (V_{BAT2})	–12	–	V_{BAT1} ($\lvert V_{BAT1}\rvert$<=100)	V

Thermal Characteristics

Parameter	Min	Typ	Max	Unit
Thermal Protection Shutdown (Tjc)[1]	175	190	—	°C
28 PLCC Thermal Resistance Junction to Ambient (θJA)[1, 2]:				
Natural Convection 2S2P Board	—	35.5	—	°C/W
Natural Convection 2S0P Board	—	50.5	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S2P Board	—	31.5	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S0P Board	—	42.5	—	°C/W

1. *This parameter is not tested in production. It is guaranteed by design and device characterization.*
2. *Airflow, PCB board layers, and other factors can greatly affect this parameter.*

ELECTRICAL CHARACTERISTICS

Supply Currents

Unless otherwise specified, **V_{BAT1}** = –75 V for Le9500A; **V_{BAT1}** = –85 V for Le9500B; **V_{BAT1}** = –100 V for Le9500C and Le9500D; **V_{BAT2}** = –21 V, Vcc = 3.3 V.

Parameter	Min	Typ	Max	Unit
Scan state; no loop current:				
I_{VCC}	—	3.2	4.4	mA
I_{VBAT1}	—	0.25	0.44	mA
I_{VBAT2}	—	1	6	µA
Forward/reverse active; no loop current, with or without PPM, V_{BAT2} applied:				
I_{VCC}	—	4.6	5.8	mA
I_{VBAT1}	—	23	85	µA
I_{VBAT2}	—	1.0	1.4	mA
On-hook transmission state; no loop current, with or without PPM, V_{BAT1} applied:				
I_{VCC}	—	4.7	6.2	mA
I_{VBAT1}	—	1.4	1.9	mA
I_{VBAT2}	—	1	6	µA
Disconnect state:				
I_{VCC}	—	1.8	2.8	mA
I_{VBAT1}	—	0	110	µA
I_{VBAT2}	—	1	25	µA
Ground start state, no loop current:				
I_{VCC}	—	3.2	—	mA
I_{VBAT1}	—	0.25	—	mA
I_{VBAT2}	—	1	—	µA
Ring state; no load (V_{BAT1}= –145V for Le9500D):				
I_{VCC}	—	4.9	6.5	mA
I_{VBAT1}	—	2	2.8	mA
I_{VBAT2}	—	1	6	µA

Power Dissipation

V_{BAT2} = –21V, V_{CC}=3.3V.

Parameter	Min	Typ	Max	Unit
Le9500A (V_{BAT1} = –75 V)				
Scan state; no loop current	—	29	45	mW
Forward/reverse active; no loop current, V_{BAT2} applied	—	38	53	
On-hook transmission state; no loop current, V_{BAT1} applied	—	111	151	
Disconnect state	—	6	15	
Ground start state	—	29	—	
Ring state; no load	—	150	200	
Le9500B (V_{BAT1} = –85 V)				
Scan state; no loop current	—	32	50	mW
Forward/reverse active; no loop current, V_{BAT2} applied	—	38	54	
On-hook transmission state; no loop current, V_{BAT1} applied	—	127	182	
Disconnect state	—	6	17	
Ground start state	—	32	—	
Ring state; no load	—	171	235	
Le9500C (V_{BAT1} = –100 V)				
Scan state; no loop current	—	36	58	mW
Forward/reverse active; no loop current, V_{BAT2} applied	—	38	56	
On-hook transmission state; no loop current, V_{BAT1} applied	—	154	215	
Disconnect state	—	6	20	
Ground start state	—	35	—	
Ring state; no load	—	204	280	
Le9500D (V_{BAT1} = –100 V; V_{BAT1} = –145 V during ringing only)				
Scan state; no loop current	—	36	58	mW
Forward/reverse active; no loop current, V_{BAT2} applied	—	38	56	
On-hook transmission state; no loop current, V_{BAT1} applied	—	154	215	
Disconnect state	—	6	20	
Ground start state	—	35	—	
Ring state; no load[1]	—	324	435	

1. *Tested at -100 V V_{BAT1} in production with proportioned limits*

LINE CHARACTERISTICS

Unless otherwise specified, the test conditions are as specified in Figure 2, on page 14.

Typical values are characteristic of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not a part of the testing requirements. Minimum and maximum values apply across the operating temperature range and the entire battery range unless otherwise specified. Typical is defined as T_A=25° C. Vcc = 3.3 V, V_{BAT2} = –24 V, V_{BAT1} = –60 V for Scan/OHT/Ground Start/Disconnect states, –75 V/–85 V/ –100 V/–145 V for Ringing state of Le9500A/B/C/D.

Table 1. Two-Wire Port

Parameter	Min	Typ	Max	Unit
Tip or Ring Drive Current = DC + Longitudinal + Signal Currents[1]	105	—	—	mApk
Tip or Ring Drive Current = Ringing + Longitudinal[1]	65	—	—	
Signal Current[1]	10	—	—	mArms
Longitudinal Current Capability per Wire (Longitudinal current is independent of DC loop current.)[1]	8.5	15	—	
Ringing Current (R_{LOAD} = 1386 Ω + 40 μF)[1]	29	—	—	
DC Loop Current Limit – I_{LIM} (V_{BAT2} applied, R_{LOOP} = 100 Ω):				mA
V_{PROG} = AGND	—	25	—	
V_{PROG} = Open	—	40	—	
DC Current Limit Variation	—	—	±8	%
DC Feed Resistance (does not include protection resistors)	—	40	—	Ω
Open Loop Voltages:				V
Scan state:				
$\|V_{BAT1}\|$ > 51 V $\|V_{TIP}\| – \|V_{RING}\|$	44	51	—	
$\|V_{TIP}\|$, $\|V_{RING}\|$ to Battery Ground	—	—	56.5	
OHT state:				
$\|V_{BAT1}\|$ > 51 V $\|V_{TIP}\| – \|V_{RING}\|$	41	49	—	
$\|V_{TIP}\|$, $\|V_{RING}\|$ to Battery Ground	—	—	56.5	
Active state:				
$\|V_{TIP} – V_{RING}\| – \|V_{BAT2}\|$	5.75	7.2	8.5	
Ring state:				
$\|V_{TIP} – V_{RING}\| – \|V_{BAT1}\|$	—	4	—	
Loop Closure Threshold:				mA
Scan/Active/On-hook Transmission states, On– to Off–hook	9.4	11.0	12.6	
Loop Closure Threshold Hysteresis:				mA
Scan/Active/On-hook Transmission states	—	3.0	—	
Longitudinal to Metallic Balance at PT/PR[2]:				dB
Test Method: Q552 (11/96) Section 2.1.2 and *IEEE*® 455:				
300 Hz to 600 Hz	52	—	—	
600 Hz to 3.4 kHz	52	—	—	
Metallic to Longitudinal (HARM) Balance[3]:				dB
200 Hz to 1000 Hz	40	—	—	
100 Hz to 4000 Hz	40	—	—	
PSRR 500 Hz – 3000 Hz[1]:				dB
V_{BAT1}, V_{BAT2}	45	—	—	
V_{CC}	25	30	—	

1. *This parameter is not tested in production. It is guaranteed by design and device characterization.*
2. *Tested at 1KHz in production.*
3. *DC test only.*

Table 2. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
TXI (input impedance)	—	100	—	kΩ
Output Offset (VTX)	—	—	±10	mV
Output Offset (VITR)	—	—	100	mV
Output Drive Current (VTX)	±300	—	—	µA
Output Drive Current (VITR)	±10	—	—	µA
Output Voltage Swing:				
Maximum (VTX, VITR)	AGND	—	V_{CC}	V
Minimum (VTX)	AGND + 0.25	—	V_{CC} – 0.5	V
Minimum (VITR)	AGND + 0.35	—	V_{CC} – 0.4	V
Output Short-circuit Current	—	—	±50	mA
Output Load Resistance[1]	10	—	—	kΩ
Output Load Capacitance[1]	—	20	—	pF
RCVN and RCVP:				
Input Voltage Range	0	—	V_{CC} – 0.3	V
Input Bias Current	—	0.12	—	µA
Differential PT/PR Current Sense (DCOUT):				
Gain (PT/PR to DCOUT)	—	15	—	V/A
Offset Voltage at I_{LOOP} = 0	–15	—	15	mV
AC Termination Impedance[2]	150	600	1400	Ω
Total Harmonic Distortion (200 Hz – 4 kHz)[1]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain (f = 1004 Hz, 1020 Hz)[3]:				
PT/PR Current to VITR	291	300	309	V/A
Receive Gain, f = 1004 Hz, 1020 Hz Open Loop				
RCVP or RCVN to PT – PR	7.76	8	8.24	—
Gain vs. Frequency (transmit and receive)[1],				
600 Ω Termination, 1004 Hz, 1020 Hz Reference:				
200 Hz to 300 Hz	–0.3	0	0.05	dB
300 Hz to 3.4 kHz	–0.05	0	0.05	
3.4 kHz to 20 kHz	–3.0	0	0.05	
20 kHz to 266 kHz	—	—	2.0	
Gain vs. Level (transmit and receive)[1], 0 dBV Reference:				
–55 dB to +3.0 dB	–0.05	0	0.05	dB
Idle-channel Noise (tip/ring), 600 Ω Termination:				
C-Message	—	8	13	dBmC
Psophometric[1]	—	–82	–77	dBrnp
3 kHz Flat[1]	—	—	20	dBrn
Idle-channel Noise (VTX), 600 Ω Termination:				
C-Message	—	8	13	dBmC
Psophometric[1]	—	–82	–77	dBrnp
3 kHz Flat[1]	—	—	20	dBrn

1. *This parameter is not tested in production. It is guaranteed by design and device characterization.*
2. *Set externally either by discrete external components or a third- or fourth-generation codec. Any complex impedance R1 + R2 || C between 150 Ω and 1400 Ω can be synthesized.*
3. *VITR transconductance depends on the resistor from ITR to VITR. This gain assumes an ideal 4.75 kΩ, (the recommended value). Positive current is defined as the differential current flowing from PT to PR.*

Table 3. Logic Inputs and Outputs

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages: Low Level High Level	 V_{IL} V_{IH}	 –0.5 2.0	 0.2 2.5	 0.5 V_{CC}	V
Input Current: Low Level (V_{CC} = 3.46 V, V_I = 0.4 V) High Level (V_{CC} = 3.46 V, V_I = 2.4 V)	 I_{IL} I_{IH}	 — —	 — —	 ±50 ±50	µA
Output Voltages (open collector with internal 60 kΩ pull-up resistor): Low Level (V_{CC} = 3.13 V, I_{OL} = 360 µA) High Level (V_{CC} = 3.13 V, I_{OH} = –5 µA)	 V_{OL} V_{OH}	 0 2.2	 0.2 —	 0.5 V_{CC}	V

Table 4. Ground Start

Parameter	Min	Typ	Max	Unit
Tip Open state – Tip Input Impedance	150	—	—	kΩ
Threshold, On– to Off–hook	—	13	—	mA
Hysteresis	—	2	—	mA

Table 5. Ringing Specifications

Parameter	Min	Typ	Max	Unit
$RING_{INN/P}$: Input Voltage Swing	 0	 —	 V_{CC}	V
Ring Signal Isolation: PT/PR to VTX Ring state	 —	 60	 —	dB
Ring Signal Isolation: $RING_{IN}$ to PT/PR Non-ringing state	 —	 80	 —	dB
Ring Signal Distortion[1]: Open or 5 REN Load, 100 Ω Loop 5 REN (Ringing Equivalency Number) is equivalent of 1380 Ω in series with 40 µF	 —	 3	 —	%
Differential Gain $RING_{INP/N}$ to PT/PR R_{LOAD} = Open, V_{BAT1} = –75 V (Le9500A), $V_{RINGINP/N}$ = 0.51 V_{PP}; V_{BAT1} = –85 V (Le9500B), $V_{RINGINP/N}$ = 0.59 V_{PP}; V_{BAT1} = –100 V (Le9500C), $V_{RINGINP/N}$ = 0.70 V_{PP}; V_{BAT1} = –145 V (Le9500D), $V_{RINGINP/N}$ = 1.04 V_{PP}.	 124	 130	 136	 V/V

1. This parameter is not tested in production. It is guaranteed by design and device characterization.

Table 6. Ring Trip

Parameter	Min	Typ	Max	Unit
Ring Trip (NSTAT = 0): Loop Resistance (total) V_{BAT1} Applied	 100	 —	 600	Ω
Ring Trip (NSTAT = 1): Loop Resistance (total) V_{BAT1} Applied	 —	 —	 10	kΩ
Trip Time (f = 20 Hz)[1]	—	—	100	ms
Hysteresis[1]	—	10	—	mA

1. This parameter is not tested in production. It is guaranteed by design and device characterization.

Pre-trip immunity

Ringing will not be tripped by the following loads across Tip and Ring as shown in the reference schematic in the this document. Ringing frequency = 17 Hz to 23 Hz otherwise specified.

- 10-kΩ resistor in parallel with 5 Ringer Equivalency Number (REN) (equivalent of 1386-Ω + 40-µF) per GR-909 Issue 2, December 2004
- 10-kΩ resistor in parallel with a 2-µF capacitor in parallel with 5 Ringer Equivalency Number (REN) (equivalent of 1386-Ω + 40-µF) per GR 57 Issue 1 October 2001.

OPERATING STATES

Table 7. Control States

B0	B1	B2	Operating State
0	0	1	Forward active
0	1	1	Reverse active
0	0	0	On-hook transmission forward battery
0	1	0	On-hook transmission reverse battery
1	1	0	Ground start
1	0	0	Scan
1	1	1	Disconnect (*default device power up state)*
1	0	1	Ring

Table 8. Supervision Coding

NSTAT
0 = off-hook or ring trip or thermal shutdown or ring ground.
1 = on-hook and no ring trip and no thermal shutdown and no ring ground.

Operating State Definitions

Forward Active

- Pin PT is positive with respect to PR.
- V_{BAT2} is applied to tip/ring drive amplifiers.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- Overhead is set to nominal 7.2 V for undistorted transmission of 3.14 dBm into 900 Ω with 500 mVrms of PPM.

Reverse Active

- Pin PR is positive with respect to PT.
- V_{BAT2} is applied to tip/ring drive amplifiers.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- Overhead is set to nominal 7.2 V for undistorted transmission of 3.14 dBm into 900 Ω with 500 mVrms of PPM.

Scan

- Except for loop closure, all circuits (including ring trip and common-mode detector) are powered down.
- On-hook transmission is disabled.
- Pin PT is positive with respect to PR and V_{BAT1} is applied to tip/ring.
- The tip to ring on-hook differential voltage will be typically between –44 V and –51 V with a –51 V to –100 V primary battery.

On-Hook Transmission—Forward Battery

- Pin PT is positive with respect to PR.
- V_{BAT1} is applied to tip/ring drive amplifiers.
- Supervision circuits, loop closure, and common-mode detect are active.
- Ring trip detector is turned off to conserve power.

- On-hook transmission is allowed.
- The tip to ring on-hook differential voltage will be typically between –41 V and –49 V with a –51 V to –100 V primary battery.

On-Hook Transmission—Reverse Battery

- Pin PR is positive with respect to PT.
- V_{BAT1} is applied to tip/ring drive amplifiers.
- Supervision circuits, loop closure, and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- On-hook transmission is allowed.
- The tip to ring on-hook differential voltage will be typically between –41 V and –49 V with a –51 V to –100 V primary battery.

Disconnect

- The tip/ring amplifiers and all supervision are turned off.
- The SLIC device goes into a high-impedance state.
- NSTAT is forced high (on-hook).
- Due to internal pull-ups, device will power up in this state.

Ring

- Power ring signal is applied to tip and ring.
- Input wave form at $RING_{INN/P}$ is amplified.
- Ring trip supervision and common-mode current supervision are active; loop closure is inactive.
- Overhead voltage is reduced to typically 4 V.

Ground Start

- Tip drive amplifier is turned off.
- Device presents a high impedance (>100 kΩ) to pin PT.
- Device presents a clamped (amplitude <56.5 V) current-limited battery (V_{BAT1}) to PR.

Thermal Shutdown

- Not controlled via truth table inputs.
- This mode is caused by excessive heating of the device, such as may be encountered in an extended power cross situation. NSTAT output is forced low or off hook during a thermal shutdown event.

TEST CIRCUIT

Figure 2. Le9500 Device Basic Test Circuit

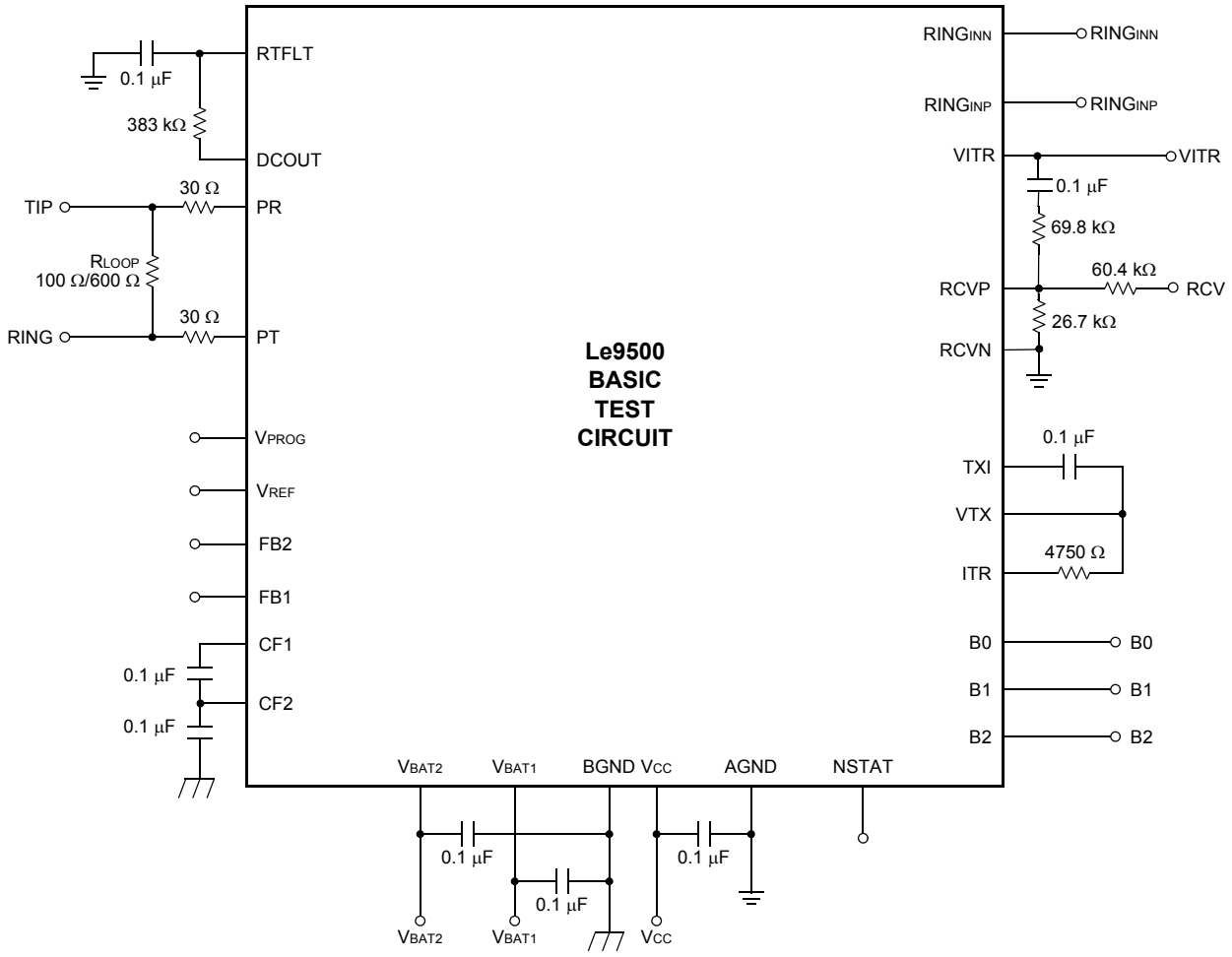


Figure 3. Metallic PSRR

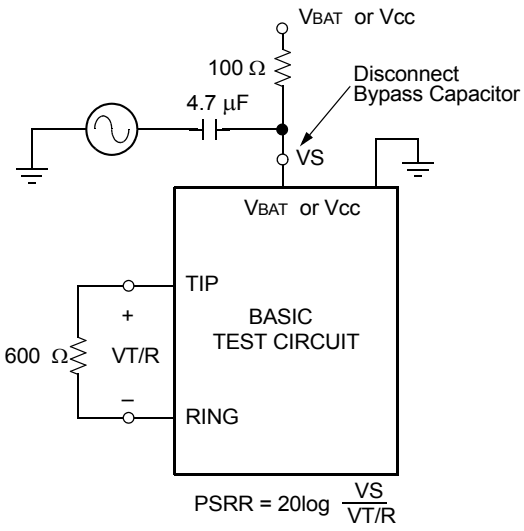


Figure 4. Longitudinal PSRR

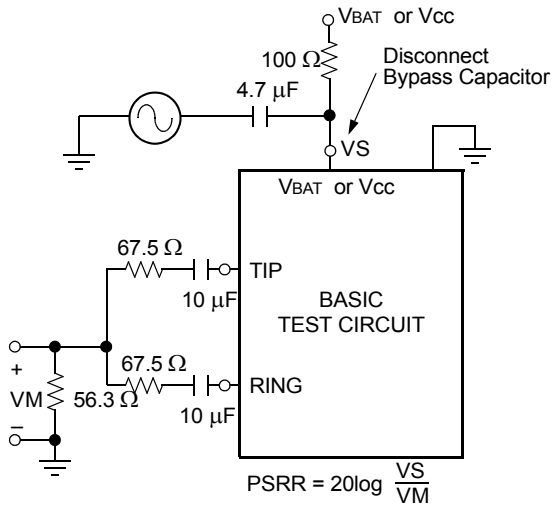


Figure 5. Longitudinal Balance

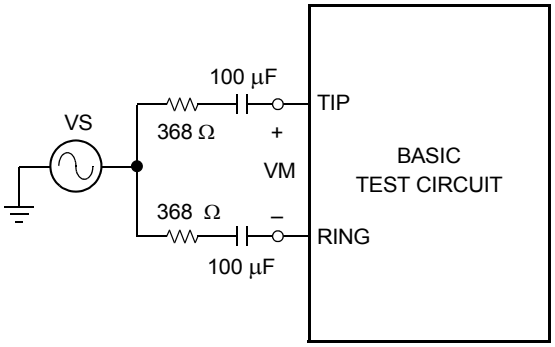
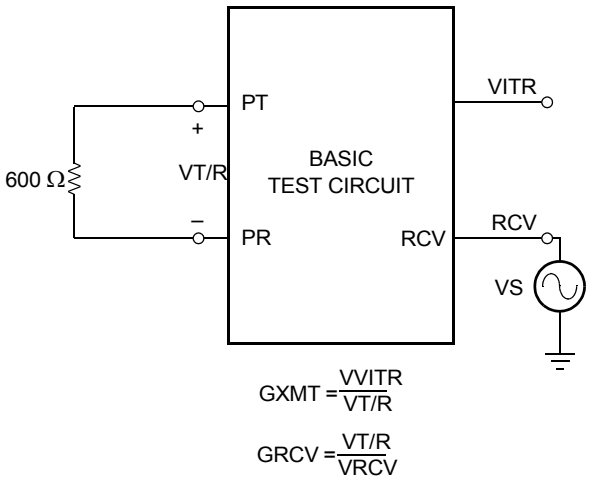


Figure 6. AC Gains



APPLICATIONS

DC Loop Current Limit

Current limit may be chosen from two discrete values, 25 mA or 40 mA, depending on if V_{PROG} is grounded (25 mA) or left floating (40 mA). Note that there is a 12.5 kΩ slope to the I/V characteristic in the current-limit region; thus, once in current limit, the actual loop current will increase slightly, as loop length decreases.

The above describes the active state steady-state current-limit response. There will be a transient response of the current-limit circuit upon an on- to off-hook transition. Typical active state transient current-limit response is given in Table 10.

Table 9. Typical Active state On-Hook to Off-Hook Tip/Ring Current-Limit Transient Response

Parameter	Value	Unit
DC Loop Current: Active state R_{LOOP} = 100 Ω On- to Off-hook Transition t < 5 ms	I_{LIM} + 60	mA
DC Loop Current: Active state R_{LOOP} = 100 Ω On- to Off-hook Transition t < 50 ms	I_{LIM} + 20	mA
DC Loop Current: Active state R_{LOOP} = 100 Ω On- to Off-hook Transition t < 300 ms	I_{LIM}	mA

Overhead Voltage

Active state

Overhead is fixed to a nominal 7.2 V, which is adequate for an on-hook transmission of 3.14 dBm into 900 Ω with additional head room for a 500-mV PPM signal.

Scan state

If the magnitude of the primary battery is greater than 51 V (but no more than 100 V), the magnitude of the open loop tip-to-ring open loop voltage is clamped typically between 44 V and 51 V. If the magnitude of the primary battery is less than a nominal 51 V, the overhead voltage will track the magnitude of the battery voltage, i.e., the magnitude of the open circuit tip-to-ring voltage will be about 4V less than battery.

On-Hook Transmission state

If the magnitude of the primary battery is greater than 51 V (but no more than 100 V), the magnitude of the open loop tip-to-ring open loop voltage is clamped typically between 41 and 49 V. If the magnitude of the primary battery is less than a nominal 51 V, the overhead voltage will track the magnitude of the battery voltage, i.e., the magnitude of the open circuit tip-to-ring voltage will be 6 to 8 V less than battery.

Ring state

In the ring state, to maximize ringing loop length, the overhead is decreased to the saturation of the tip ring drive amplifiers, a nominal 4 V.

During the ring state, to conserve power, the receive input at RCVN/RCVP is deactivated. During the ring state, to conserve power, the AAC amplifier in the transmit direction at VITR is deactivated. However, the AX amplifier at VTX is active during the ring state; differential ring current may be sensed at VTX during the ring state.

DC Loop Range

The DC loop range can be calculated by using the following equation:

$$R_{LOOP} = \frac{|V_{BAT2}| - V_{OH}}{I_{LOOP}} - 2R_P - R_{DC}$$

where:

V_{BAT2} is applied under off-hook conditions for power conservation and SLIC device thermal considerations.

V_{OH} is overhead voltage, typically 7.2V.

R_{DC} is DC feed impedance, typically 40 Ω.

R_P is protection resistor, typically 50 Ω.

I_{LOOP} is the loop DC current, no more than DC current limit.

If the minimum loop current allowed is 22 mA and V_{BAT2} is –21V then the maximum loop resistance by the equation is 487 Ω. This includes telephone set at the end of the loop.

The Le9500 device is intended for short-loop applications and, therefore, could always be in current limit during off-hook conditions. The above equation does not apply when the DC current is in the current limit region.

The actual maximum loop length the device can support, however, is often limited by the ringing loop length rather than the DC loop length (with adequate amplitude of V_{BAT2}).

Battery Reversal Rate

The rate of battery reverse is controlled or ramped by capacitors C_{FB1} and C_{FB2}. A chart showing C_{FB1} and C_{FB2} values versus typical ramp time is given below. Leave FB1 and FB2 open if it is not desired to ramp the rate of battery reversal. Use with 0.47 µF for CTX.

The voltage seen on FB1 and FB2 pins on the SLIC can be close to VBAT1. The value of C_{FB1} and C_{FB2} being greater than 0.22 µF is not recommended.

Table 10. C_{FB1} and C_{FB2} Values versus Typical Ramp Time

C_{FB1} and C_{FB2}	Transition Time
0.001 µF	2 ms
0.01 µF	20 ms
0.022 µF	50 ms
0.047 µF	100 ms
0.1 µF	220 ms
0.15 µF	320 ms

Supervision

The Le9500 device offers the loop closure and ring trip supervision functions. Internal to the device, the outputs of these detectors are multiplexed into a single package output, NSTAT. The ring trip detector is valid on NSTAT during the ring state, and loop closure detector is valid on NSTAT during active and on-hook transmission states. Additionally, common-mode current is detected for ground start applications. This status is output onto NSTAT and is valid during ground start mode.

Loop Closure

The loop closure has a fixed on-hook to off-hook threshold in Scan/Active/OHT states with hysteresis.

Ring Trip

The ring trip detector requires only a single-pole filter at the input, minimizing external components. An R/C combination of 383 kΩ and 0.1 µF, for a filter pole at 5.15 Hz, is recommended.

The ring trip threshold is internally fixed as a function of battery voltage and is given by the following:

$$R_T\ (mA) = 67 * \{(0.0045 * V_{BAT1}) + 0.317\}$$

where:

R_T is ring trip current in mA.

V_{BAT1} is the magnitude of the ring battery in V.

There is a typical 10 mA hysteresis.

Ground Start

In the ground start applications, the loop closure detector is also used to indicate ring-ground has occurred. During ground start mode, loop current will be common mode, rather than differential as in loop start mode. Thus, in ground start the threshold of the loop closure detector is reduced by one half the threshold seen in the loop start mode. This output is seen at the NSTAT output pin.

Power Ring

The device offers a ring state, in which a balanced power ring signal is provided to the tip/ring pair. During the ring state, a user-supplied low-voltage ring signals are input to the device's $RING_{INP/N}$ inputs. These signals are amplified to produce the balanced power ring signals. The user may supply a sine wave input, PWM input, or a square wave to produce sinusoidal or trapezoidal ringing at tip and ring.

Sine Wave Input Signal and Sine Wave Power Ring Signal Output

The low-voltage sine wave input is applied differentially or single ended to the Le9500 device at pins RINGINP and RINGINN. During the ring state, the signals at pins RINGINP and RINGINN are amplified and presented to the subscriber loop. The differential gain from RINGINP/N to tip and ring is specified in the device specifications.

When the device enters the Ring state, the clamp circuit is disabled, allowing the voltage magnitude of the power ring signal to be maximized. Additionally, in the Ring state, the loop current limit is increased and is not limited by DC loop current limit.

The magnitude of the power ring voltage will be a function of the gain of the ring amplifier, the high-voltage battery, and the input signal level at RINGINP/N. The input range of the signal at RINGINP/N is 0 V to Vcc. As the input voltage at RINGINP/N is increased, the magnitude of the power ring voltage at tip and ring will increase linearly, until the tip and ring drive amplifiers begin to saturate. Once the tip and ring amplifiers reach saturation, further increases of the input signal will cause clipping distortion of the power ring signal at tip and ring. The ring signal will appear balanced on tip and ring. That is, the power ring signal is applied to both tip and ring, with the signal on tip 180-degree out of phase from the signal on ring.

The point at which clipping of the power ring signal begins at tip and ring is a function of the battery voltage, the input capacitor at RINGINP/N, and the input signal at RINGINP/N and VCC. During non-ringing states, the sinusoidal ringing waveform may be left on at RINGINP/N. Via the state table, the ring signal will be removed from tip and ring, even if the low voltage input is still present at RINGINP/N.

Power Ringing with Le9500D

For operation of the Le9500D device with a high magnitude on VBAT1 greater than -100 V, special attention must be given to the following areas at system level.

Ringing Cadence

Scan or On Hook transmission state must be used during the silent period of ringing. Do not use Active state.

VBAT1 supply

VBAT1 may be more negative than -100 V only during the actual power ringing. The amplitude of VBAT1 should not exceed 100 V when the SLIC device is not in the Ringing mode. The amplitude of VBAT1 may not exceed 100 V during the silent period of ringing or any other non-ringing mode of operation.

Pre-Trip Immunity

The Le9500D device pre-trip immunity is specified as 2 µF. With battery voltages more negative than -100 V, ringing into a heavy pre trip load will generate excessive power. Depending on system and ambient conditions, ringing into a load heavier than 2 µF could force the device into thermal shutdown. Under these conditions, as the device goes into and out of thermal shutdown a glitch will appear on NSTAT. Proper operation may require the system to filter out these glitches.

Robust Ring Trip Indication

Upon ring trip, there will be large current going through the SLIC device which may cause the SLIC to go into thermal shutdown. Upon thermal shutdown, NSTAT remains Low, which is still consistent with the Ring Trip state. During thermal shutdown, the net voltage on RTFLT will go up because the Tip Ring amplifiers are off. When the voltage on RTFLT passes a certain limit (ring trip threshold), until a SLIC state change, NSTAT will toggle between the thermal shutdown inducted low indication and the RTFLT voltage high indication.

There are several ways to help remedy this situation. Limit the current on VBAT1 supply such that VBAT1 will move up towards ground upon off hook, add a 100-Ω power resistor in the VBAT1, or add a 2-MΩ resistor from RTFLT to ground to lower ring trip threshold.

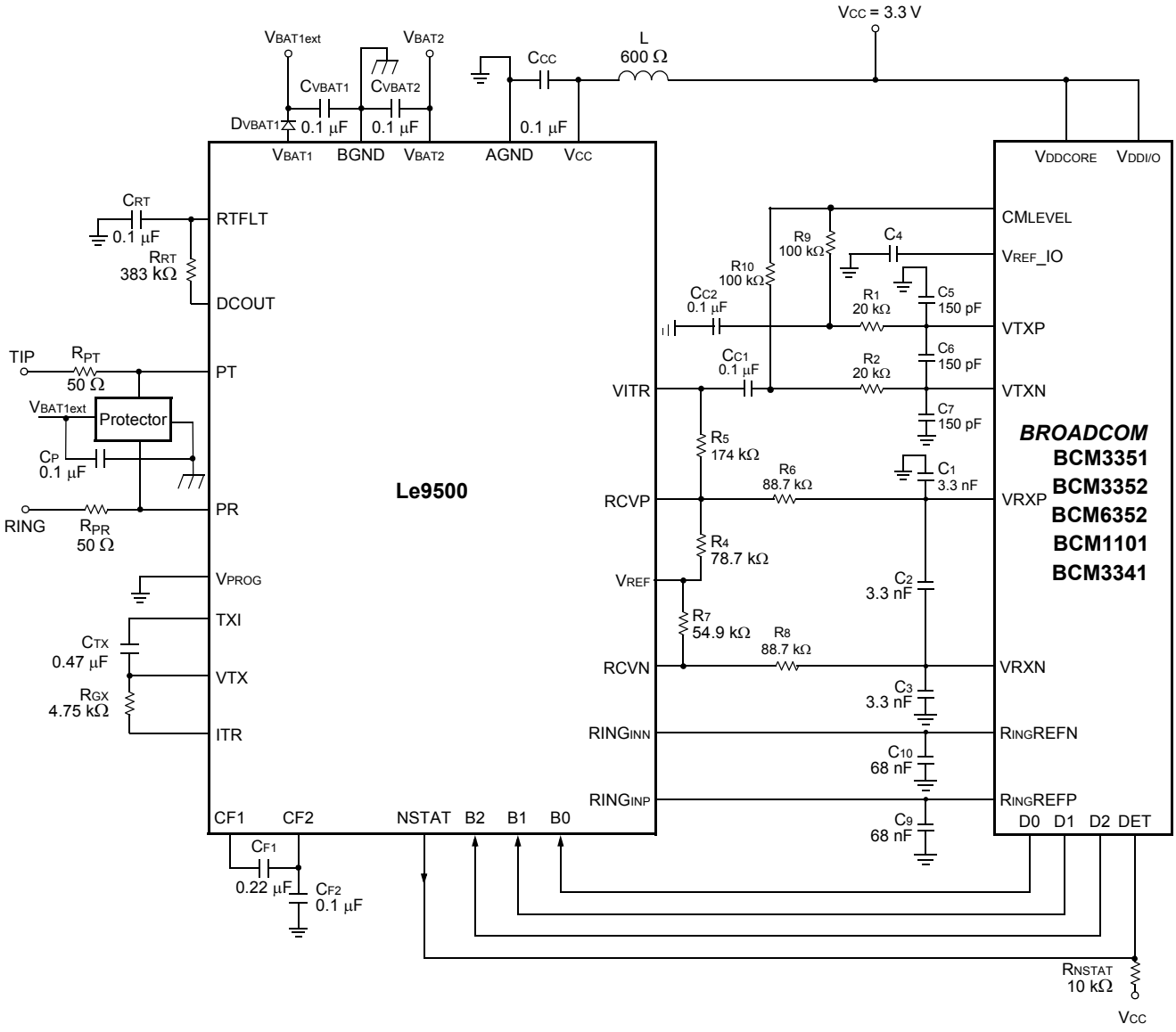
For more details, please contact Zarlink field/customer applications.

Design Examples

The following reference schematics show the complete Le9500 SLIC schematic for interfaces to Broadcom codecs.

Le9500/Broadcom® Reference Schematic A

The following reference circuit shows the complete Le9500 SLIC device schematic for interface to the *Broadcom* BCM3352 as designed on the *Broadcom* BCM93352SV application reference design and board. This circuit has a 600-Ω AC termination. The BCM3351, BCM3352, and BCM6352 have programmable registers to modify the external 600-Ω termination to achieve worldwide real or complex terminations. For complex terminations with BCM1101, the external circuit must be changed to set the complex termination. Other resistive terminations require a change to this circuit. Contact your Zarlink account representative for assistance with modifications to this circuit.



Application Circuit Parts List A

The following parts list is for the Zarlink Le9500 SLIC device and Broadcom BCM3352 codec (per Broadcom BCM93552SV application board daughter board components), fully programmable.

Item	Type	Value	Tolerance	Rating	Comments
Fault Protection					
R_{PT}	Resistor	50 Ω	1%	Fusible or PTC	Protection resistor.
R_{PR}	Resistor	50 Ω	1%	Fusible or PTC	Protection resistor.
Protector	Battery referenced thyristor		—	—	Secondary protection. Reference to most negative power supply ($V_{BAT1ext}$).
C_P	Capacitor	0.1 µF	20%	100 V[1]	Consult protector vendor for recommended value.
Power Supply					
C_{VBAT1}	Capacitor	0.1 µF	20%	100 V[1]	V_{BAT1} filter capacitor.
C_{VBAT2}	Capacitor	0.1 µF	20%	50 V[2]	V_{BAT2} filter capacitor. $\|V_{BAT2}\| < \|V_{BAT1}\|$.
D_{VBAT1}	Diode	1N4004	—	—	Reverse current.
C_{CC}	Capacitor	0.47 µF	20%	10 V	Ceramic bypass capacitor.
L	Ferrite Bead	600 Ω, *Murata*® BLM11A601SPB	—	—	Filtering.
C_{F1}	Capacitor	0.22 µF	20%	100 V	Filter capacitor.
C_{F2}	Capacitor	0.1 µF	20%	100 V	Filter capacitor.
Ring Trip					
C_{RT}	Capacitor	0.1 µF	20%	10 V	Ring trip filter capacitor.
R_{RT}	Resistor	383 kΩ	1%	1/16 W	Ring trip filter resistor.
AC Interface					
R_{GX}	Resistor	4.75 kΩ	1%	1/16 W	Sets T/R to VITR transimpedance.
C_{TX}	Capacitor	0.47 µF	20%	10 V	AC/DC separation.
C_{C1}	Capacitor	0.1 µF	20%	10 V	DC blocking capacitor
R_4	Resistor	78.7 kΩ	1%	1/16 W	AC interface.
R_5	Resistor	174 kΩ	1%	1/16 W	AC interface.
R_6	Resistor	88.7 kΩ	1%	1/16 W	AC interface.
R_7	Resistor	54.9 kΩ	1%	1/16 W	AC interface.
R_8	Resistor	88.7 kΩ	1%	1/16 W	AC interface.
R_{NSTAT}	Resistor	10 kΩ	1%	1/16 W	Control.
Le9500	SLIC device	—	—	—	

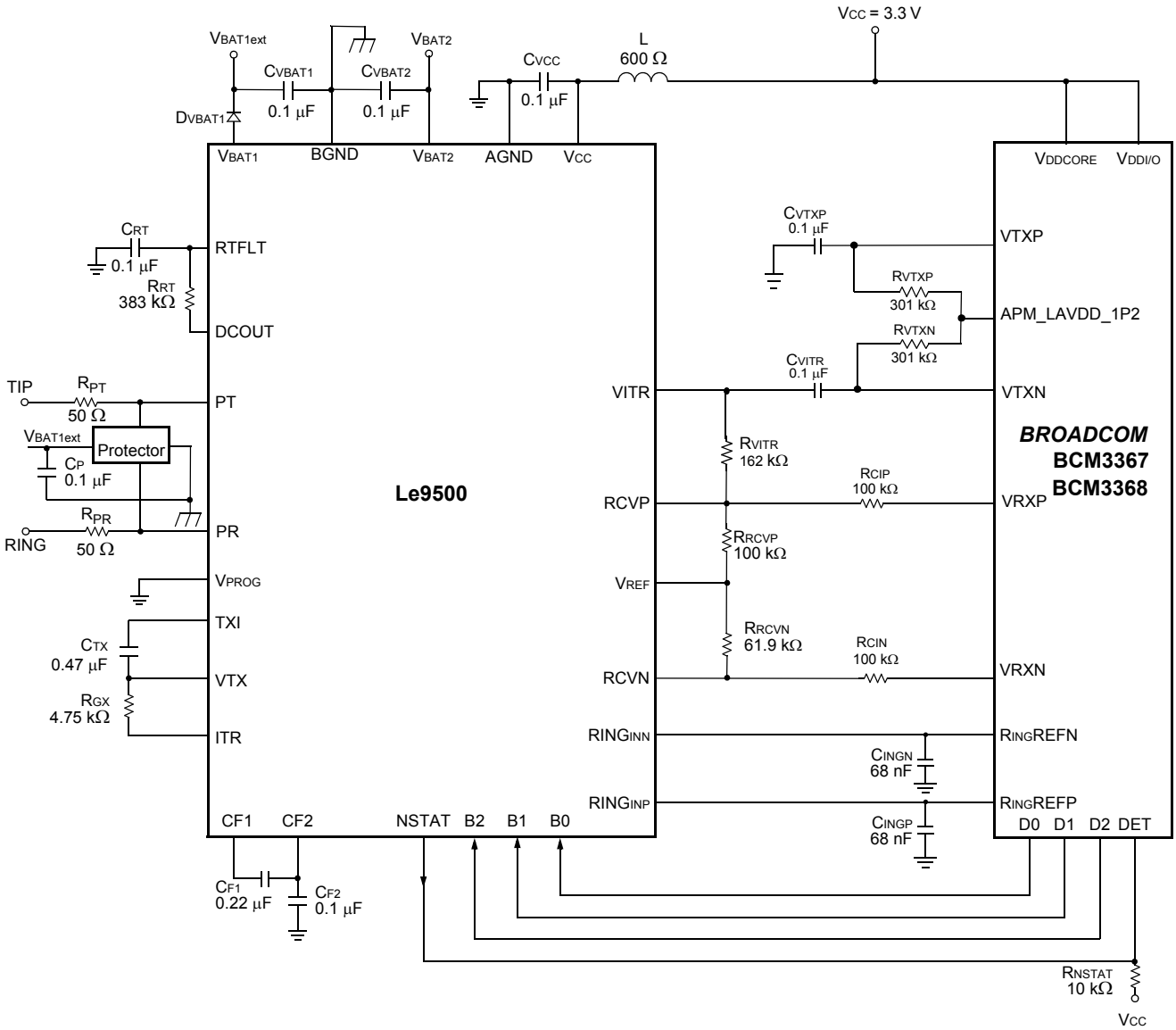
Note:

1. *Increase to 200 V for Le9500C and Le9500D.*
2. *Assume $\|V_{BAT2}\|$<50V.*

Le9500/Broadcom® Reference Schematic B

The following reference schematic shows the complete Le9500 SLIC device schematic for interface to the *Broadcom* BCM3367/3368. This circuit has a natural 700-Ω AC termination impedance. The BCM3367 or MCB3368 has programmable registers to modify the external 700-Ω termination to achieve worldwide real or complex terminations, as well as to set transmit and receive gains, and other AC parameters. The BCM3367/3368 codec also drives ringing inputs, sets SLIC operation state, and monitors NSTAT. The voltage of the battery supply to V_{BAT1} is expected to be properly set and may vary depending upon SLIC operational states.

Contact your Zarlink account representative for assistance with other applications.



Application Circuit Parts List B

The following parts list is for the Zarlink Le9500 SLIC device and Broadcom BCM3367/3368 codec.

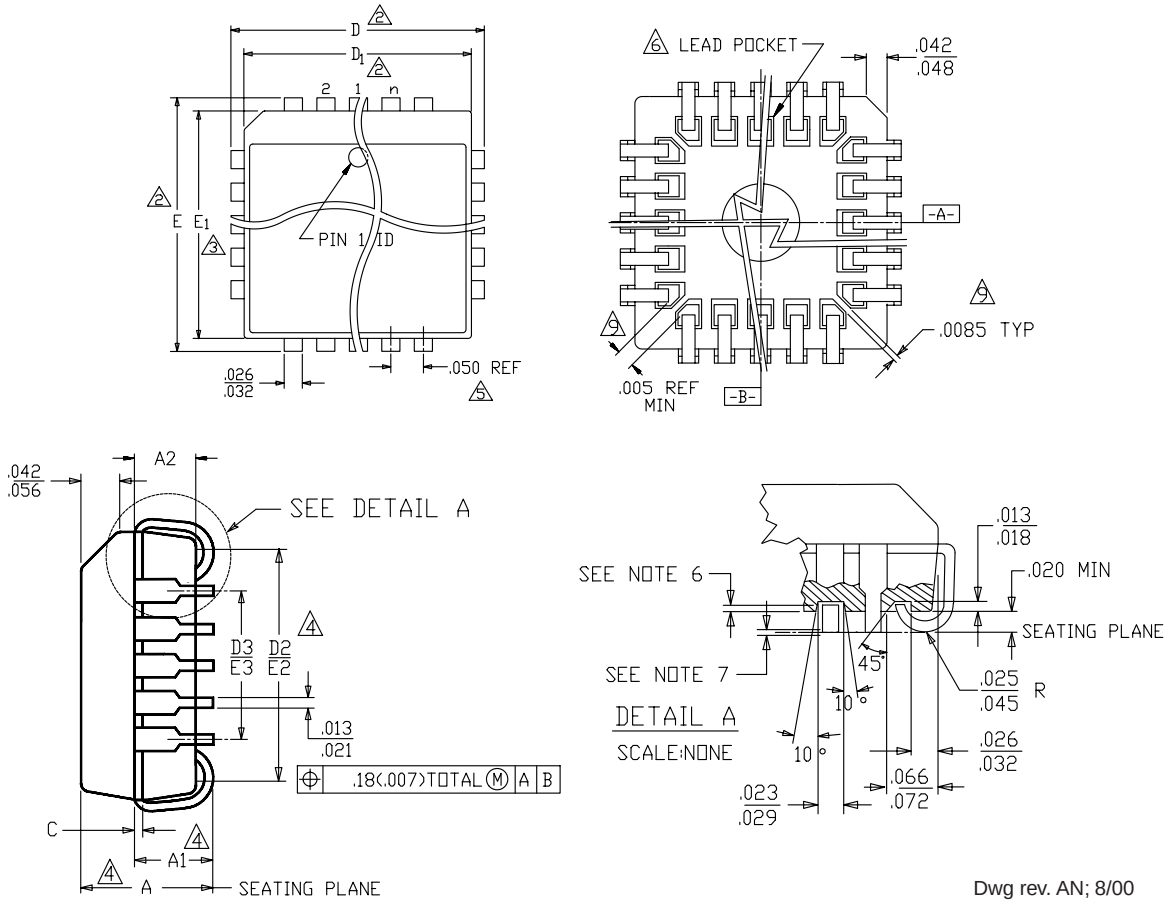
Item	Type	Value	Tolerance	Rating	Comments
Fault Protection					
R_{PT}	Resistor	50 Ω	1%	Fusible or PTC	Protection resistor.
R_{PR}	Resistor	50 Ω	1%	Fusible or PTC	Protection resistor.
Protector	Battery referenced thyristor		—	—	Secondary protection. Reference to most negative power supply ($V_{BAT1ext}$).
C_P	Capacitor	0.1 µF	20%	100 V[1]	Consult protector vendor for recommended value.
Power Supply					
C_{VBAT1}	Capacitor	0.1 µF	20%	100 V[1]	V_{BAT1} filter capacitor.
C_{VBAT2}	Capacitor	0.1 µF	20%	50 V[2]	V_{BAT2} filter capacitor. $\|V_{BAT2}\| < \|V_{BAT1}\|$.
D_{VBAT1}	Diode	1N4004	—	—	Reverse current.
C_{VCC}	Capacitor	0.47 µF	20%	10 V	Ceramic bypass capacitor.
L	Ferrite Bead	600 Ω, *Murata*® BLM11A601SPB	—	—	Filtering.
C_{F1}	Capacitor	0.22 µF	20%	100 V	Filter capacitor.
C_{F2}	Capacitor	0.1 µF	20%	100 V	Filter capacitor.
Ring Trip					
C_{RT}	Capacitor	0.1 µF	20%	10 V	Ring trip filter capacitor.
R_{RT}	Resistor	383 kΩ	1%	1/16 W	Ring trip filter resistor.
AC Interface					
R_{GX}	Resistor	4.75 kΩ	1%	1/16 W	Sets T/R to VITR transimpedance.
C_{TX}	Capacitor	0.47 µF	20%	10 V	AC/DC separation.
C_{VITR}	Capacitor	0.1 µF	20%	10 V	DC blocking capacitor.
C_{VTXP}	Capacitor	0.1 µF	20%	10 V	DC blocking capacitor.
R_{VITR}	Resistor	162 kΩ	1%	1/16 W	AC interface.
R_{VTXP}	Resistor	301 kΩ	1%	1/16 W	AC interface.
R_{VTXN}	Resistor	301 kΩ	1%	1/16 W	AC interface.
R_{CIP}	Resistor	100 kΩ	1%	1/16 W	AC interface.
R_{CIN}	Resistor	100 kΩ	1%	1/16 W	AC interface.
R_{RCVP}	Resistor	100 kΩ	1%	1/16 W	AC interface.
R_{RCVN}	Resistor	61.9 kΩ	1%	1/16 W	AC interface.
C_{INGP}	Capacitor	0.068 µF	20%	10 V	Ringing interface.
C_{INGN}	Capacitor	0.068 µF	20%	10 V	Ringing interface.
R_{NSTAT}	Resistor	10 kΩ	1%	1/16 W	Control.
Le9500	SLIC device	—	—	—	

Note:

1. *Increase to 200 V for Le9500C and Le9500D.*
2. *Assume $\|V_{BAT2}\|<50V$.*

PHYSICAL DIMENSIONS

28-Pin PLCC



Dwg rev. AN; 8/00

PACKAGE	28-Pin PLCC	
JEDEC	MS-018(A)AB	
SYMBOL	MIN	MAX
A	.165	.180
A1	.090	.120
A2	.062	.083
D	.485	.495
D1	.450	.456
D2	.390	.430
D3	.300	REF
E	.485	.495
E1	.450	.456
E2	.390	.430
E3	.300	REF
C	.009	.015

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010 INCH
4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE
5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005 INCH.
6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.
7. LEAD COPLANARITY SHALL BE WITHIN .004 INCH AS MEASURED FROM SEATING PLANE.
8. LEAD TWEEZE SHALL BE WITHIN .0045 INCH ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE.
9. LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

REVISION HISTORY

Revision A1 to B1

- Added Note 1 to 5V Supply Currents and Power Dissipation tables.
- Updated typical values for 3.3V and 5V Supply Currents and Power Dissipation tables.
- Added Le9500C section with "TBD" values.
- Removed "150V" from "150V HV7 Technology", page 1.
- Corrected Battery Supply and Office Battery Supply specifications for absolute and electrical ranges, page 6.
- Fixed "5-V" and "5 V" formatting on power dissipation tables, page10.
- Corrected typical values for Table 1, added "Note 2" to Longitudinal to Metallic Balance, and "Note 3" to metallic to Longitudinal Balance, page 11.
- Applied "Note 2" to Psophometric and 3-kHz Flat ICN, page 12.
- Combined Ground Start Hysteresis to one line, and added "Note 1" to Differential Gain on Table 6, page 13.
- Corrected wording "(-65V to 105V)" to be "(-65V to -100V)" under the power control section, page 18.

Revision B1 to C1

- Removed standard OPNs and added green package OPNs in *Ordering Information*, on page 1
- Added *Package Assembly*, on page 6

Revision C1 to D1

- Added Le9500D device information.

Revision D1 to E1

- In *Ordering Information*, on page 1, added column for packing; added Note 2 for instructions on tape/reel ordering.
- In *Electrical Characteristics*, on page 7,changed the Active State /PT-PR/-/Vbat2/ maximum from 7.75 V to 8.5 V.

Revision E1 to F1

- In *Absolute Maximum Ratings*, on page 6, separated ratings for VBAT1 in non-ringing and ringing states.
- In *Ring Trip*, on page 11, added pre-trip condition for the Le9500D device.
- Added *Power Ringing with Le9500D*, on page 18

Revision F1 to F2

- Added a note (the new note 1) under the Thermal Characteristics table on page 7 and removed the corresponding statement about TSD in the note under the ABSOLUTE MAXIMUM RATINGS table on page 6.

Revision F2 to G1

- Removed descriptions and specifications related to Vcc = 5 V.
- Added BCM3367/3368 to *Applications*, on page 1.
- Updated *Thermal Characteristics*, on page 7.
- Added test conditions to *Line Characteristics*, on page 9.
- Updated Loop Closure Thresholds and Hysteresis in Table 1, *Two-Wire Port*, on page 9.
- Updated PSRR for Vcc to reflect Vcc= 3.3 V in Table 1, *Two-Wire Port*, on page 9.
- Corrected the DCOUT gain in Table 2, *Analog Pin Characteristics*, on page 10
- Updated Ring Signal Distortion and Differential Gain RINGINP/N to PT/PR in Table 5, *Ringing Specifications*, on page 11
- Updated descriptions to *DC Loop Current Limit*, on page 16.
- Updated descriptions to *Battery Reversal Rate*, on page 17 and Table 10, *CFB1 and CFB2 Values versus Typical Ramp Time*, on page 17.
- Updated descriptions to *Power Ring*, on page 17.
- Added Reference Schematic B, on page 21.
- Added Parts List B, on page 22.

Revision G1 to G2

- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

For more information about all Zarlink products visit our Web Site at

www.zarlink.com