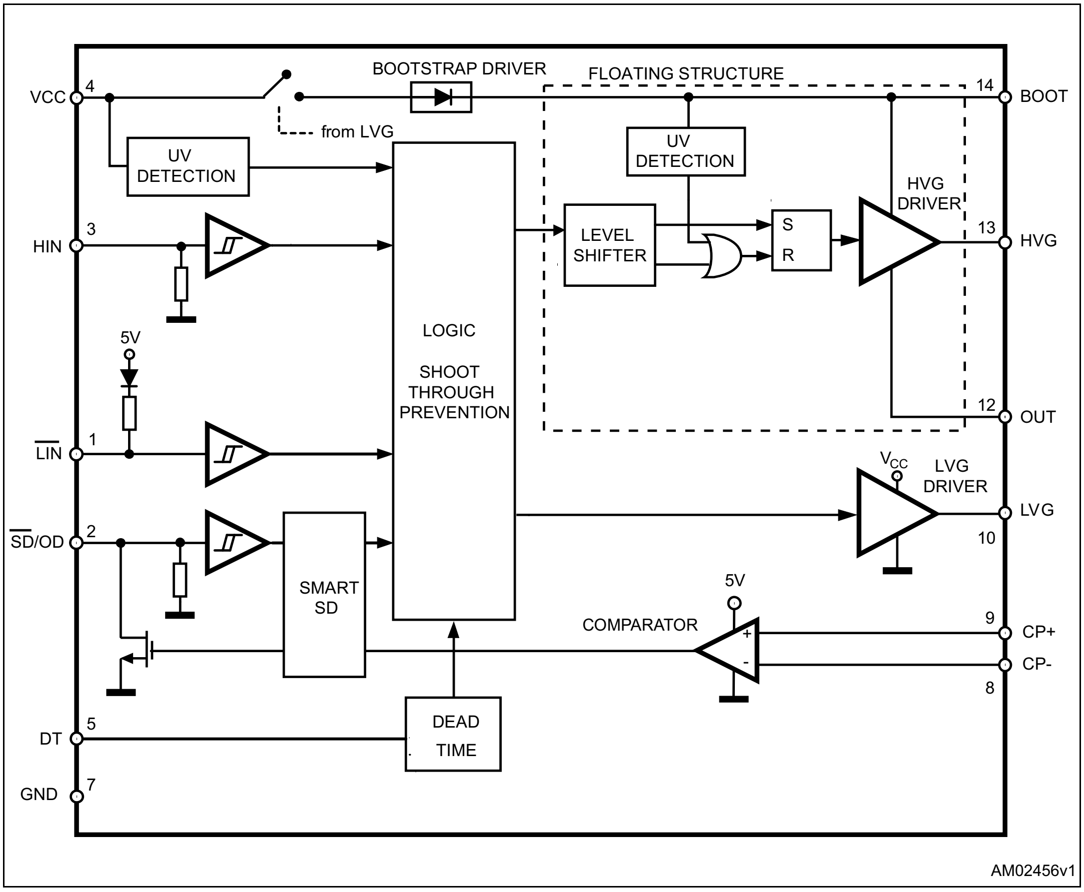
Contents

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

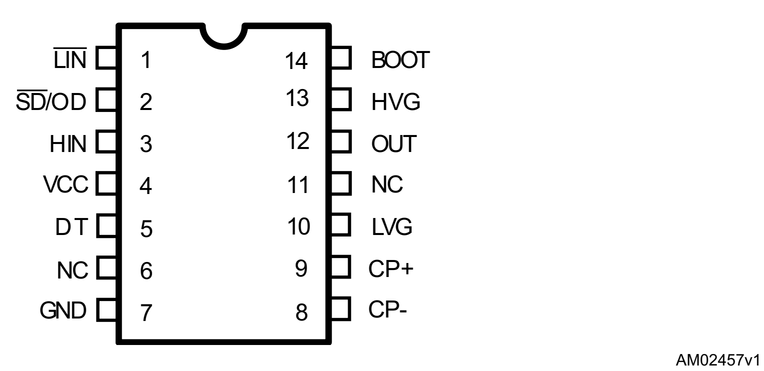


Table 1. Pin description

Pin number	Pin name	Type	Function
1	$\overline{LIN}$	I	Low-side driver logic input (active low)
2	$\overline{SD}$/OD [1]	I/O	Shutdown logic input (active low)/open-drain comparator output
3	HIN	I	High-side driver logic input (active high)
4	VCC	P	Lower section supply voltage
5	DT	I	Deadtime setting
6	NC		Not connected
7	GND	P	Ground
8	CP-	I	Comparator negative input
9	CP+	I	Comparator positive input
10	LVG[1]	O	Low-side driver output
11	NC		Not connected
12	OUT	P	High-side (floating) common voltage
13	HVG[1]	O	High-side driver output
14	BOOT	P	Bootstrapped supply voltage

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA), with V_{CC} > 3 V. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in $\overline{SD}$ condition.

3 Truth table

Table 2. Truth table

Input			Output	
$\overline{\text{SD}}$	$\overline{\text{LIN}}$	HIN	LVG	HVG
L	X(1)	X(1)	L	L
H	H	L	L	L
H	L	H	L	L
H	L	L	H	L
H	H	H	L	H

1. X: don't care.

4 Electrical data

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{cc}	Supply voltage	-0.3	21	V
V_{out}	Output voltage	V_{boot} - 21	V_{boot} + 0.3	V
V_{boot}	Bootstrap voltage	-0.3	620	V
V_{hvg}	High-side gate output voltage	V_{out} - 0.3	V_{boot} + 0.3	V
V_{lvg}	Low-side gate output voltage	-0.3	V_{cc} + 0.3	V
V_{cp-}	Comparator negative input voltage	-0.3	V_{cc} + 0.3	V
V_{cp+}	Comparator positive input voltage	-0.3	V_{cc} + 0.3	V
V_i	Logic input voltage	-0.3	15	V
V_{OD}	Open-drain voltage	-0.3	15	V
dv_{out} / dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation (T_A = 25 °C)		800	mW
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	SO-14	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	120	°C/W

4.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Pin	Parameter	Test conditions	Min.	Max.	Unit
V_{cc}	4	Supply voltage		12.5	20	V
V_{BO}(1)	14 - 12	Floating supply voltage		12.4	20	V
V_{out}	12	DC output voltage		- 9(2)	580	V
V_{CP-}	8	Comparator negative input voltage	V_{CP+} [2.5 V]		V_{CC}(3)	V
V_{CP+}	9	Comparator positive input voltage	V_{CP-} [2.5 V]		V_{CC}(3)	V
f_{sw}		Switching frequency	HVG, LVG load C_L = 1 nF		800	kHz
T_J		Junction temperature		-40	125	°C

1. $V_{BO} = V_{BOOT} - V_{OUT}$.
2. LVG off. V_{cc} = 12.5 V. Logic is operational if V_{BOOT} > 5 V.
3. At least one of the comparator's inputs must be lower than 2.5 V to guarantee proper operation.

5 Electrical characteristics

5.1 AC operation

Table 6. AC operation electrical characteristics (V_{CC} = 15 V; T_J = +25 °C)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}	1 vs. 10 3 vs. 13	High/low-side driver turn-on propagation delay	V_{out} = 0 V V_{boot} = Vcc C_L = 1 nF V_i = 0 to 3.3 V see *Figure 3*	50	125	200	ns
t_{off}		High/low-side driver turn-off propagation delay		50	125	200	ns
t_{sd}	2 vs. 10, 13	Shutdown to high/low-side driver propagation delay		50	125	200	ns
t_{isd}		Comparator triggering to high/low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CP+; CP- = 0.5 V		200	250	ns
MT		Delay matching, HS and LS turn-on/off				30	ns
DT	5	Deadtime setting range[1]	R_{DT} = 0 Ω, C_L = 1 nF	0.1	0.18	0.25	µs
			R_{DT} = 37 kΩ, C_L = 1 nF, C_{DT} = 100 nF	0.48	0.6	0.72	µs
			R_{DT} = 136 kΩ, C_L = 1 nF, C_{DT} = 100 nF	1.35	1.6	1.85	µs
			R_{DT} = 260 kΩ, C_L = 1 nF, C_{DT} = 100 nF	2.6	3.0	3.4	µs
MDT		Matching deadtime[2]	R_{DT} = 0 Ω, C_L = 1 nF			80	ns
			R_{DT} = 37 kΩ, C_L = 1 nF, C_{DT} = 100 nF			120	ns
			R_{DT} = 136 kΩ, C_L = 1 nF, C_{DT} = 100 nF			250	ns
			R_{DT} = 260 kΩ, C_L = 1 nF, C_{DT} = 100 nF			400	ns
t_r	10,13	Rise time	C_L = 1 nF		75	120	ns
t_f		Fall time	C_L = 1 nF		35	70	ns

1. See *Figure 4*.
2. MDT = | DT_{LH} - DT_{HL} | (see *Figure 5 on page 12*).

Figure 3. Timing

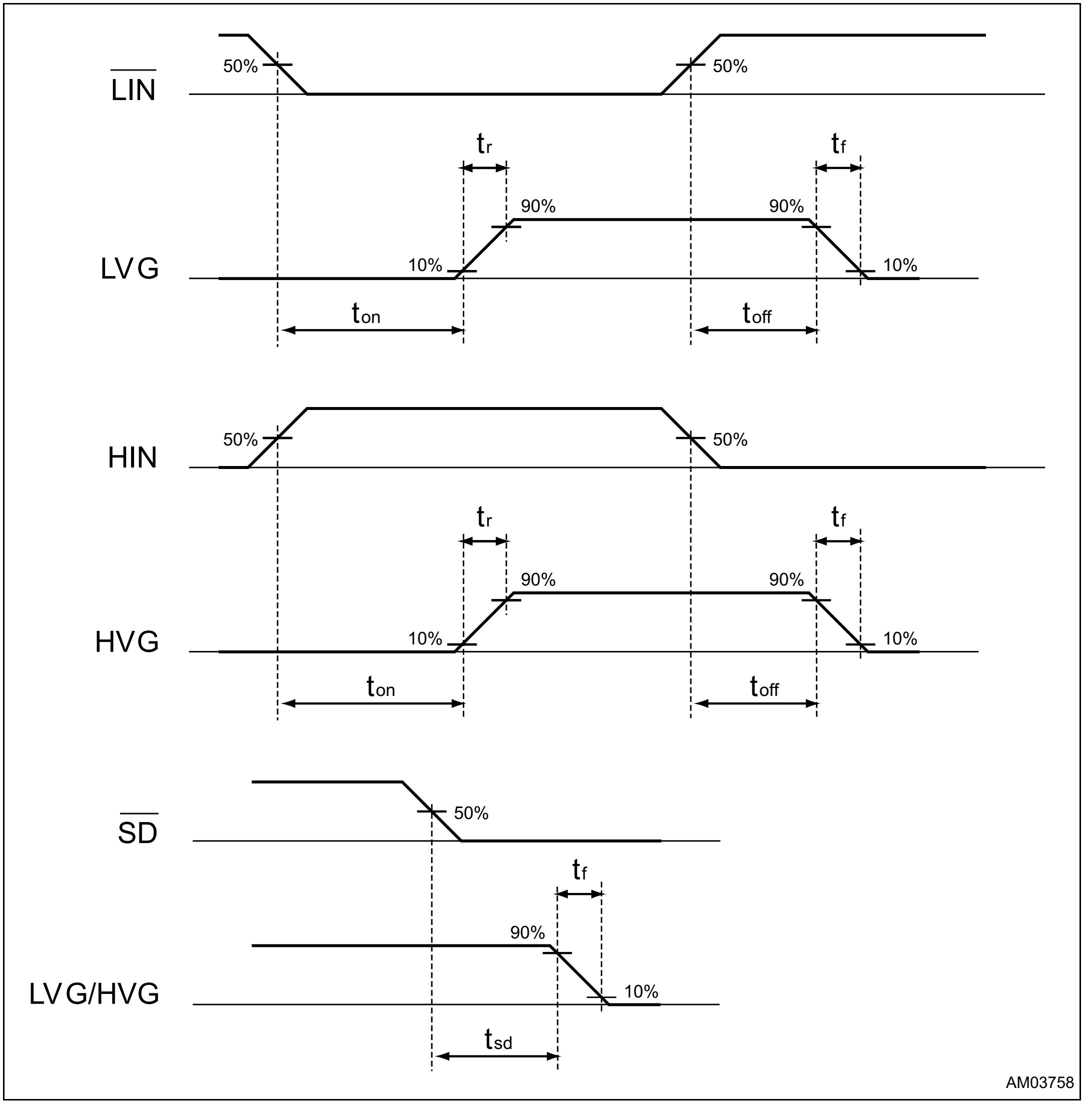
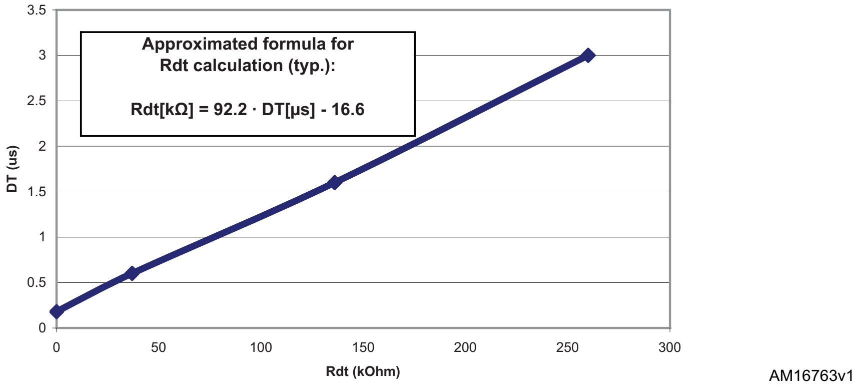


Figure 4. Typical deadtime vs. DT resistor value



5.2 DC operation

Table 7. DC operation electrical characteristics (V_{CC} = 15 V; T_J = + 25 °C)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{cc_hys}	4	V_{cc} UV hysteresis		1.2	1.5	1.8	V
V_{cc_thON}		V_{cc} UV turn-ON threshold		11.5	12	12.5	V
V_{cc_thOFF}		V_{cc} UV turn-OFF threshold		10	10.5	11	V
I_{qccu}		Undervoltage quiescent supply current	V_{cc} = 9.5 V $\overline{SD}$ = 5 V; $\overline{LIN}$ = 5 V; HIN = GND; R_{DT} = 0 Ω; CP+ = GND; CP- = 5 V		100	150	µA
I_{qcc}		Quiescent current	V_{cc} = 15 V $\overline{SD}$ = 5 V; $\overline{LIN}$ = 5 V; HIN = GND; R_{DT} = 0 Ω; CP+ = GND; CP- = 5 V		500	1000	µA
Bootstrapped supply voltage section(1)							
V_{BO_hys}	14 - 12	V_{BO} UV hysteresis		1.2	1.5	1.8	V
V_{BO_thON}		V_{BO} UV turn-ON threshold		10.6	11.5	12.4	V
V_{BO_thOFF}		V_{BO} UV turn-OFF threshold		9.1	10	10.9	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	V_{BO} = 9 V $\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V; R_{DT} = 0 Ω; CP+ = GND; CP- = 5 V		70	110	µA
I_{QBO}		V_{BO} quiescent current	V_{BO} = 15 V $\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V; R_{DT} = 0 Ω; CP+ = GND; CP- = 5 V		200	240	µA
I_{LK}		High voltage leakage current	V_{hvg} = V_{out} = V_{boot} = 600 V			10	µA
$R_{DS(on)}$		Bootstrap driver on resistance(2)	LVG ON		120		W
Driving buffer section							
I_{so}	10, 13	High/low-side source short-circuit current	V_{IN} = V_{ih} (t_p < 10 µs)	200	290		mA
I_{si}		High/low-side sink short-circuit current	V_{IN} = V_{il} (t_p < 10 µs)	250	430		mA
Logic inputs							
V_{il}	1, 2, 3	Low level logic threshold		0.8		1.1	V
V_{ih}		High level logic threshold voltage		1.9		2.25	V
V_{il_S}	1, 3	Single input voltage	$\overline{LIN}$ and HIN connected together and floating			0.8	V

Table 7. DC operation electrical characteristics (V_{CC} = 15 V; T_J = + 25 °C) (continued)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{HINh}	3	HIN logic “1” input bias current	HIN = 15 V	110	175	260	µA
I_{HINl}		HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINl}	1	$\overline{\text{LIN}}$ logic “0” input bias current	$\overline{\text{LIN}}$ = 0 V	3	6	20	µA
I_{LINh}		$\overline{\text{LIN}}$ logic “1” input bias current	$\overline{\text{LIN}}$ = 15 V			1	µA
I_{SDh}	2	$\overline{\text{SD}}$ logic “1” input bias current	$\overline{\text{SD}}$ = 15 V	10	40	100	µA
I_{SDl}		$\overline{\text{SD}}$ logic “0” input bias current	$\overline{\text{SD}}$ = 0 V			1	µA

1. $V_{BO} = V_{BOOT} - V_{OUT}$.
2. $R_{DS(on)}$ is tested in the following way: $R_{DS(on)} = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1(V_{CC},V_{BOOT1}) - I_2(V_{CC},V_{BOOT2})]$ where I_1 is pin 14 current when $V_{BOOT} = V_{BOOT1}$, I_2 when $V_{BOOT} = V_{BOOT2}$.

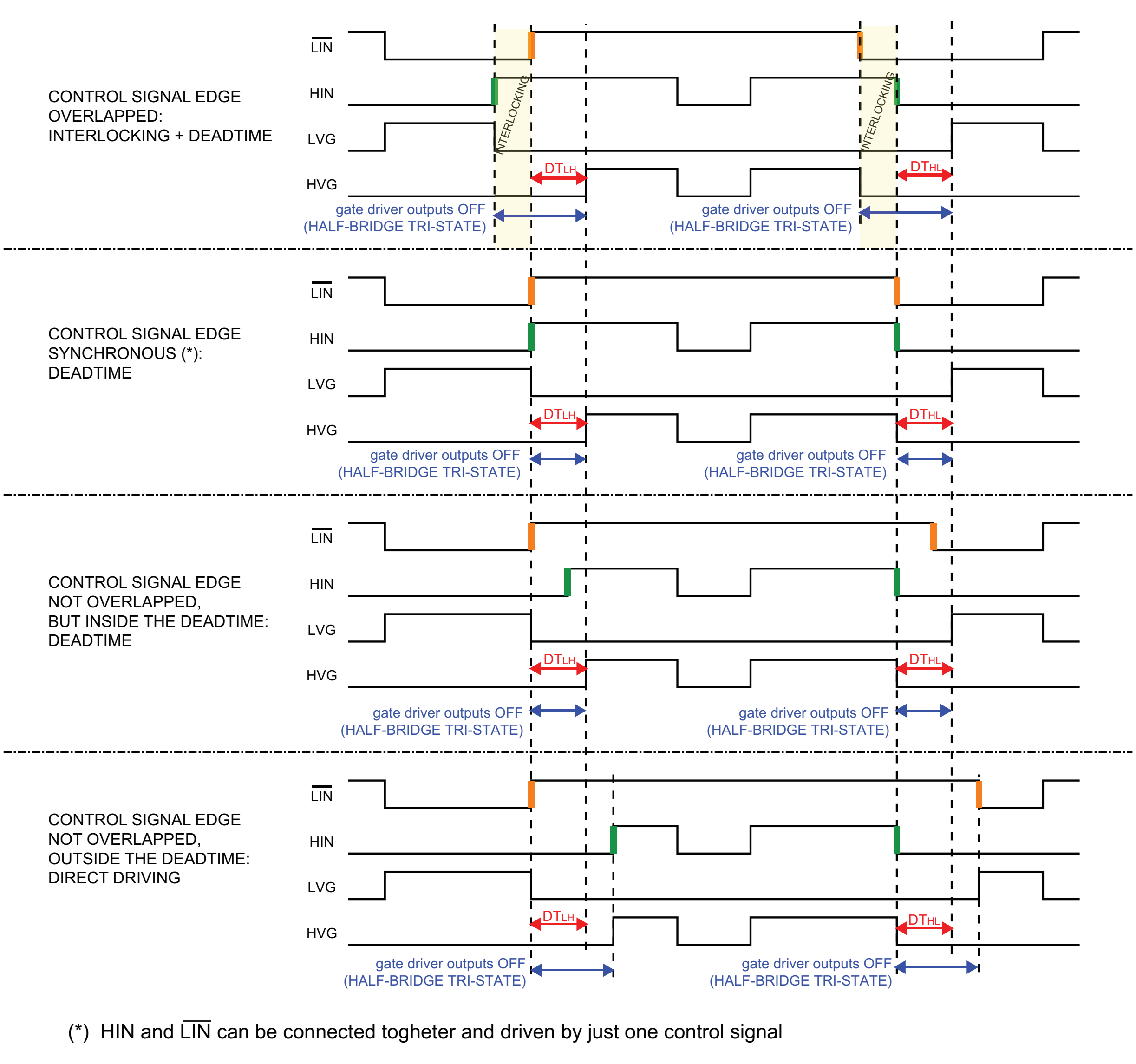
Table 8. Sense comparator[1] (V_{CC} = 15 V, T_J = +25 °C)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	8, 9	Input offset voltage		-15		15	mV
I_{ib}	8, 9	Input bias current	V_{CP+} = 1 V, V_{CP-} = 0.5 V			1	µA
V_{ol}	2	Open-drain low level output voltage	I_{od} = - 3 mA V_{CP+} = 1 V; V_{CP-} = 0.5 V;			0.5	V
t_{d_comp}		Comparator delay	R_{pull} = 100 kΩ to 5 V on $\overline{\text{SD}}$/OD pin; V_{CP-} = 0.5 V; voltage step on CP+ = 0 to 3.3 V		90	130	ns
SR	2	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ		60		V/µs

1. Comparator is disabled when V_{cc} is in UVLO condition.

6 Waveform definitions

Figure 5. Deadtime and interlocking waveform definitions



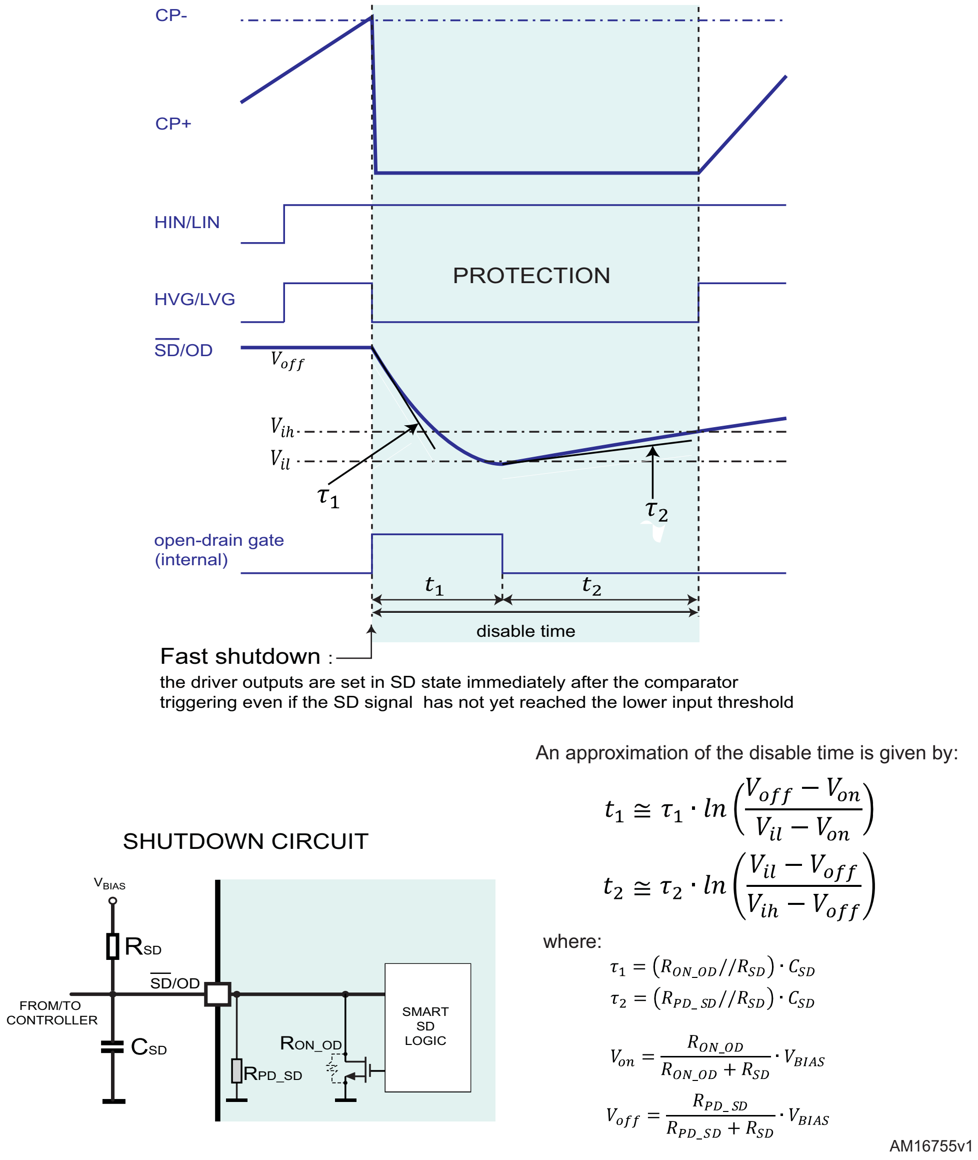
(*) HIN and $\overline{\text{LIN}}$ can be connected togheter and driven by just one control signal

7 Smart shutdown function

The L6391 device integrates a comparator committed to the fault sensing function. Both comparator's inputs are available on pins 8 and 9. For example, applying a voltage reference to CP- and connecting the CP+ to an external shunt resistor, a simple overcurrent detection function can be implemented.

The output signal of the comparator is fed to an integrated MOSFET with the open-drain output available on the pin 2, shared with the $\overline{\text{SD}}$ input. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low level leaving the half-bridge in tristate.

Figure 6. Smart shutdown timing waveforms



Fast shutdown : the driver outputs are set in SD state immediately after the comparator triggering even if the SD signal has not yet reached the lower input threshold

An approximation of the disable time is given by:

$$t_1 \cong \tau_1 \cdot ln\left(\frac{V_{off} - V_{on}}{V_{il} - V_{on}}\right)$$

$$t_2 \cong \tau_2 \cdot ln\left(\frac{V_{il} - V_{off}}{V_{ih} - V_{off}}\right)$$

where:

$$\tau_1 = (R_{ON\_OD} // R_{SD}) \cdot C_{SD}$$

$$\tau_2 = (R_{PD\_SD} // R_{SD}) \cdot C_{SD}$$

$$V_{on} = \frac{R_{ON\_OD}}{R_{ON\_OD} + R_{SD}} \cdot V_{BIAS}$$

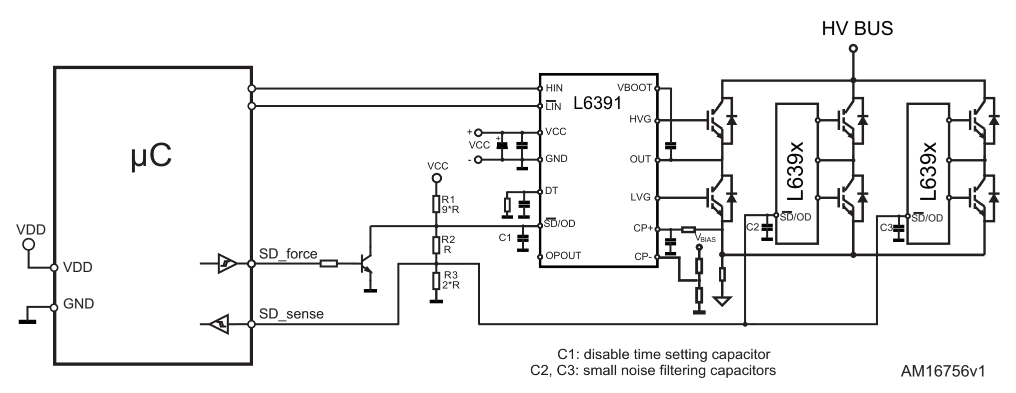
$$V_{off} = \frac{R_{PD\_SD}}{R_{PD\_SD} + R_{SD}} \cdot V_{BIAS}$$

In common overcurrent protection architectures, the comparator output is usually connected to the $\overline{\text{SD}}$ input and an RC network is connected to this $\overline{\text{SD}}$/OD line in order to provide a monostable circuit, which implements a protection time following the fault condition. Differently from the common fault detection systems, the L6391 smart shutdown architecture allows immediate turn-off of the output gate driver in case of fault, by minimizing the propagation delay between the fault detection event and the current output switch-off. In fact the time delay between the fault and the output turn-off is no longer dependent on the RC value of the external network connected to the $\overline{\text{SD}}$/OD pin. In the smart shutdown circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering. At the same time, the internal logic turns on the open-drain output and holds it on until the $\overline{\text{SD}}$ voltage goes below the $\overline{\text{SD}}$ logic input lower threshold. When such threshold is reached, the open-drain output is turned off, allowing the external pull-up to recharge the capacitor. The driver outputs restart following the input pins as soon as the voltage at the $\overline{\text{SD}}$/OD pin reaches the higher threshold of the $\overline{\text{SD}}$ logic input. The smart shutdown system gives the possibility to increase the time constant of the external RC network (that determines the disable time after the fault event) up to very large values without increasing the delay time of the protection.

Any external signal provided to the $\overline{\text{SD}}$ pin is not latched and can be used as control signal in order to perform, for instance, PWM chopping through this pin. In fact when a PWM signal is applied to the $\overline{\text{SD}}$ input and the logic inputs of the gate driver are stable, the outputs switch from the low level to the state defined by the logic inputs and vice versa.

In some applications, it may be useful to latch the driver in the shutdown condition for an arbitrary time, until the controller decides to reset it to normal operation. This may, for example, be achieved by a circuit as the one shown in *Figure 7*. When the open-drain starts pulling down the $\overline{\text{SD}}$/OD pin, the external latch turns on and keeps the pin to GND, preventing it from being pulled up again once the $\overline{\text{SD}}$ logic input lower threshold is reached and the internal open-drain turns off. One pin of the controller is used to release the external latch, and one to externally force a shutdown condition and also to read the status of the $\overline{\text{SD}}$/OD pin.

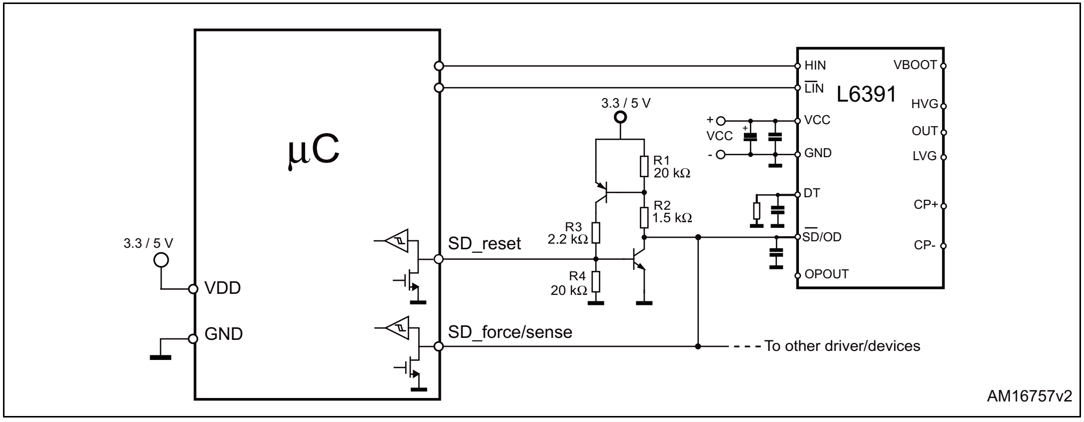
Figure 7. Protection latching circuit



C1: disable time setting capacitor
C2, C3: small noise filtering capacitors

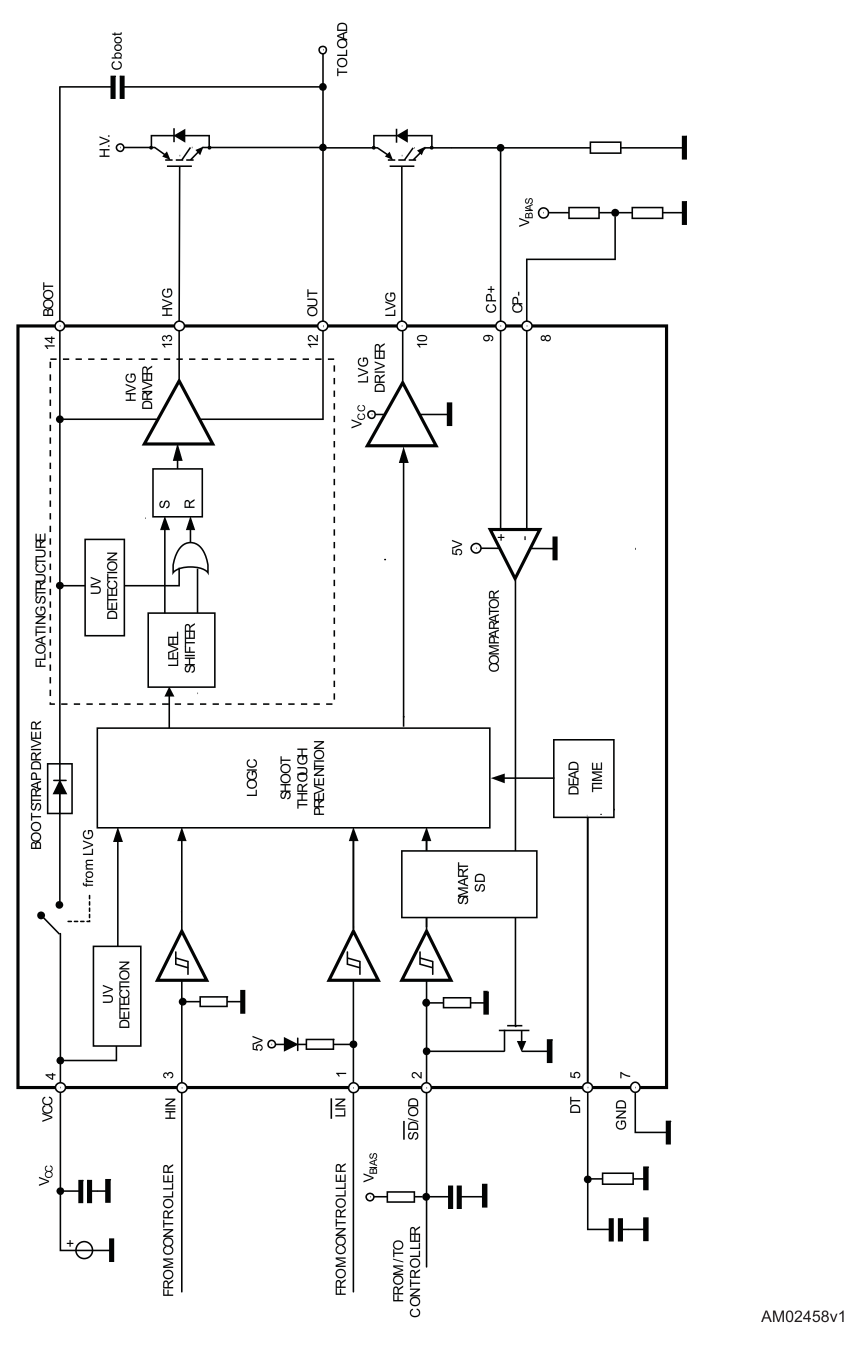
In applications using only one L6391 for the protection of different legs (such as a single-shunt inverter, for example), the resistor divider, shown in *Figure 8*, can be implemented. This simple network allows the $\overline{\text{SD}}$ pins of the other devices to reach a voltage lower than L6391 V_{il}, so that each device can get its low logic level regardless of part to part variations of the thresholds.

Figure 8. $\overline{\text{SD}}$ level shifting circuit



8 Typical application diagram

Figure 9. Application diagram



9 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is usually accomplished by a high voltage fast recovery diode (*Figure 10*). In the L6391 device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with diode in series, as shown in *Figure 11*. An internal charge pump (*Figure 11*) provides the DMOS driving voltage.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

Equation 2

$$C_{BOOT} >>> C_{EXT}$$

if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop is 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has also to take into account the leakage and quiescent losses.

HVG steady-state consumption is lower than 240 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply C_{EXT} with 1.2 µC. This charge on a 1 µF capacitor means a voltage drop of 1.2 V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$ (typical value: 120 Ω). At low frequency this drop can be neglected. Anyway, the rise of frequency has to take into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge} R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{DS(on)}$$

where Q_{gate} is the gate charge of the external power MOS, $R_{DS(on)}$ is the on resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs. In fact:

Equation 4

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 120\Omega \sim 0.7V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 10. Bootstrap driver with high voltage fast recovery diode

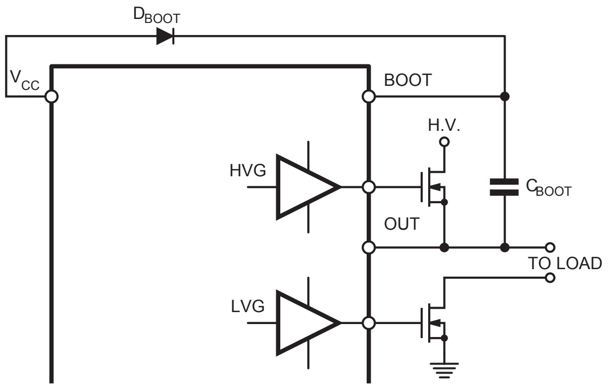
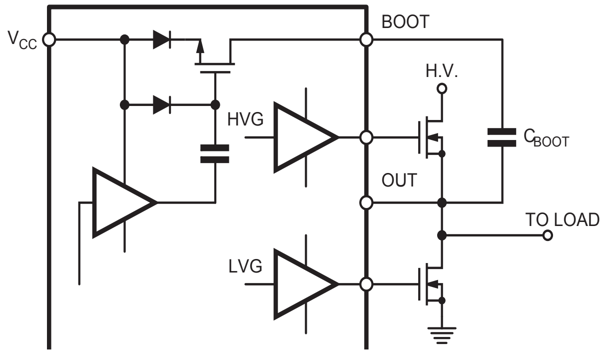


Figure 11. Bootstrap driver with internal charge pump



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

SO-14 package information

Figure 12. SO-14 package outline

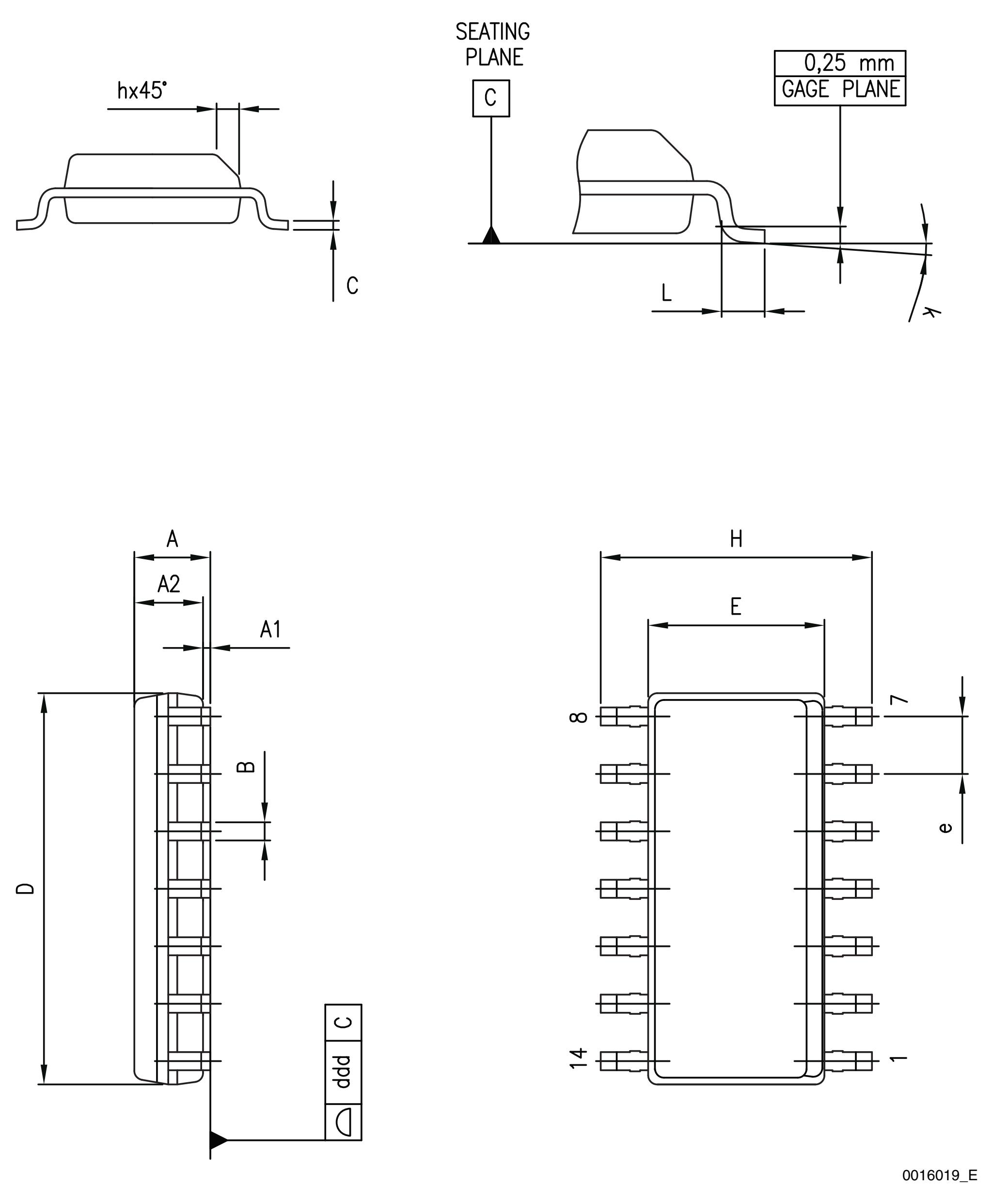
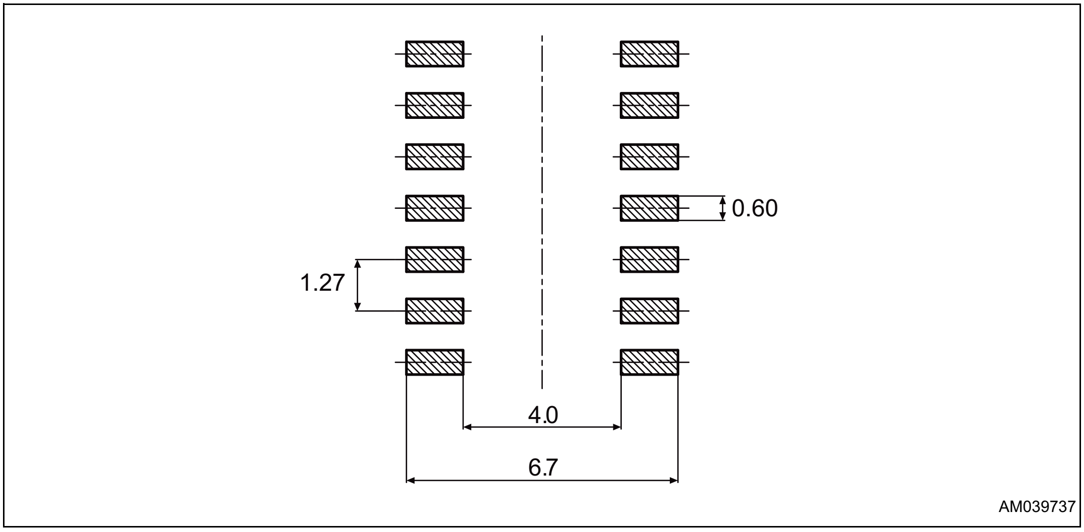


Table 9. SO-14 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	1.35		1.75
A1	0.10		0.25
A2	1.10		1.65
B	0.33		0.51
C	0.19		0.25
D	8.55		8.75
E	3.80		4.00
e		1.27	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
K	0		8
e		0.40	
ddd			0.10

Figure 13. SO-14 footprint



11 Order codes

Table 10. Order codes

Order code	Package	Packaging
L6391D	SO-14	Tube
L6391DTR	SO-14	Tape and reel

12 Revision history

Table 11. Document revision history

Date	Revision	Changes
14-Dec-2010	1	First release.
10-May-2013	2	Added HBM parameter to *Table 3*. Added I_{QBO} max. value to *Table 7*. Changed V_{il} and V_{ih} min. and max. values in *Table 7*. Added note to *Table 8*. Updated *Section 7* and *Section* . Changed *Figure 6* and added *Figure 7* and *Figure 8*. Updated SO-14 mechanical data. Updated DIP-14 mechanical data.
11-Sep-2015	3	Removed DIP-14 package from the entire document. Updated *Table 4 on page 6* (updated $R_{th(JA)}$ value). Moved *Table 10 on page 21* (moved from page 1 to page 21, updated titles. Updated *Table 3 on page 6* (updated ESD parameter and value). Updated note *1.*and *2.* below *Table 7 on page 10* (minor modifications, replaced V_{CBOOTx} by V_{BOOTx}). Added *Figure 13 on page 20*. Updated cross-references throughout document. Minor modifications throughout document.