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1 Block diagram and pin configuration

Figure 1. Block diagram

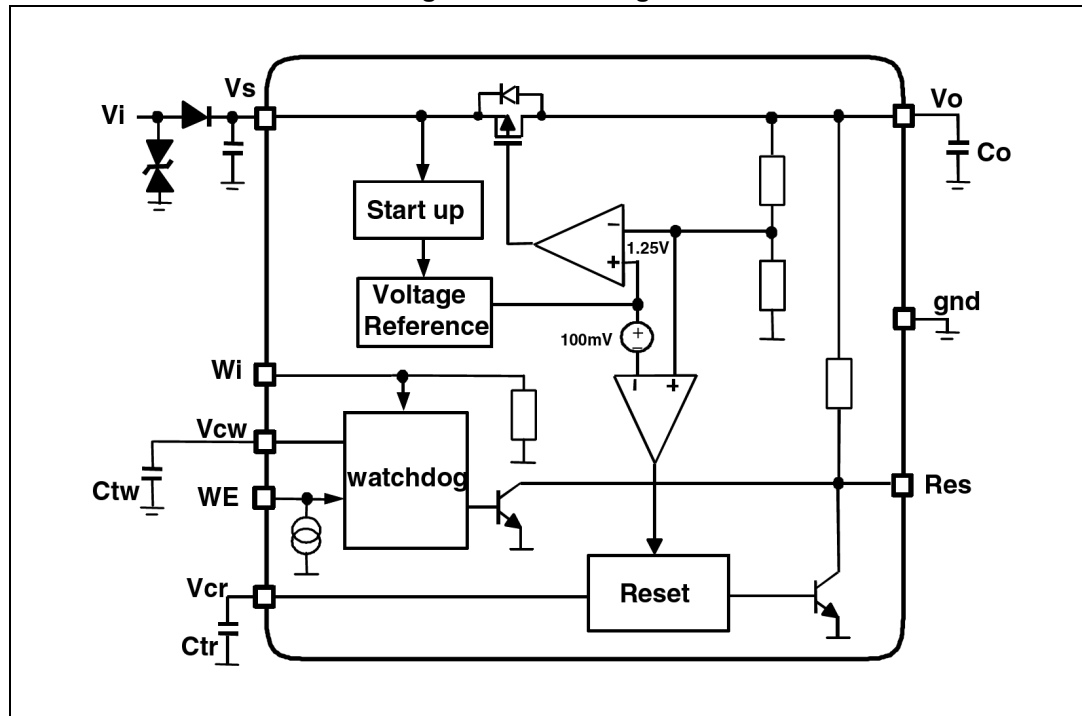


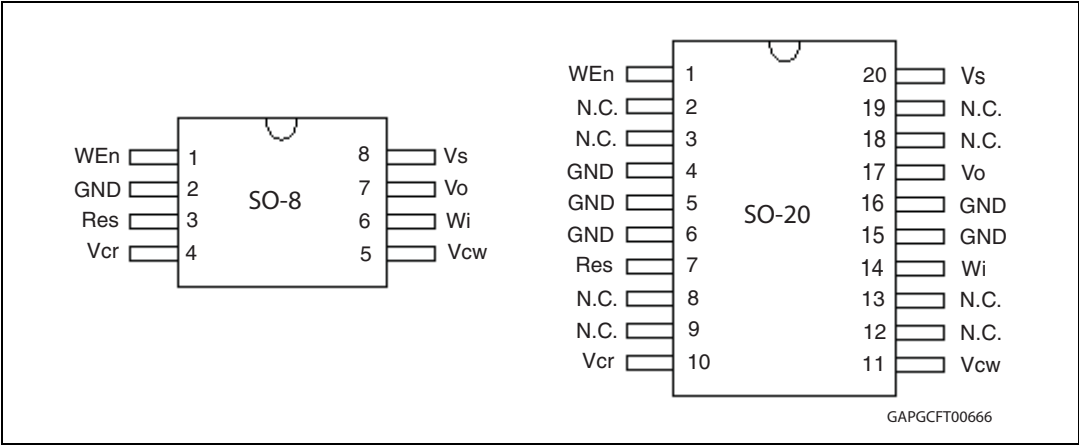
Table 2. Pins description

Pin name	SO-8(D)	S0-20(MD)	Function
WE _n	1	1	Watchdog Enable input If high watchdog functionality is active.
Gnd	2	4	Ground reference
Gnd		5, 6, 15, 16	Ground. Connected these pins to a heat spreader ground
Res	3	7	Reset output. It is pulled down when output voltage goes below V _{o_th} or frequency at Wi is too low.
Vcr	4	10	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (t _{rd})
Vcw	5	11	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
Wi	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.

Table 2. Pins description (continued)

Pin name	SO-8(D)	S0-20(MD)	Function
V _o	7	17	Voltage regulator output Block to ground with a capacitor >100 nF (needed for regulator stability)
V _S	8	20	Supply voltage Block to ground directly at IC pin with a capacitor
N.C.		2, 3, 8, 9, 12, 13, 18, 19	Not connected

Figure 2. Pins configuration (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{VSDC}	DC supply voltage	-0.3 to 40	V
I_{VSDC}	Input current	Internally limited	
V_{Vo}	DC output voltage	-0.3 to 6	V
I_{Vo}	DC output current	Internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{Od}	Open Drain output voltage	-0.3 to $V_{Vo} + 0.3$	V
I_{Od}	Open Drain output current	Internally limited	
V_{Cr}	Reset delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{CW}	Watchdog delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{WEn}	Watchdog Enable input voltage	-0.3 to 40	V
T_j	Junction temperature	-40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	S0-8	S0-12+4+4	Unit
$R_{th-jamb}$	Thermal resistance junction to ambient	130 to 180	50 ⁽¹⁾	°C/W

1. With 6 sq. cm on board heat sink.

2.3 Electrical characteristics

$V_S = 5.6 \text{ V to } 31 \text{ V}$, $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ unless otherwise specified.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	V_{O_ref}	Output voltage	$V_S = 5.6 \text{ to } 31 \text{ V}$; $I_O = 1 \text{ to } 150 \text{ mA}$	4.85	5.0	5.15	V
V_O	I_{short_13}	Short circuit current	$V_S = 13.5 \text{ V}^{(1)}$	160	210	250	mA
V_O	I_{lim}	Output current limitation	$V_S = 13.5 \text{ V}^{(1)}$	170	250	290	mA
V_S, V_O	V_{line}	Line regulation voltage	$V_S = 5.6 \text{ to } 31 \text{ V}$; $I_O = 1 \text{ to } 150 \text{ mA}$			25	mV
V_O	V_{load}	Load regulation voltage	$I_O = 1 \text{ to } 150 \text{ mA}$			25	mV
V_S, V_O	V_{dp}	Drop voltage	$I_O = 150 \text{ mA}$		180	400	mV
V_S, V_O	SVR	Ripple rejection	$f_r = 100 \text{ Hz}$	55			dB
V_S, V_O	I_{qs_1}	Current consumption with watchdog not active $I_{qs_1} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$; $I_O < 1 \text{ mA}$; $WE_n = \text{low}$		69	115	μA
V_S, V_O	I_{qs_10}	Current consumption with watchdog not active $I_{qs_10} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$; $I_O = 10 \text{ mA}$; $WE_n = \text{low}$		127	300	μA
V_S, V_O	I_{qs_50}	Current consumption with watchdog not active $I_{qs_50} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$; $I_O = 50 \text{ mA}$; $WE_n = \text{low}$		498	900	μA
V_S, V_O	I_{qs_150}	Current consumption with watchdog not active $I_{qs_150} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$; $I_O = 150 \text{ mA}$; $WE_n = \text{low}$		1.40	2	mA
V_S, V_O	I_{qn_1}	Current consumption with watchdog active $I_{qn_1} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$; $I_O < 1 \text{ mA}$; $WE_n = \text{high}$		110	170	μA
V_S, V_O	I_{qn_10}	Current consumption with watchdog active $I_{qn_10} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$; $I_O = 10 \text{ mA}$; $WE_n = \text{high}$		168	350	μA
V_S, V_O	I_{qn_50}	Current consumption with watchdog active $I_{qn_50} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$; $I_O = 50 \text{ mA}$; $WE_n = \text{high}$		538	1000	μA
V_S, V_O	I_{qn_150}	Current consumption with watchdog active $I_{qn_150} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$; $I_O = 150 \text{ mA}$; $WE_n = \text{high}$		1.45	2	mA
	T_w	Thermal protection temperature		150		190	$^\circ\text{C}$
	T_{w_hy}	Thermal protection temperature hysteresis			10		$^\circ\text{C}$

1. See [Figure 3](#).

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Res	Vres_l	Reset output low voltage	$R_{\text{ext}} = 5 \text{ k}\Omega$ to V_0 ; $V_0 > 1 \text{ V}$			0.4	V
Res	$I_{\text{Res_lkg}}$	Reset output high leakage current	$V_{\text{Res}} = 5 \text{ V}$			1	μA
Res	R_{Res}	Pull up internal resistance	Versus V_0	10	20	50	$\text{k}\Omega$
Res	V_{0_th}	Reset threshold voltage	$V_S = 5.6$ to 31 V ; $I_0 = 1$ to 150 mA	6%	8%	10%	Below V_{0_ref}
Vcr	V_{rlth}	Reset timing low threshold	$V_S = 13.5 \text{ V}$	10%	13%	16%	V_{0_ref}
Vcr	V_{rhth}	Reset timing high threshold	$V_S = 13.5 \text{ V}$	44%	47%	50%	V_{0_ref}
Vcr	I_{cr}	Charge current	$V_S = 13.5 \text{ V}$	8	15	30	μA
Vcr	I_{dr}	Discharge current	$V_S = 13.5 \text{ V}$	8	15	30	μA
Res	T_{rr_2}	Reset reaction time ⁽¹⁾	$V_0 = V_{0_th} - 100 \text{ mV}$	100	250	700	μs
Res	T_{rd}	Reset delay time	$V_S = 13.5 \text{ V}$; $C_{tr} = 1 \text{ nF}$	65	115	165	ms

1. When V_0 becomes lower than 4 V, the reset reaction time decreases down to 2 μs assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Wi	V_{ih}	Input high voltage	$V_S = 13.5 \text{ V}$	3.5			V
Wi	V_{il}	Input low voltage	$V_S = 13.5 \text{ V}$			1.5	V
Wi	V_{ih}	Input hysteresis	$V_S = 13.5 \text{ V}$		500		mV
Wi	R_{wi}	Pull down resistor	$V_S = 13.5 \text{ V}$	30	100	250	$\text{k}\Omega$
Vcw	V_{whth}	High threshold	$V_S = 13.5 \text{ V}$	44%	47%	50%	V_{0_ref}
Vcw	V_{wlth}	Low threshold	$V_S = 13.5 \text{ V}$	10%	13%	16%	V_{0_ref}
Vcw	I_{cwc}	Charge current	$V_S = 13.5 \text{ V}$; $V_{cw} = 0.1 \text{ V}$	5	10	20	μA
Vcw	I_{cwd}	Discharge current	$V_S = 13.5 \text{ V}$; $V_{cw} = 2.5 \text{ V}$	1.25	2.5	5	μA
Vcw	T_{wop}	Watchdog period	$V_S = 13.5 \text{ V}$; $C_{tw} = 47 \text{ nF}$	20	40	80	ms
Res	t_{wol}	Watchdog output low time	$V_S = 13.5 \text{ V}$; $C_{tw} = 47 \text{ nF}$	4	8	16	ms

Table 8. Watchdog Enable

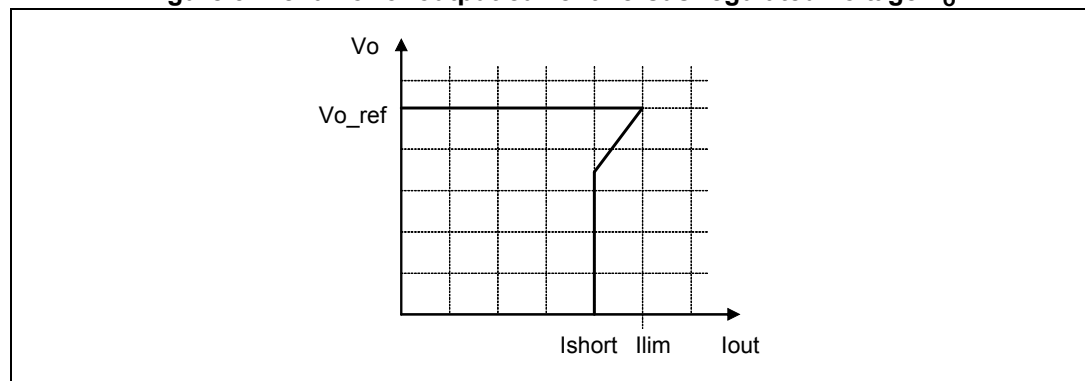
Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
WE _n	V _{WE_n_l}	Enable input low voltage				1	V
WE _n	V _{WE_n_h}	Enable input high voltage		3			V
WE _n	V _{WE_n_hy}	Enable input hysteresis		600	920	1300	mV
WE _n	I _{leak}	Pull down current	V _S = 13.5 V	1	2.5	5	μA

3 Application information

3.1 Voltage regulator

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure a very low dropout voltage at current up to 150 mA is obtained. The output voltage is regulated up to transient input supply voltage of 40 V. No functional interruption due to over-voltage pulses is generated. The voltage Regulator is always active and not depending on the state of WE_n input pin. A short circuit protection to GND is provided.

Figure 3. Behavior of output current versus regulated voltage V_o



3.2 Reset

The reset circuit supervises the output voltage V_o . The V_{o_th} reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than V_{o_th} then Res goes low with a reaction time t_{rr} . The reset low signal is guaranteed for an output voltage V_o greater than 1 V.

When the output voltage becomes higher than V_{o_th} then Res goes high with a delay t_{rd} . This delay is obtained by an internal oscillator.

The oscillator period is given by:

$$T_{osc} = [(V_{rth} - V_{rlth}) \times C_{tr}] / I_{cr} + [(V_{rth} - V_{rlth}) \times C_{tr}] / I_{dr}$$

where:

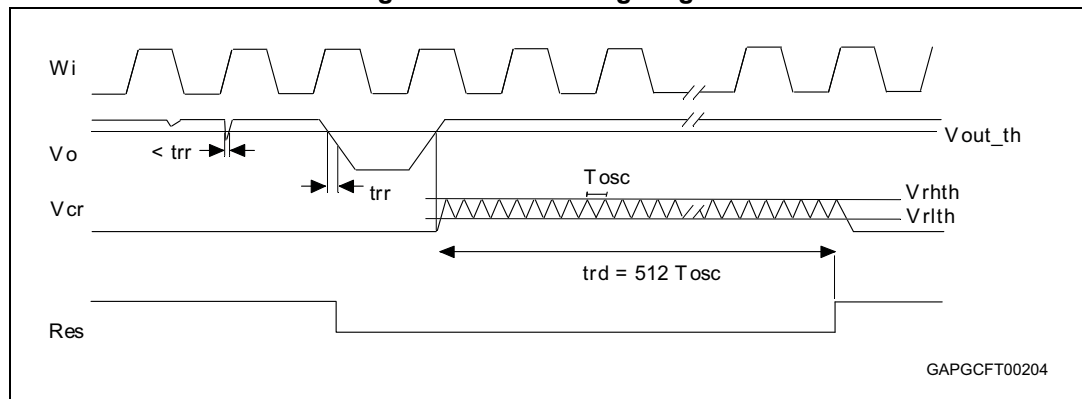
- I_{cr} : is an internally generated charge current
- I_{dr} : is an internally generated discharge current
- V_{rth}, V_{rlth} : are two voltages defined with the output voltage and a resistor output divider
- C_{tr} : is an external capacitance.

t_{rd} is given by:

$$t_{rd} = 512 \times T_{osc}$$

The Reset is always active and not depending on the state of WE_n input pin.

Figure 4. Reset timing diagram



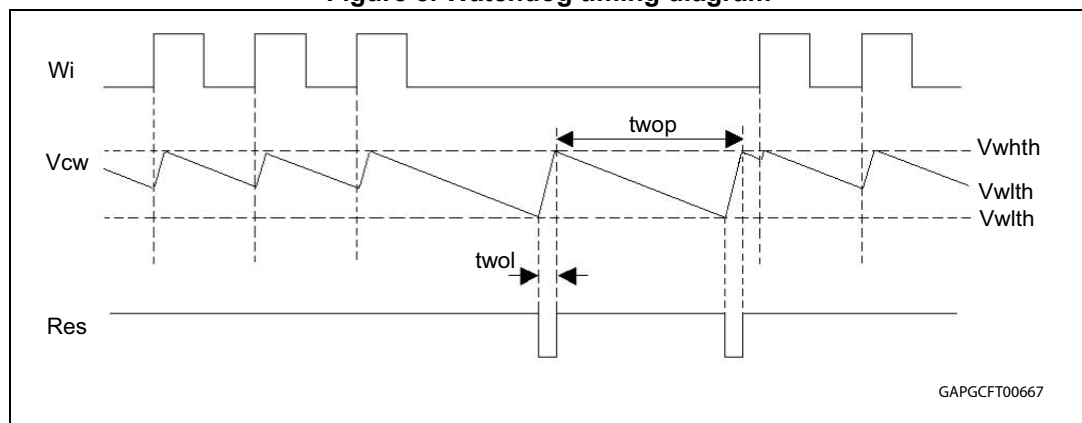
3.3 Watchdog

A connected microcontroller is monitored by the watchdog input W_i . If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, C_{tw} . The watchdog circuit discharges the capacitor C_{tw} with the constant current I_{cwd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time t , during which the micro-controller must output the positive edge, the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times t$$

Every W_i positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{whth} , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor C_{tw} .

Figure 5. Watchdog timing diagram



4 Package and packing information

4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2 SO-8 package information

Figure 6. SO-8 package dimensions

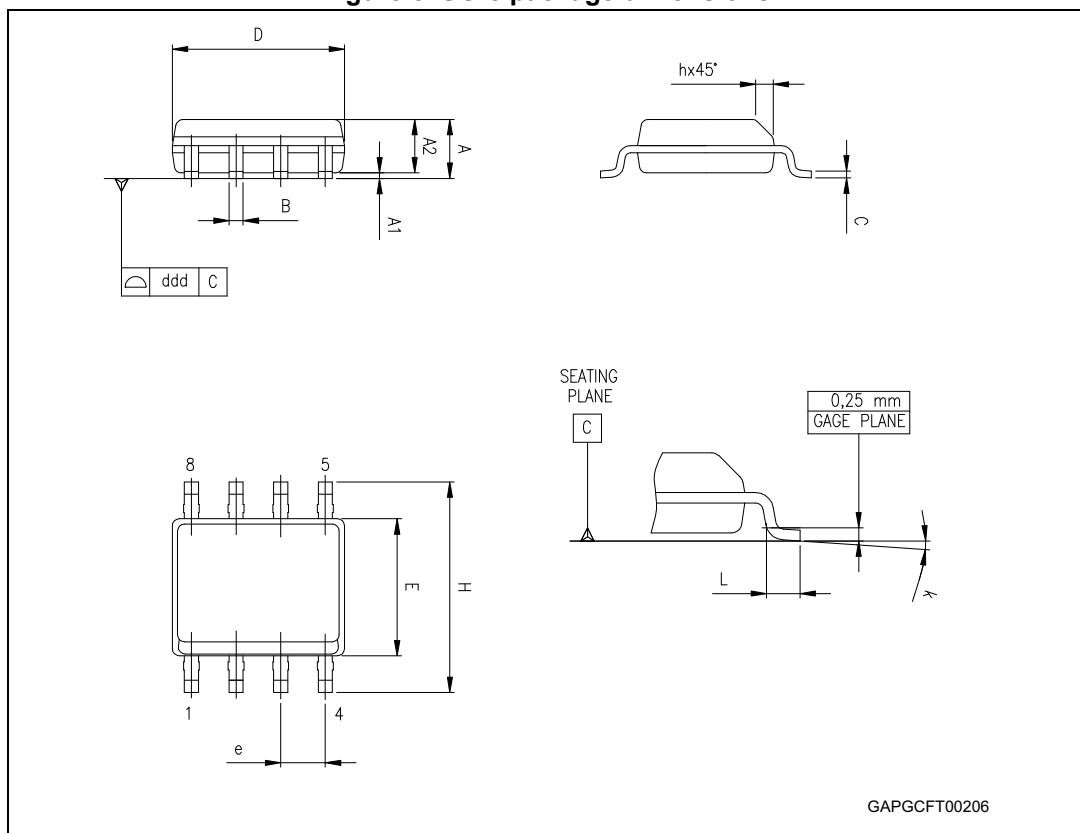


Table 9. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

4.3 SO-20 package information

Figure 7. SO-20 package dimensions

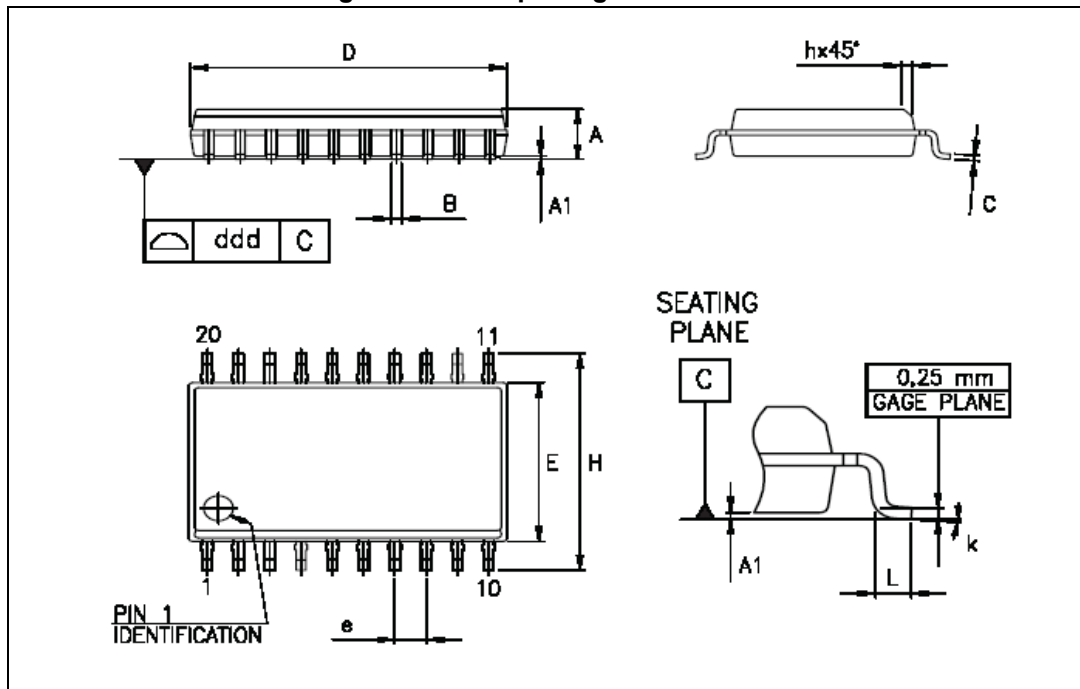


Table 10. SO-20 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D ⁽¹⁾	12.60		13.00
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

1. "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15 mm per side.

4.4 SO-8 packing information

Figure 8. SO-8 tube shipment (no suffix)

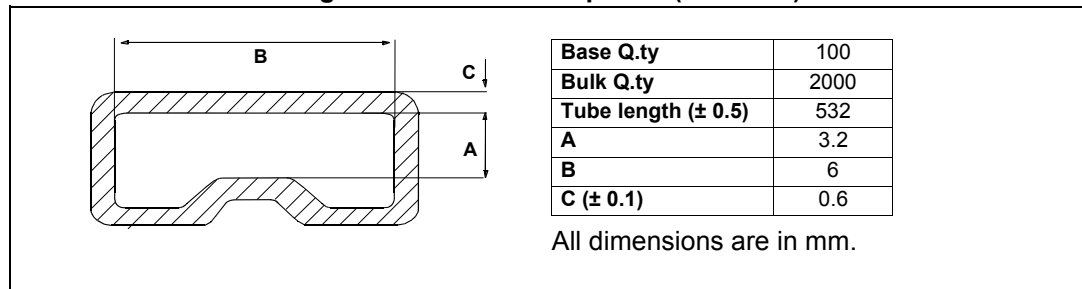
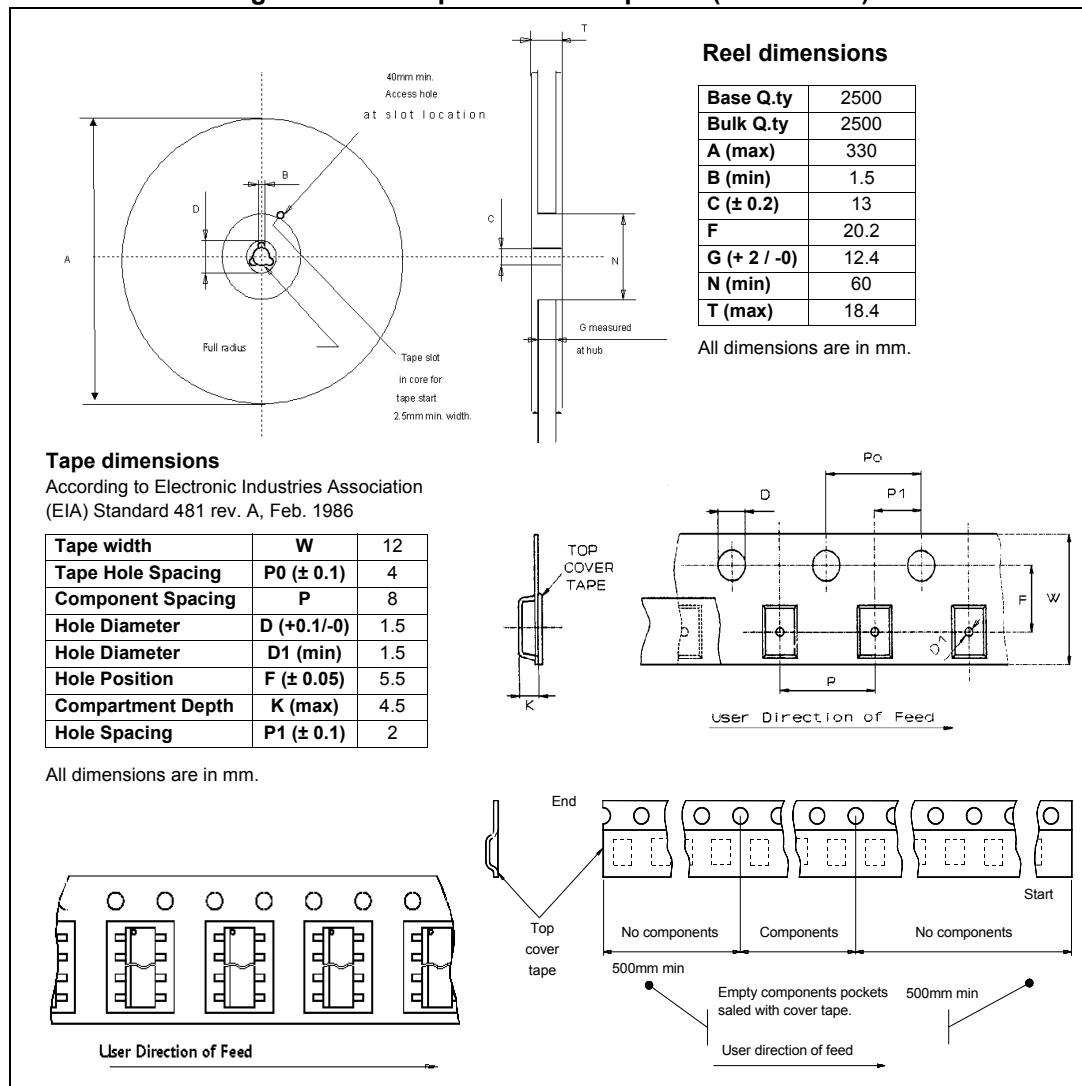


Figure 9. SO-8 tape and reel shipment (suffix “TR”)



4.5 SO-20 packing information

Figure 10. SO-20 tube shipment (no suffix)

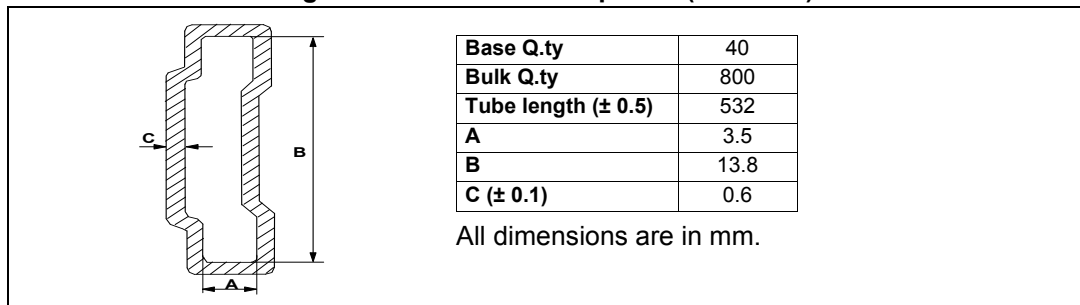
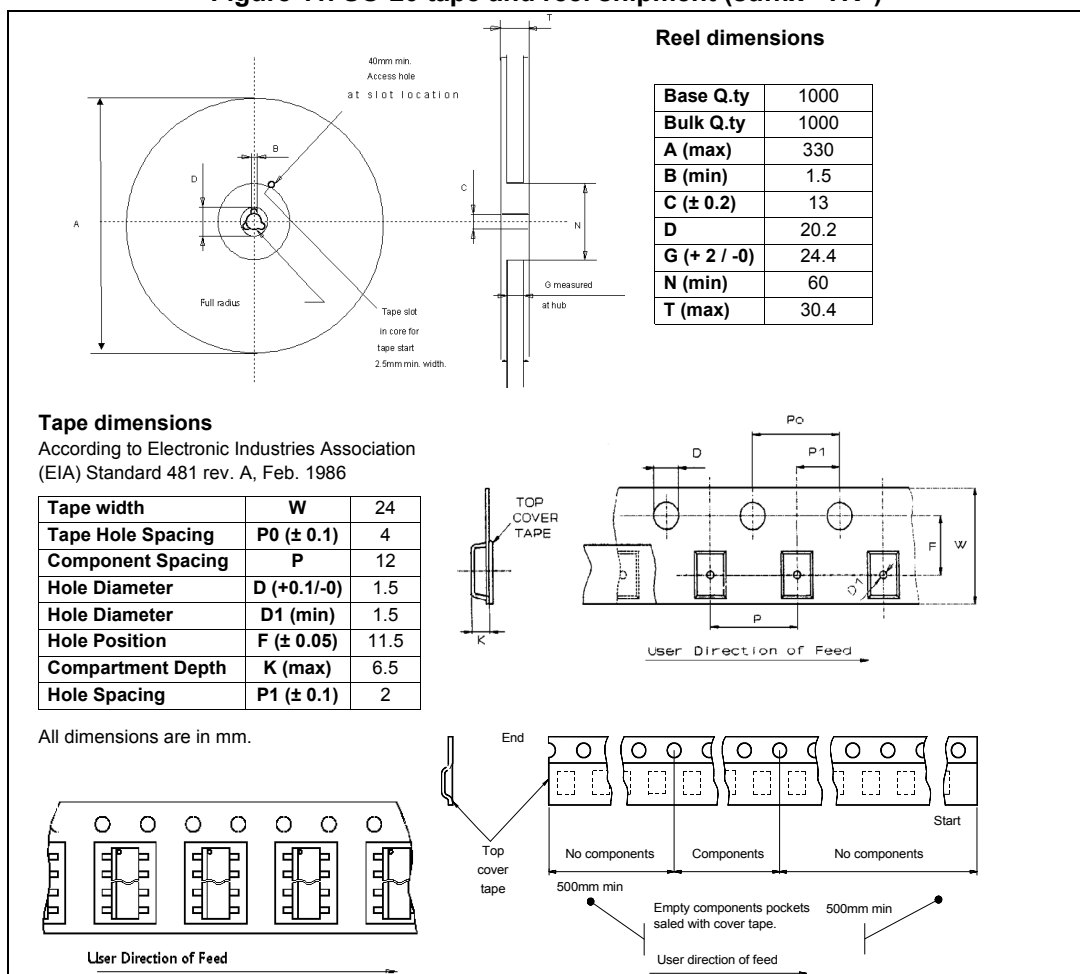


Figure 11. SO-20 tape and reel shipment (suffix "TR")



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
16-Apr-2012	1	Initial release. This document replace the L4989 datasheet.
19-Sep-2013	2	Updated Disclaimer.
01-Oct-2018	3	Updated title and added the feature "AEC-Q100 qualified" in cover page with automotive logo.

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