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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	11.1 7.0	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	24	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	129	mJ	$I_D = 2.9\text{A}$; $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.20	mJ	$I_D = 2.9\text{A}$; $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}	-	-	2.9	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation (Full PAK)	P_{tot}	-	-	28.0	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	4.6	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	24.0	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$
Maximum diode commutation speed ³⁾	di/dt	-	-	500	A/ μs	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$
Insulation withstand voltage for TO-220 FullPAK	V_{ISO}	-	-	2500	V	V_{rms} , $T_C = 25^\circ\text{C}$, $t = 1\text{min}$

2 Thermal characteristics

Table 3 Thermal characteristics TO220 Full PAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.46	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	$^\circ\text{C/W}$	lead
Soldering temperature, wavesoldering only allowed at leads	T_{sld}	-	-	260	$^\circ\text{C}$	1.6mm (0.063 in.) from case for 10s

¹⁾ Limited by $T_{j,max} < 150^\circ\text{C}$, Maximum Duty Cycle $D = 0.5$, TO220 equivalent

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DClk} = 400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	$V_{DS}=V_{GS}$, $I_D=0.2mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=500V$, $V_{GS}=0V$, $T_j=25^\circ C$ $V_{DS}=500V$, $V_{GS}=0V$, $T_j=150^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.45	0.50	Ω	$V_{GS}=13V$, $I_D=2.3A$, $T_j=25^\circ C$ $V_{GS}=13V$, $I_D=2.3A$, $T_j=150^\circ C$
Gate resistance	R_G	-	3	-	Ω	$f=1\text{ MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	433	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	31	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1\text{ MHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	25	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	100	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.9A$, $R_G=3.4\Omega$
Rise time	t_r	-	5	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.9A$, $R_G=3.4\Omega$
Turn-off delay time	$t_{d(off)}$	-	30	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.9A$, $R_G=3.4\Omega$
Fall time	t_f	-	12	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.9A$, $R_G=3.4\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2.3	-	nC	$V_{DD}=400V$, $I_D=2.9A$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	10	-	nC	$V_{DD}=400V$, $I_D=2.9A$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	18.7	-	nC	$V_{DD}=400V$, $I_D=2.9A$, $V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	$V_{DD}=400V$, $I_D=2.9A$, $V_{GS}=0$ to 10V

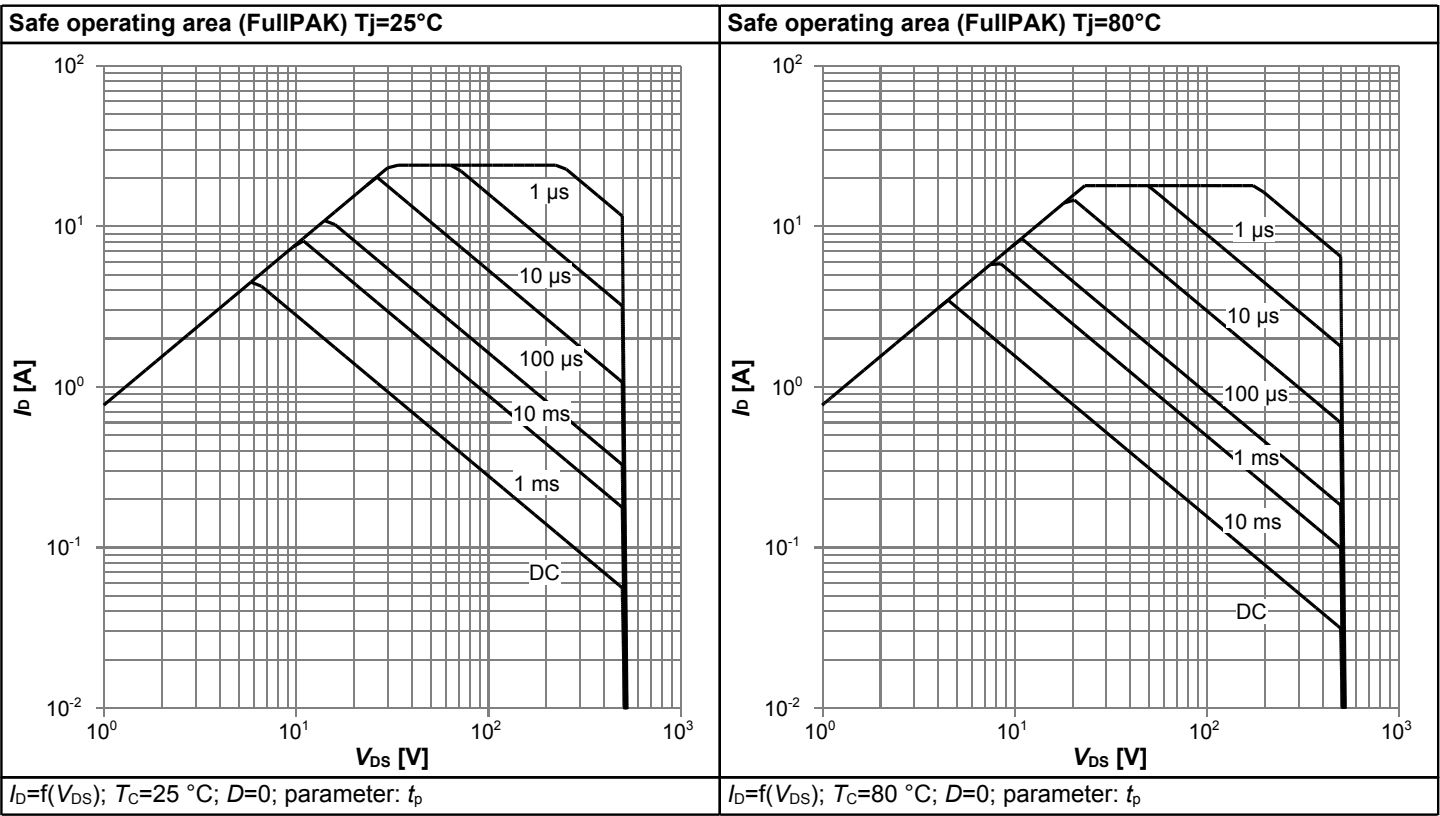
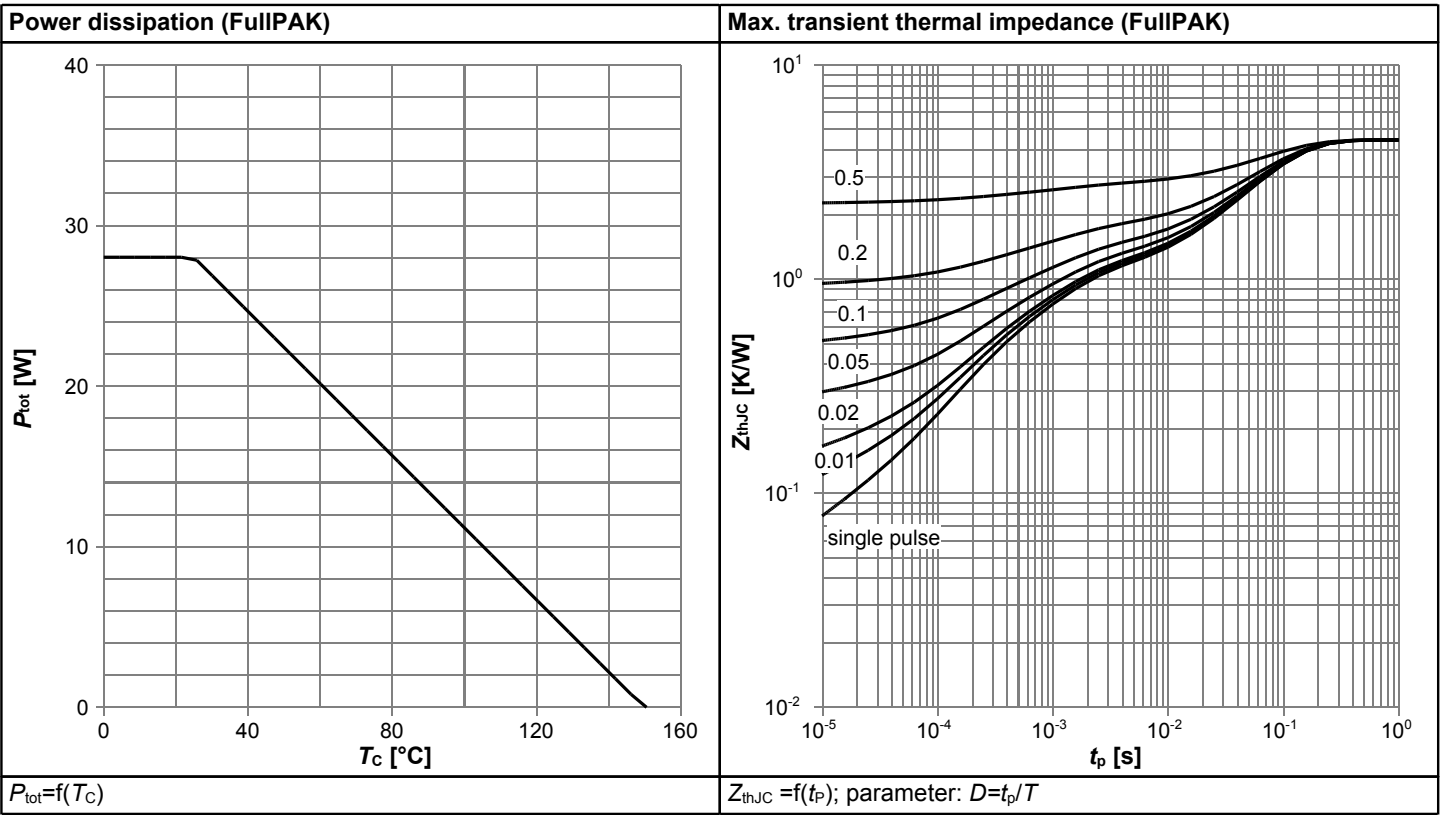
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

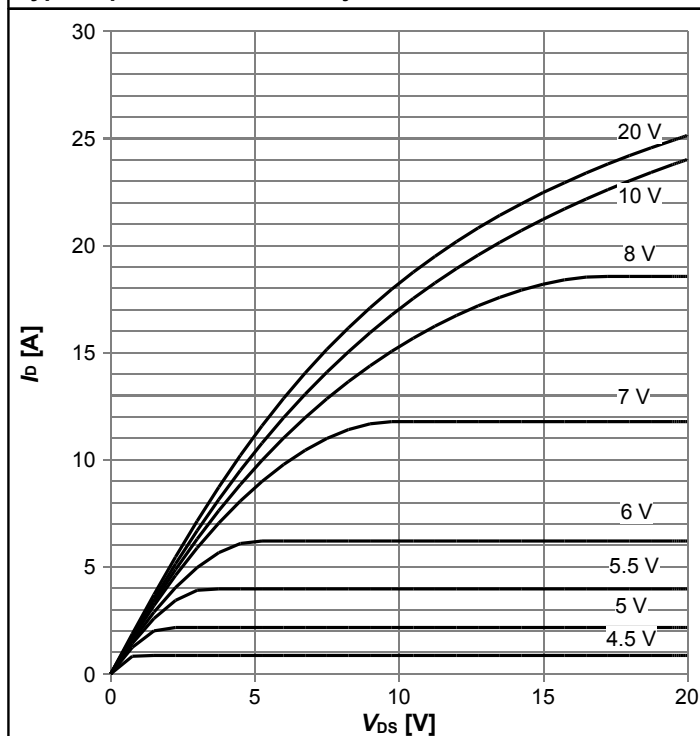
Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.85	-	V	$V_{GS}=0V, I_F=2.9A, T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	180	-	ns	$V_R=400V, I_F=2.9A, di_F/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	-	1.2	-	μC	$V_R=400V, I_F=2.9A, di_F/dt=100A/\mu s$
Peak reverse recovery current	I_{rrm}	-	12	-	A	$V_R=400V, I_F=2.9A, di_F/dt=100A/\mu s$

4 Electrical characteristics diagrams

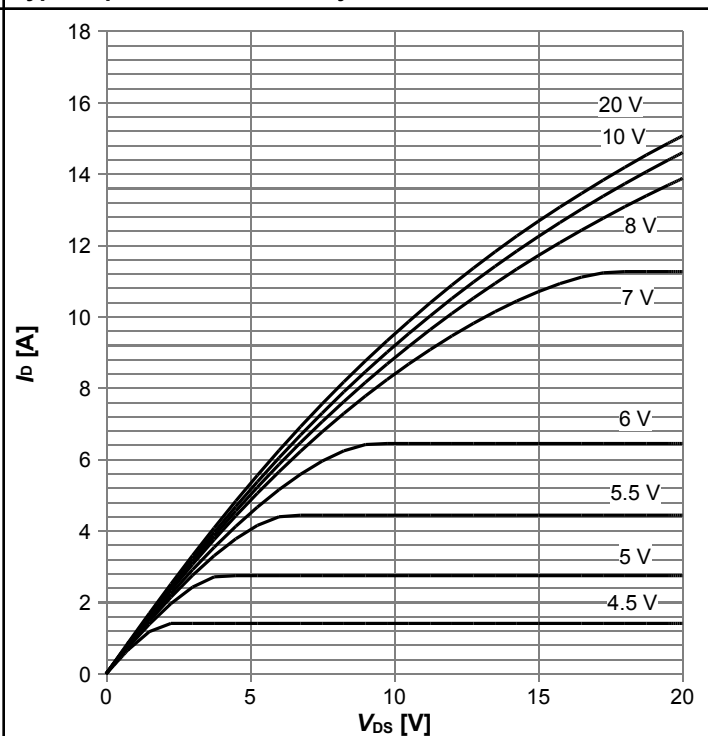


Typ. output characteristics $T_j=25^\circ\text{C}$



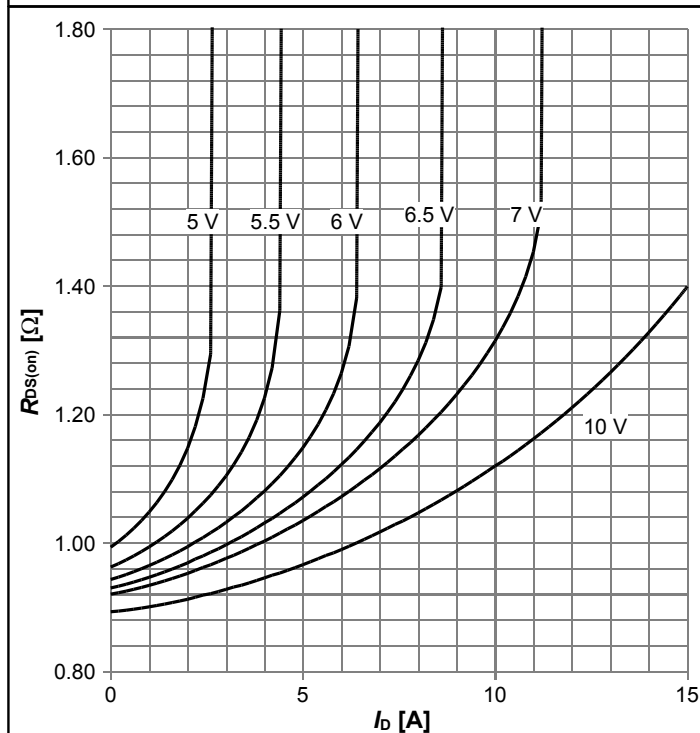
$I_D=f(V_{DS}); T_j=25^\circ\text{C}; \text{parameter: } V_{GS}$

Typ. output characteristics $T_j=125^\circ\text{C}$



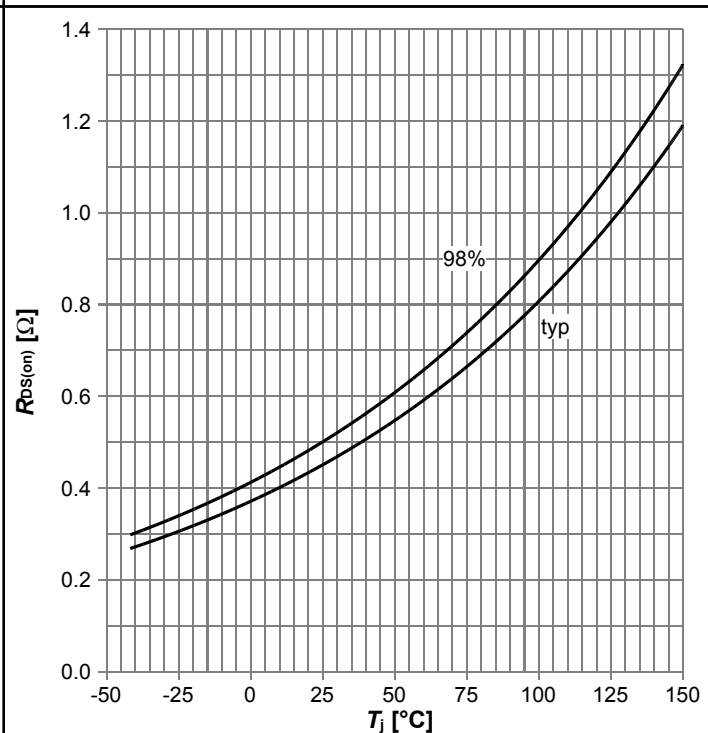
$I_D=f(V_{DS}); T_j=125^\circ\text{C}; \text{parameter: } V_{GS}$

Typ. drain-source on-state resistance

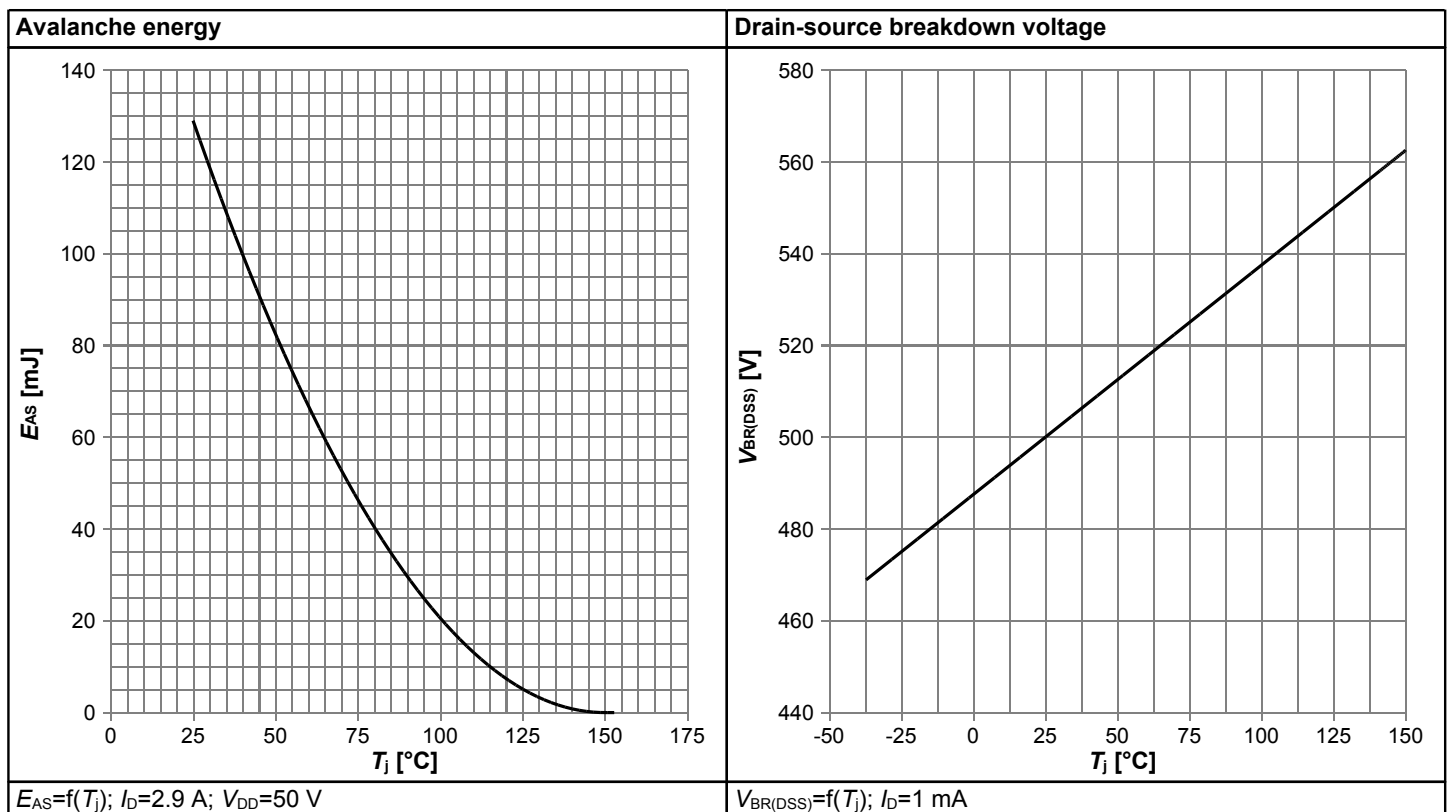
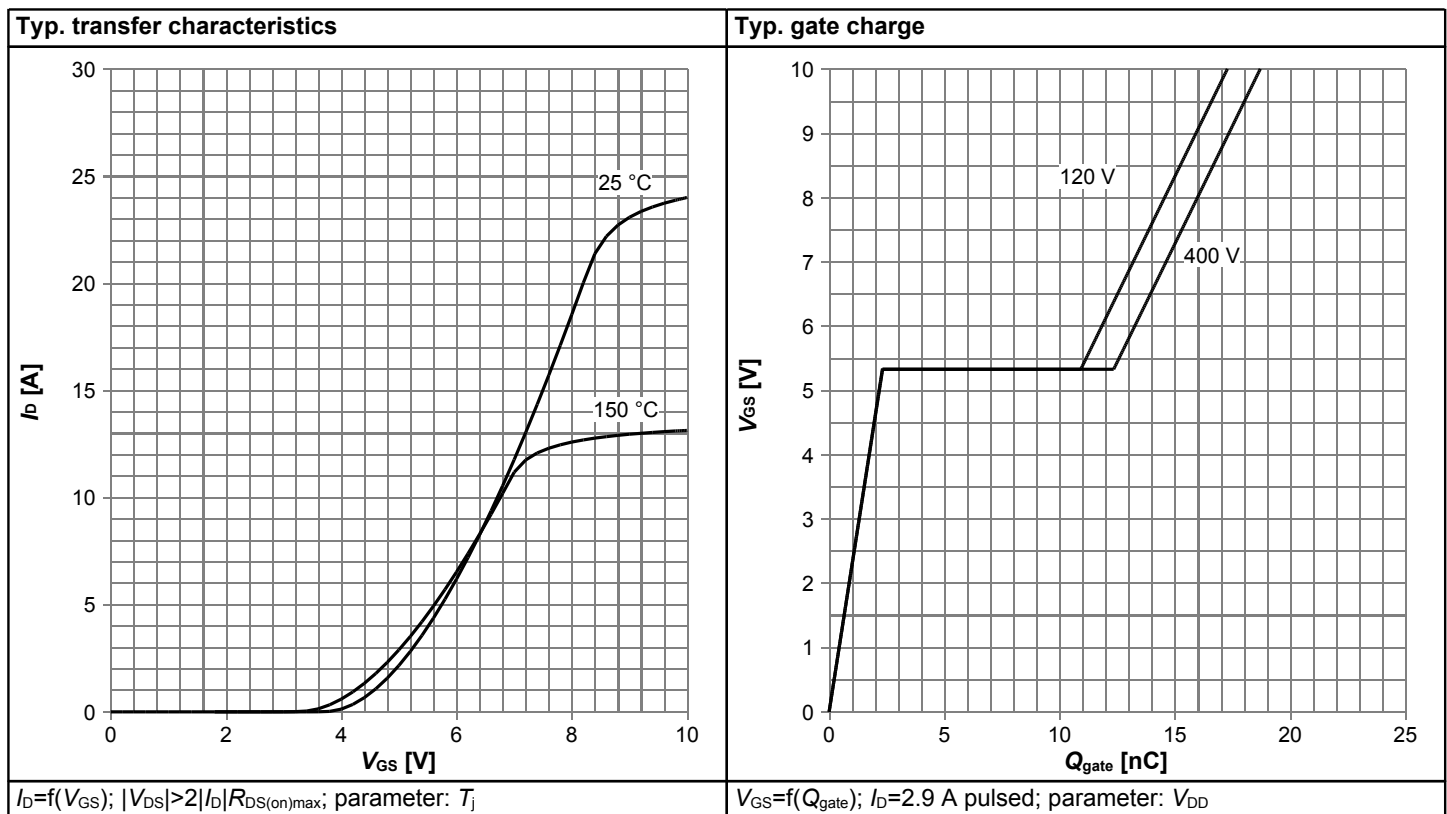


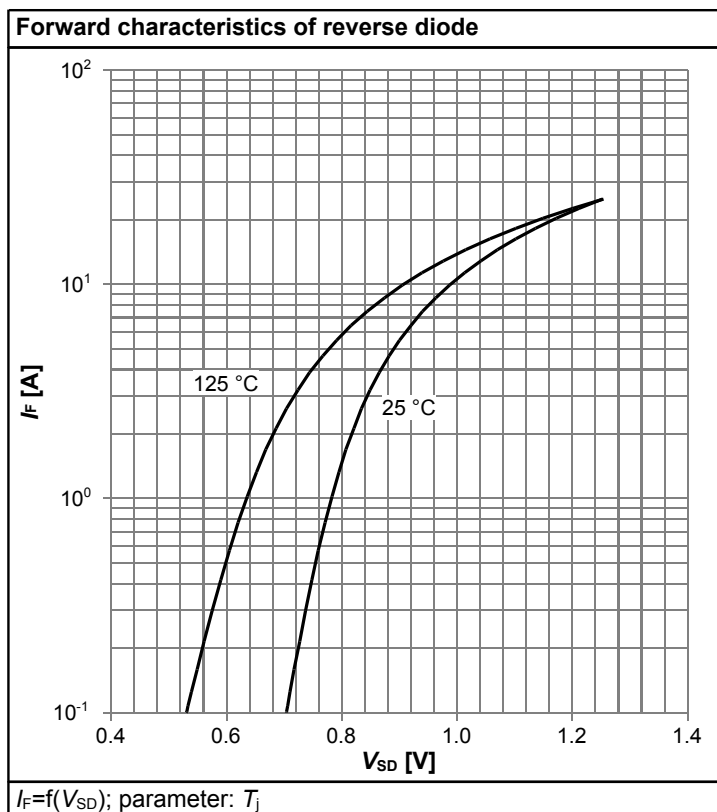
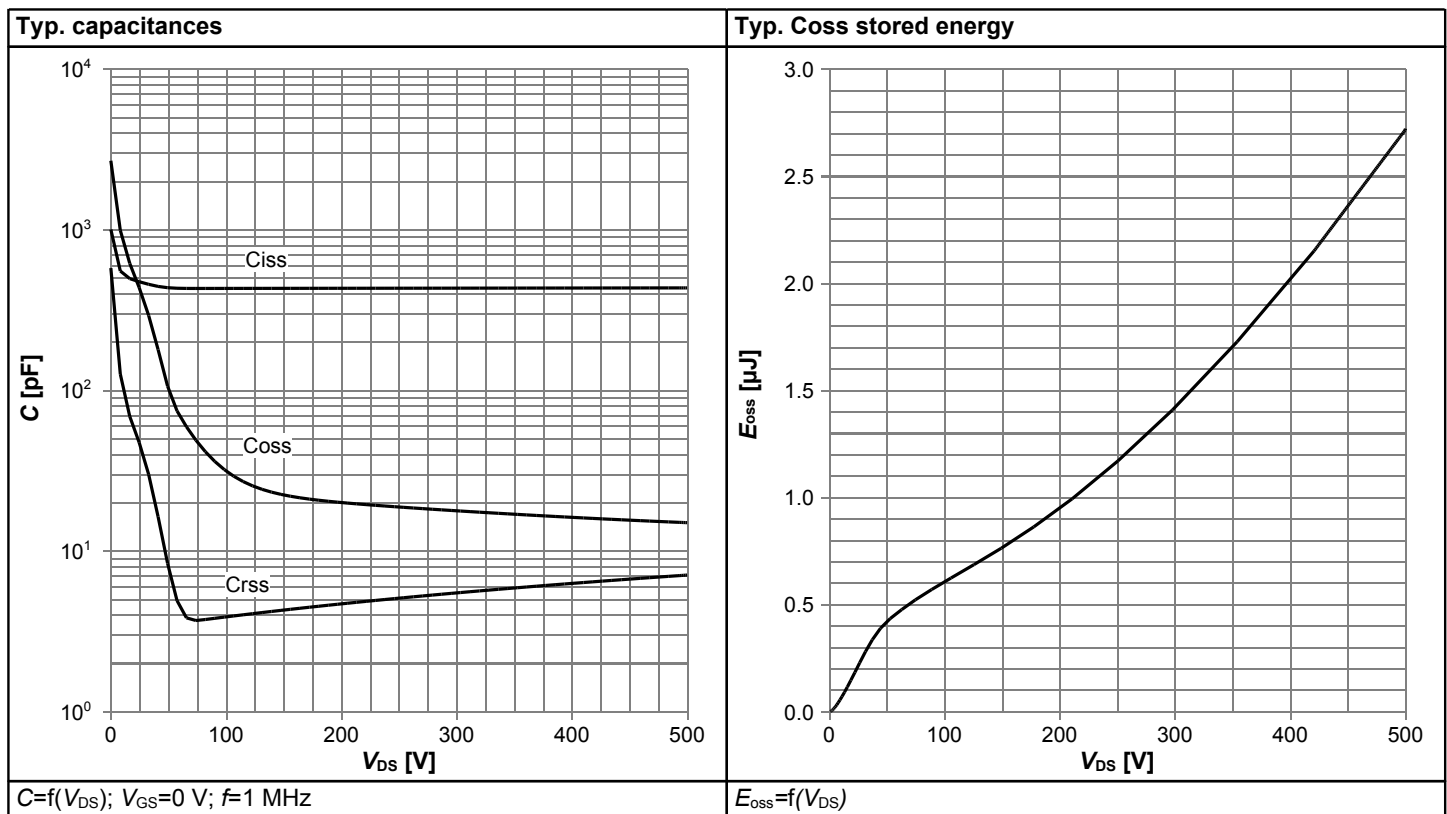
$R_{DS(on)}=f(I_D); T_j=125^\circ\text{C}; \text{parameter: } V_{GS}$

Drain-source on-state resistance



$R_{DS(on)}=f(T_j); I_D=2.3\text{ A}; V_{GS}=13\text{ V}$





5 Test Circuits

Table 8 Diode characteristics

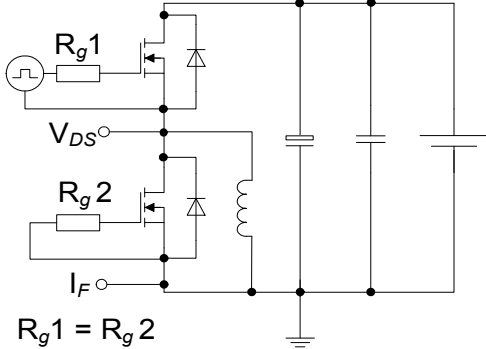
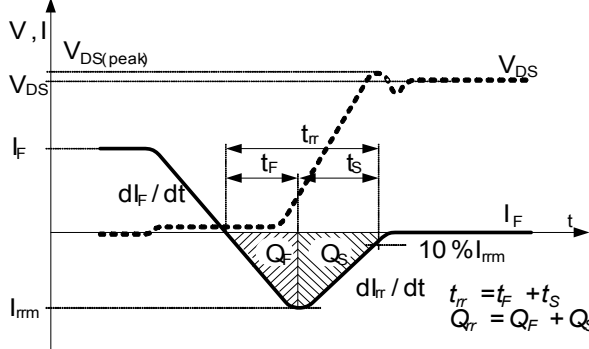
Test circuit for diode characteristics	Diode recovery waveform
 $R_{g1} = R_{g2}$	 $t_{rr} = t_F + t_S$ $Q_{rr} = Q_F + Q_S$

Table 9 Switching times

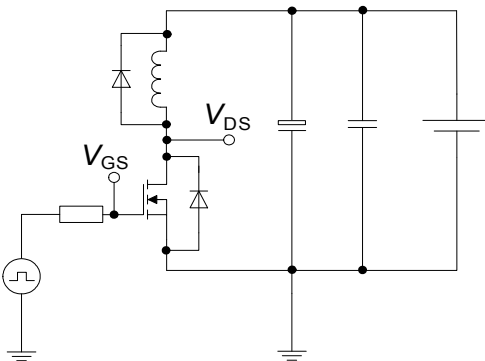
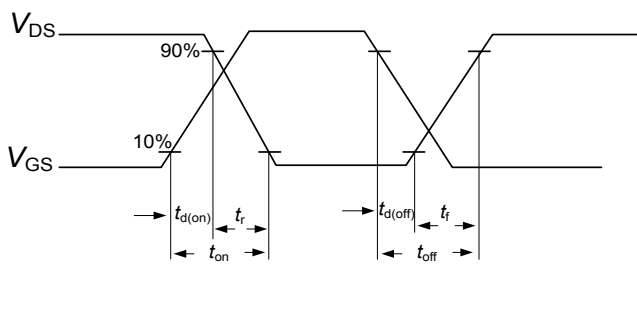
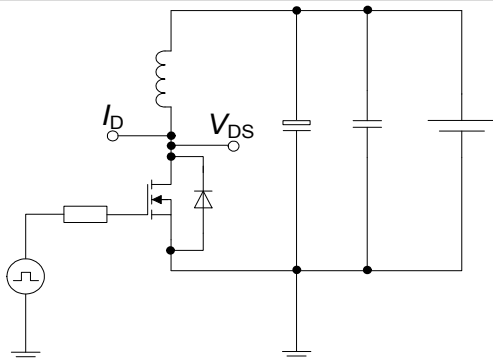
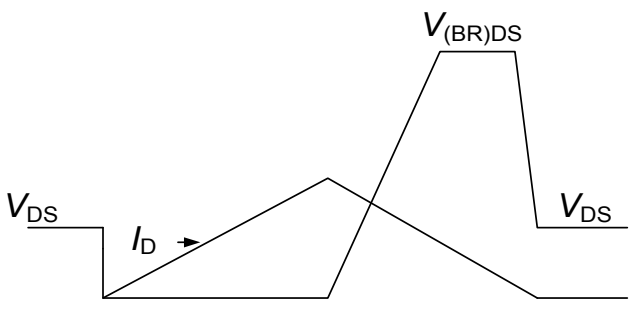
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines

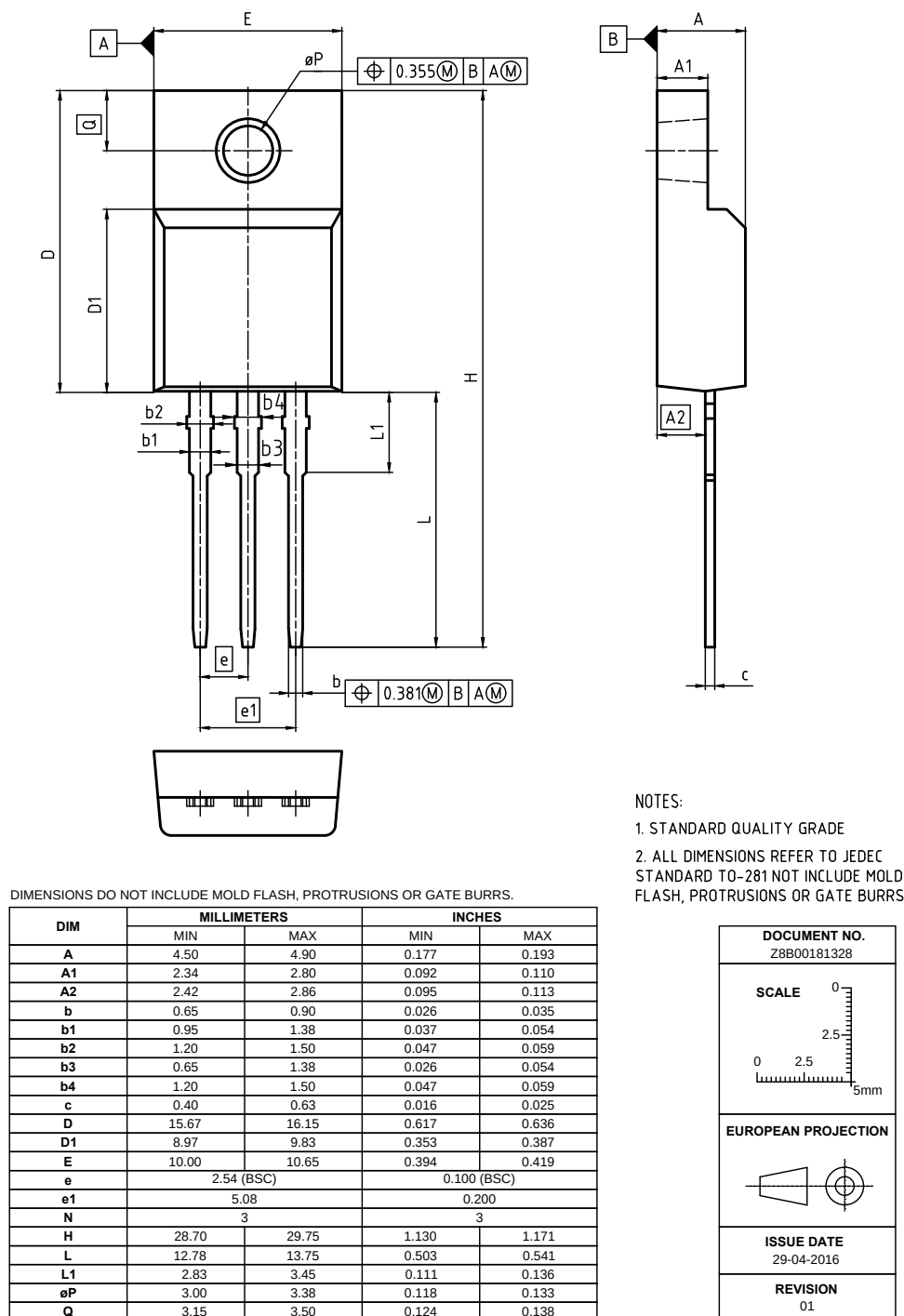


Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPA50R500CE

Revision: 2016-07-12, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-06-12	Release of final version
2.1	2016-06-13	Updated ID ratings, package marking code & package drawing
2.2	2016-07-12	Changed marking information in page 1

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