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REVISION HISTORY

8/2018—Rev. B to Rev. C

Changed Reflow Temperature (MSL1 Rating) to Reflow Temperature, Table 2 4
Deleted Note 1, Table 2; Renumbered Sequentially 4
Changes to Theory of Operation Section 8
Changes to Ordering Guide 11

11/2017—Rev. A to Rev. B

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Changed N/C to NIC ..... Throughout
Changes to Features, Applications, and General Description 1
Changes to Table 1 3
Changes to Table 2 4
Changes to Figure 2 and Table 3 5
Changes to Figure 10 through Figure 13 7
Added Theory of Operation Section 8
Added Applications Information Section 9
Changes to Table 5 9
Updated Outline Dimensions 11
Changes to Ordering Guide 11

SPECIFICATIONS

V_{DD} = 3 V or 5 V, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		4	GHz
INSERTION LOSS						
Between RFC and RF1 to RF4 (On)		100 MHz to 1 GHz		0.6	0.9	dB
		1 GHz to 2 GHz		0.7	1.0	dB
		2 GHz to 2.5 GHz		0.9	1.2	dB
		2.5 GHz to 4 GHz		1.2	1.5	dB
ISOLATION						
Between RFC and RF1 to RF4 (Off)		100 MHz to 1 GHz	40	45		dB
		1 GHz to 2 GHz	38	43		dB
		2 GHz to 2.5 GHz	35	41		dB
		2.5 GHz to 4 GHz	25	32		dB
RETURN LOSS						
RFC and RF1 to RF4 (On)		100 MHz to 2.5 GHz		18		dB
		2.5 GHz to 4 GHz		12		dB
RF1 to RF4 (Off)		100 MHz to 4 GHz		12		dB
SWITCHING		250 MHz to 4 GHz				
Rise and Fall Time	t_{RISE}, t_{FALL}	10 % to 90 % of RF output		30		ns
On and Off Time	t_{ON}, t_{OFF}	50 % V_{CTL} to 90 % of RF output		100		ns
INPUT LINEARITY[1]		250 MHz to 4 GHz				
1 dB Power Compression	P1dB	V_{DD} = 3 V		24		dBm
		V_{DD} = 5 V	23	29		dBm
Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing				
		V_{DD} = 3 V		50		dBm
		V_{DD} = 5 V		47		dBm
SUPPLY		V_{DD} pin				
Voltage	V_{DD}		3		5	V
Current	I_{DD}			2.5	5	mA
DIGITAL CONTROL INPUTS		CTRLA and CTRLB pins				
Voltage	V_{CTL}					
Low	V_{INL}	V_{DD} = 3 V	0		0.8	V
		V_{DD} = 5 V	0		0.8	V
High	V_{INH}	V_{DD} = 3 V	2		3	V
		V_{DD} = 5 V	2		5	V
Current						
Low	I_{INL}			0.2		µA
High	I_{INH}			40		µA

[1] Input linearity performance degrades at frequencies less than 250 MHz.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Positive Supply Voltage (V_{DD})	7 V
Digital Control Input Voltage	−0.5 V to V_{DD} +1 V
RF Input Power	
(f = 100 MHz to 4 GHz, T_{CASE} = 85°C)	
V_{DD} = 3 V	
Through Path	23.5 dBm
Terminated Path	20 dBm
Hot Switching	17.5 dBm
V_{DD} = 5 V	
Through Path	28.5 dBm
Terminated Path	25 dBm
Hot Switching	22.5 dBm
Junction Temperature, T_J	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Temperature	260°C
Junction to Case Thermal Resistance, θ_{JC}	
Through Path	144°C/W
Terminated Path	300°C/W
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

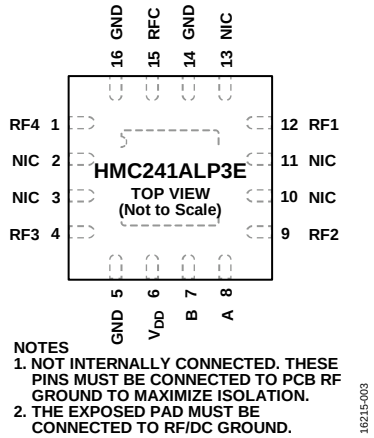

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RF4	RF Port 4. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
2, 3, 10, 11, 13	NIC	Not Internally Connected. These pins must be connected to the printed circuit board (PCB) RF ground to maximize isolation.
4	RF3	RF Port 3. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
5, 14, 16	GND	Ground. The package bottom has an exposed metal pad that must connect to the PCB RF/dc ground.
6	V_{DD}	Supply Voltage.
7	B	Logic Control Input B. See Figure 4 for the control input interface schematic. See Table 4 and the recommended input control voltages range in Table 1
8	A	Logic Control Input A. See Figure 4 for the control input interface schematic. See Table 4 and the recommended input control voltages range in Table 1
9	RF2	RF Port 2. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
12	RF1	RF Port 1. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
15	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

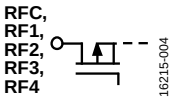

Figure 3. RFC to RF4 Interface Schematic

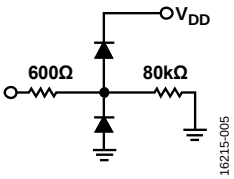

Figure 4. CTRLA and CTRLB Interface Schematic

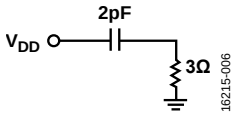

Figure 5. Supply Voltage Schematic

TYPICAL PERFORMANCE CHARCTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

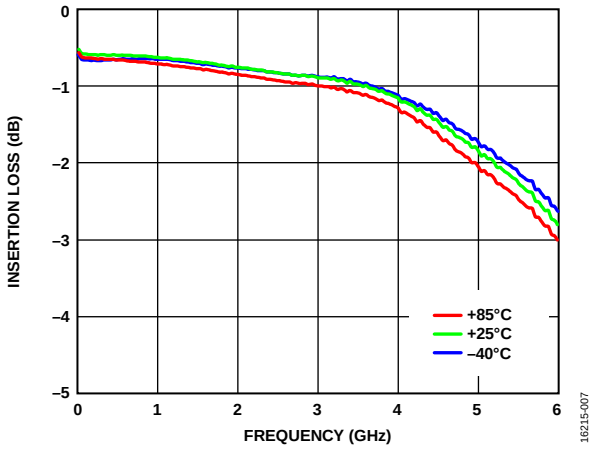

Figure 6. Insertion Loss Between RFC and RF1 vs. Frequency at Various Temperatures

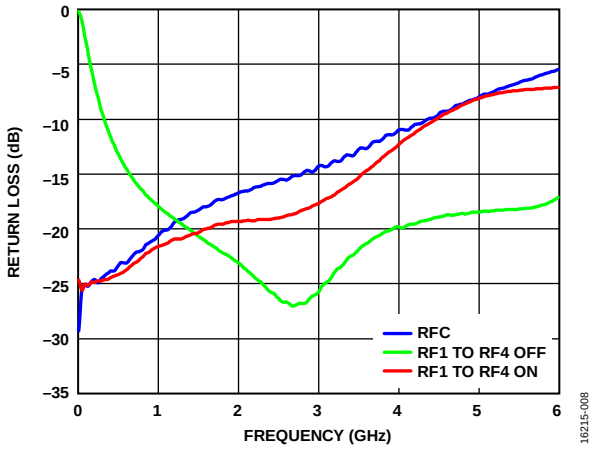

Figure 7. Return Loss for RFC, RF1 to RF4 On, and RF1 to RF4 Off vs. Frequency

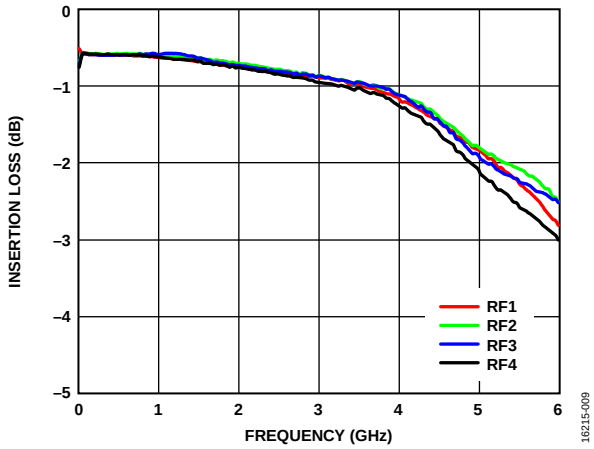

Figure 8. Insertion Loss Between RFC to RFx vs. Frequency

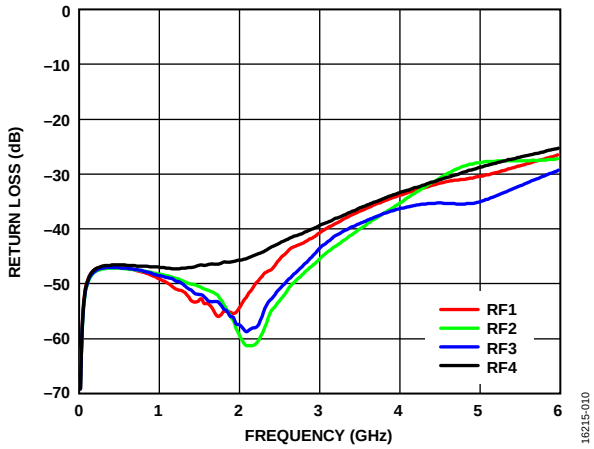

Figure 9. Isolation Between RFC and RFx vs. Frequency

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT (IP3)

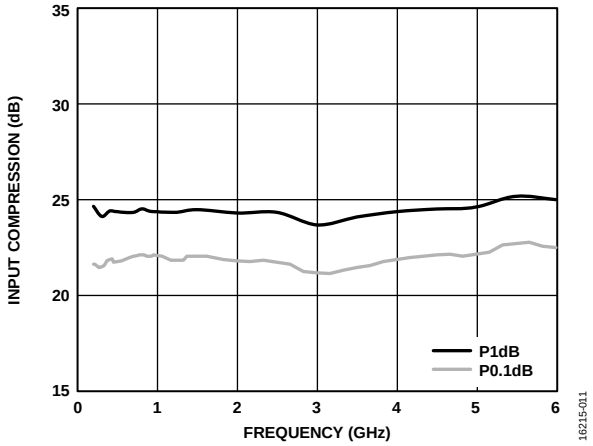

Figure 10. Input Compression vs. Frequency at Room Temperature, V_{DD} = 3 V

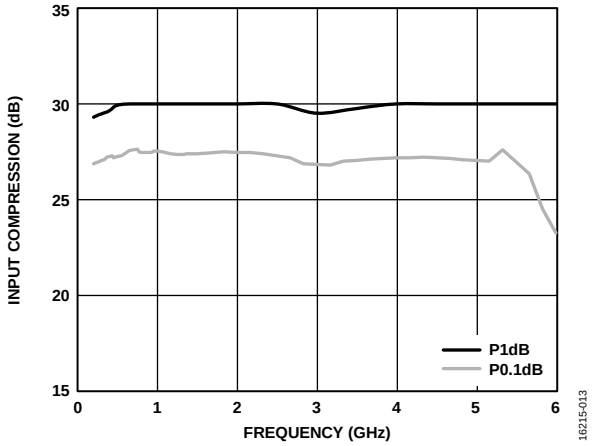

Figure 12. Input Compression vs. Frequency at Room Temperature, V_{DD} = 5 V

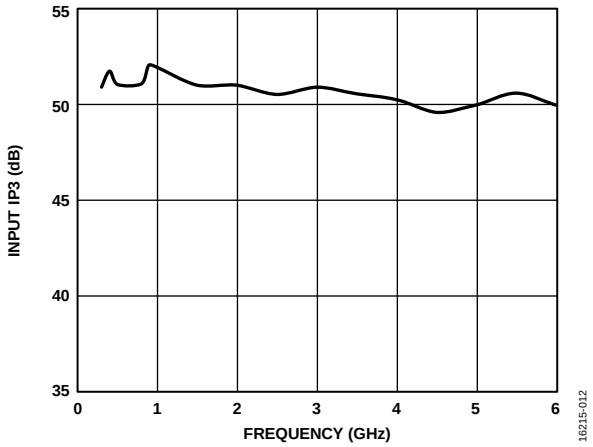

Figure 11. Input IP3 vs. Frequency at Room Temperature, V_{DD} = 3 V

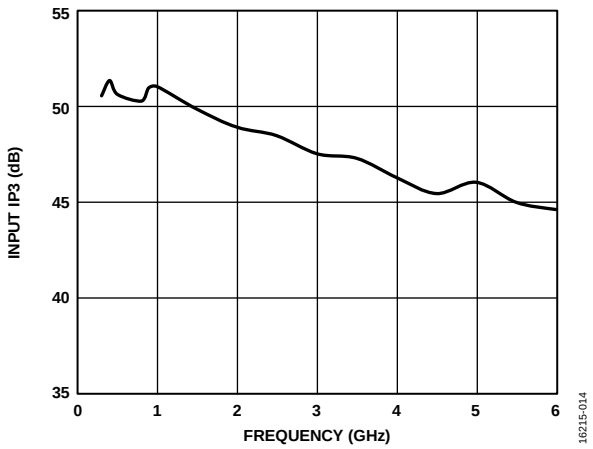

Figure 13. Input IP3 vs. Frequency at Room Temperature, V_{DD} = 5 V

THEORY OF OPERATIONS

The HMC241ALP3E requires a positive supply voltage at the V_{DD} pin and two logic control inputs at the A and B pins to control the state of the RF paths.

Depending on the logic level applied to the A and B pins, one RF path is in the insertion loss state while the other three paths are in an isolation state (See Table 4). The insertion loss path conducts the RF signal between the RF throw pad and RF common pad while the isolation paths provide high loss between RF throw pads terminated to internal 50 Ω resistors and the insertion loss path.

The ideal power-up sequence is as follows:

1. Power up GND.
2. Power up V_{DD}.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the V_{DD} supply can inadvertently become forward biased and damage the internal ESD protection structures.
4. Apply an RF input signal. The design is bidirectional; the RF input signal can be applied to the RFC pad while the RF throw pads are the outputs, or the RF input signal can be applied to the RF throw pads while the RFC pad is the output. All of the RF ports are dc-coupled to V_{DD} through internal resistors. Therefore, dc blocking the capacitors are required at the RF ports.

The power-down sequence is the reverse of the power-up sequence.

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths			
CTRLA	**CTRLB**	**RFC to RF1**	**RFC to RF2**	**RFC to RF3**	**RFC to RF4**
Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

EVALUATION BOARD

The 108333-HMC241ALP3 is a 4-layer evaluation board. Each copper layer is 0.7 mil (0.5 oz) and separated by dielectric materials. Figure 14 shows the stack up for this evaluation board.

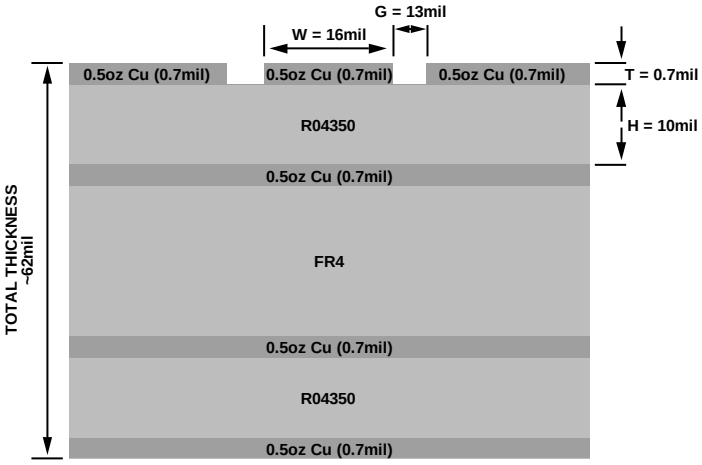

Figure 14. The 108333-HMC241ALP3 Evaluation Board (Cross Sectional View)

All RF and dc traces are routed on the top copper layer whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. Top dielectric material is a 10 mil Rogers RO4350. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, allowing the SMA launchers to be connected at the board edges.

The RF transmission lines were designed using a coplanar waveguide (CPWG) model, with trace width of 16 mil and ground clearance of 13 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Figure 15 shows the layout of the 108333-HMC241ALP3 evaluation board with component placement. The power supply port is connected to the V_{DD} test point, J6. The control voltages are connected to the A and B test points, J8 and J7. The ground reference is connected to the GND test point, J9. The NIC pins are connected to the PCB ground to maximize isolation. On the supply trace, V_{DD}, a 10 nF bypass capacitor, is used to filter high frequency noise.

The RF input and output ports (RFC, RF1, RF2, RF3, and RF4) are connected through 50 Ω transmission lines to the soldered down SMA launchers, J1 to J5. For dc blocking to the RF pins, C1 to C5 are populated with 100 pF capacitors. A thru calibration line connects the unpopulated J10 and J11 launchers; this transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

Table 5 and Figure 16 are the bill of materials and schematic, respectively.

Table 5. Evaluation Board Components

Component	Default Value	Description
J1 to J5	Not Applicable	PCB mount SMA connector
J6 to J9	Not Applicable	DC pin
J10, J11	Do not insert	PCB mount SMA connector
C1 to C5	100 pF	Capacitor, C0402 package
C6	10 nF	Capacitor, C0402 package
U1	Not Applicable	HMC241ALP3E SP4T switch
PCB	104708	Evaluation PCB

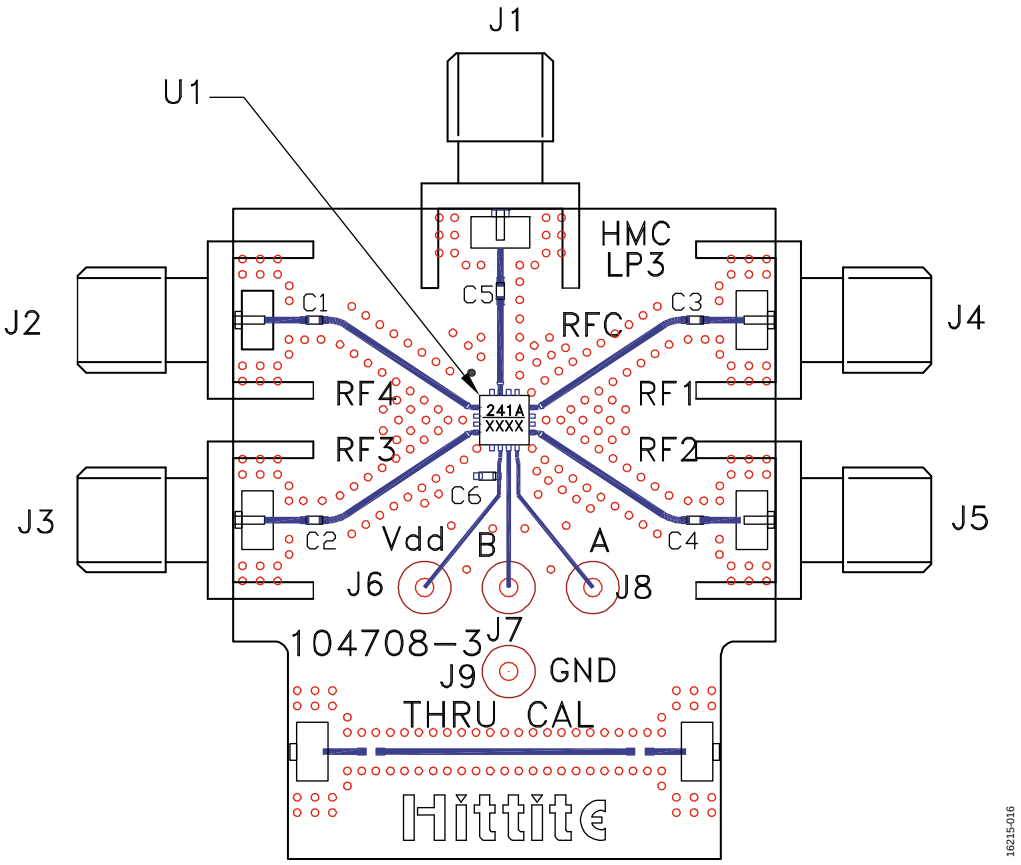

Figure 15. 108333-HMC241ALP3 Evaluation Board Component Placement

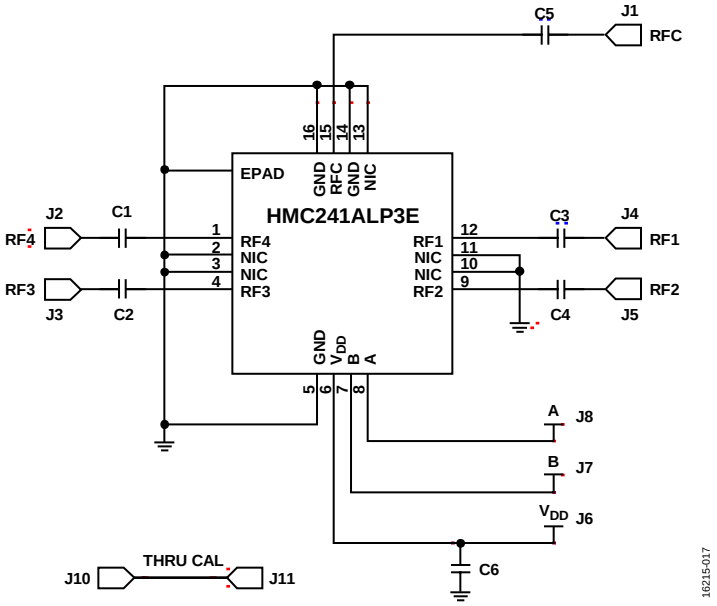

Figure 16. Evaluation Board Schematic

OUTLINE DIMENSIONS

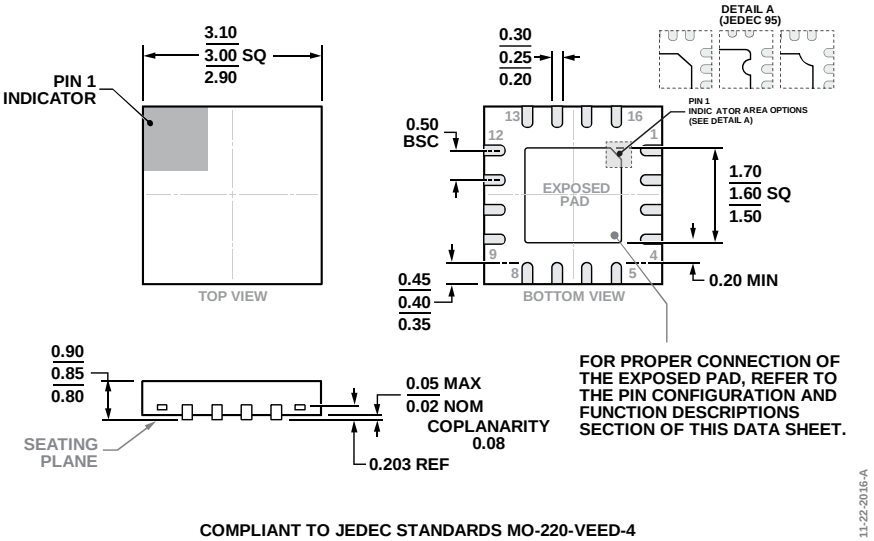

Figure 17. 16-Terminal Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.85 mm Package Height
(CP-16-50)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC241ALP3E	−40°C to +85°C	16-Terminal Lead Frame Chip Scale Package [LFCSP]	CP-16-50
HMC241ALP3ETR	−40°C to +85°C	16-Terminal Lead Frame Chip Scale Package [LFCSP]	CP-16-50
108333-HMC241ALP3		Evaluation Board	

[1] All models are RoHS compliant.

D16215-0-8/18(C)