WIDEBAND DIRECT QUADRATURE MODULATOR w/ Fractional-N PLL & VCO, 100 - 4000 MHz

Table 1. Electrical Specifications, See Test Conditions on page-4.

Parameter	Typ.	Typ.	Typ.	Typ.	Units
Frequency Range, RF	450-960	1700-2200	2200-2700	3400-4000	MHz
Output Power	-2.0	-1.1	-1.3	-3.2	dBm
Conversion Voltage Gain	-6.0	-5.1	-5.3	-7.2	dB
Output P1dB	+10.5	+10.5	+10	+9.5	dBm
Output Noise Floor	-159.5	-157.0	-156.5	-156.5	dBm/Hz
Output IP3	+28.5	+26.5	+26.0	+23.5	dBm
Carrier Feedthrough (uncalibrated)	-40	-37.0	-33.5	-34.5	dBm
Sideband Suppression (uncalibrated)	45	45	43	30.5	dBc
RF Port Return Loss	12.5	15	16	16	dB

Table 2. Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
RF Output					
RF Frequency Range		100		4000	MHz
RF Return Loss			15		dB
Baseband Input Port					
Baseband Input DC Voltage (Vbbdc)			+0.5 (+0.4 to +0.6)		V
Baseband Input DC Bias Current (Ibbdc)	Single-ended.		110		pA
Single-ended Baseband Input Capacitance	De-embed to the lead of the device.		4.5		pF
DC Power Supply					
Supply Voltage (VCC1, VCC2, VCC3, VDDLS, VDDCP, BIAS, IF1P)		+4.75	+5.0	+5.25	V
Supply Current of +5V Supply (I_{CC1})	Modulator ON and PLL ON		320		mA
	Modulator OFF and PLL ON		152		mA
	Modulator OFF and PLL OFF		12		mA
Supply Voltage (V3, DVDD, RVDD, VCCPD, VCCPS, VCCHF)		3.15	+3.3	3.45	V
Supply Current of +3.3V Supply (I_{CC2})	Modulator ON and PLL ON		48		mA
	Modulator OFF and PLL ON		48		mA
	Modulator OFF and PLL OFF		1		mA
Enable/Disable Interface					
EN High Level	Modulator disabled		5		V
EN Low Level	Modulator enabled		0		V
Enable/Disable Settling Time			400/400		ns
LO Leakage Isolation	EN_MOD=5V, LO=2.1GHz		-75		dBm
Logic Inputs					
Logic High		1.2			V
Logic Low				0.6	V
Input Current				+/- 1	uA
Input Capacitance			2		pF
LO Output Characteristics					
LO Output Frequency		50		4100	MHz
VCO Frequency at PLL Input		2000		4100	MHz

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Table 2. Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
VCO Fundamental Frequency		2000		4100	MHz
VCO Output Divider					
VCO Output Divider Range	1, 2, 4, ... 60, 62	1		62	
PLL RF Divider Characteristics					
19-Bit N Divider Range	Integer	16		524287	
	Fractional	20		524283	
Phase Detector (PD)					
PD Frequency	Fractional Mode	DC		100	MHz
	Integer Mode	DC		100	MHz
Harmonics					
fo Mode at 4000 MHz	2nd / 3rd / 4th		-30/-22/-32		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynamically max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled	1	2	3.3	Vpp
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	
VCO Open Loop Phase Noise at fo @ 4 GHz					
10 kHz Offset			-78		dBc/Hz
100 kHz Offset			-108		dBc/Hz
1 MHz Offset			-134.5		dBc/Hz
10 MHz Offset			-156		dBc/Hz
100 MHz Offset			-171		dBc/Hz
VCO Open Loop Phase Noise at fo @ 3 GHz/2 = 1.5 GHz					
10 kHz Offset			-83		dBc/Hz
100 kHz Offset			-113		dBc/Hz
1 MHz Offset			-139.5		dBc/Hz
10 MHz Offset			-165.5		dBc/Hz
100 MHz Offset			-167		dBc/Hz
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz

Table 2. Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
VCO Characteristics					
VCO Tuning Sensitivity at 3862 MHz	Measured at 2.5 V		15		MHz/V
VCO Tuning Sensitivity at 3643 MHz	Measured at 2.5 V		14.5		MHz/V
VCO Tuning Sensitivity at 3491 MHz	Measured at 2.5 V		16.2		MHz/V
VCO Tuning Sensitivity at 3044 MHz	Measured at 2.5 V		14.6		MHz/V
VCO Tuning Sensitivity at 2558 MHz	Measured at 2.5 V		15.4		
VCO Tuning Sensitivity at 2129 MHz	Measured at 2.5 V		14.8		
VCO Supply Pushing	Measured at 2.5 V		2		MHz/V

Table 3. Test Conditions: *Unless Otherwise Specified, the Following Test Conditions Were Used*

Parameter	Condition
Temperature	+25 °C
Baseband Input Frequency	200 kHz
Baseband Input DC Voltage (Vbbdc)	+0.5 V
Baseband Input AC Voltage (Peak to Peak Differential, I and Q)	1.0 V
Baseband Input AC Voltage for OIP3 Measurements (Peak to Peak Differential, I and Q)	500 mV per tone @ 150 & 250 KHz
Baseband Input AC Voltage for Noise Floor Measurements (Peak to Peak Differential, I and Q)	no baseband input voltage
Frequency Offset for Output Noise Measurements	20 MHz
Supply Voltage (VCC1, VCC2, VCC3, VDDLS, VDDCP, BIAS)	+5.0V
Supply Voltage (V3, DVDD, RVDD, VCCPD, VCCPS, VCCHF)	+3.3V
LO Power Level	Maximum Power
Mounting Configuration	Refer to HMC1197LP7FE Application Schematic Herein
Sideband & Carrier Feedthrough	Uncalibrated

Table 4. Filter Bank Selection vs. Frequency

Frequency (MHz)	≤ 500	600	700	800	900	1000/1100	1200	1300/1400/1500	1600	1700/1800	1900/2000	2000 ≥
Frequency (MHz)	≤ 500	600	700	800	900	1000/1100	1200	1300/1400/1500	1600	1700/1800	1900/2000	2000 ≥
Filter Bank Selection	0	1	5	7	8	0	7	8	9	10	11	15

Calibrated vs. Uncalibrated Test Results

During the Uncalibrated Sideband and Carrier Suppression tests, care is taken to ensure that the I/Q signal paths from the Vector Signal Generator (VSG) to the Device Under Test (DUT) are equal. The “Uncalibrated” Sideband and Carrier Suppression plots were measured at T= -40 °C, +25 °C, and +85 °C.

The “Calibrated” Sideband Suppression data was plotted after a manual adjustment of the I/Q amplitude balance and I/Q phase offset (skew) at +25 °C, 5V and 3.3V Vcc, LO maximum power level. The +25 °C adjustment settings were held constant during tests over temperature.

The “Calibrated” Carrier Suppression data was plotted after a manual adjustment of the IP/IN & QP/QN DC offsets at +25 °C, 5V and 3.3V Vcc, LO maximum power level. The +25 °C adjustment settings were held constant during tests over temperature.

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Figure 1. RF Output Power vs. Frequency Over Temperature

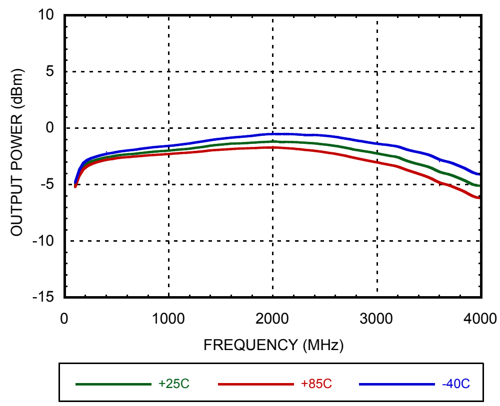


Figure 2. RF Output IP3, P1dB & Noise Floor @ 20 MHz Offset vs. Frequency Over Temperature

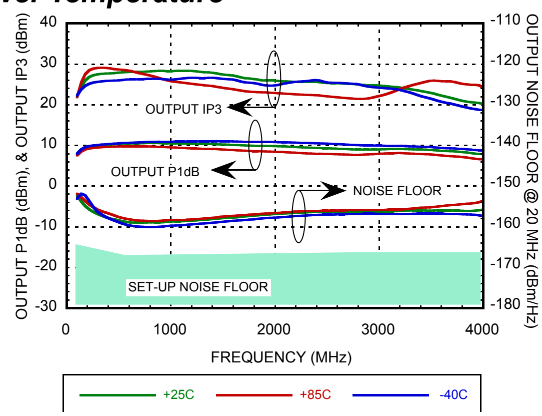


Figure 3. Uncalibrated Carrier Feedthrough vs. Frequency Over Temperature [1]

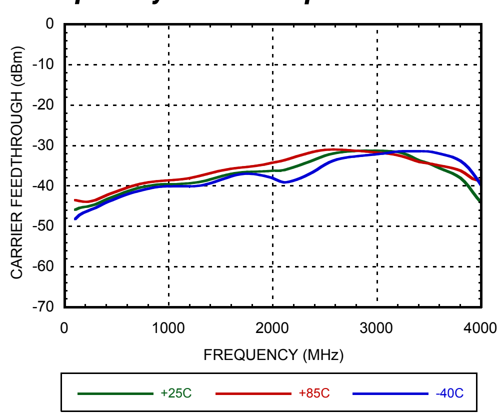


Figure 4. Calibrated Carrier Feedthrough vs. Frequency Over Temperature [1]

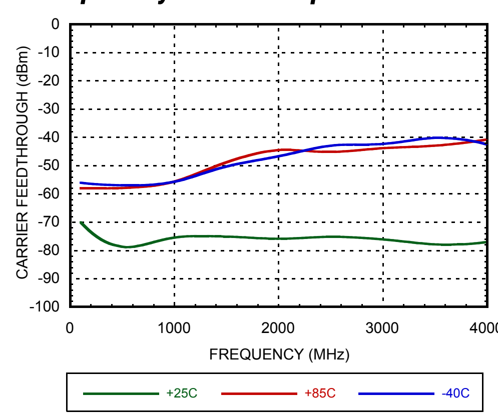


Figure 5. Uncalibrated Carrier Feedthrough vs. Frequency Over Temperature When Modulator is Disabled

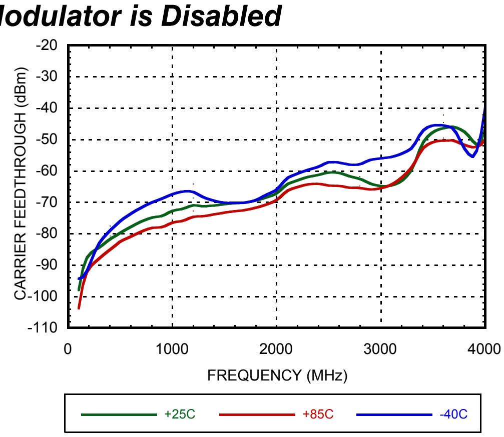
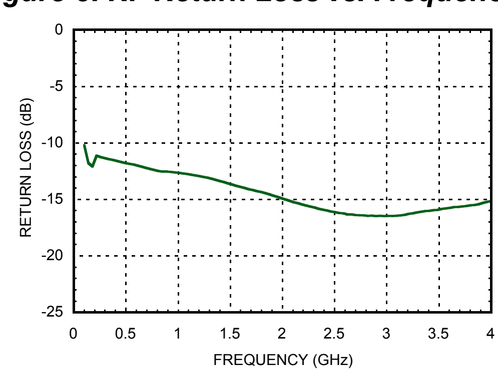


Figure 6. RF Return Loss vs. Frequency



[1] See note titled "Calibrated vs. Uncalibrated test results" herein.

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Figure 7. RF Output Power & SBR vs. Frequency Over LO Power

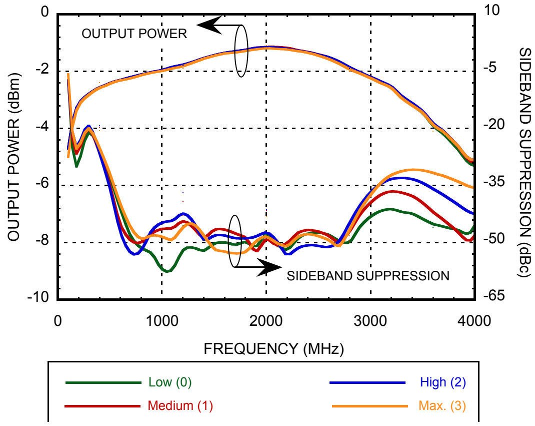


Figure 8. RF Output IP3, P1dB & Noise Floor @ 20 MHz Offset vs. Frequency Over LO Power

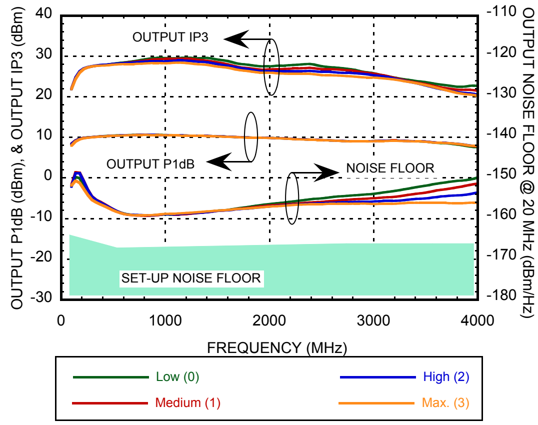


Figure 9. Uncalibrated Sideband Suppression vs. Frequency Over Temperature [1]

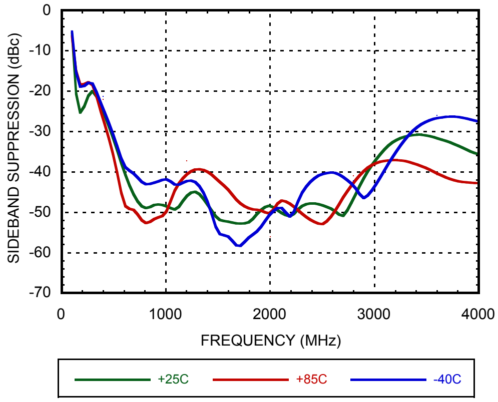


Figure 10. Calibrated Sideband Suppression vs. Frequency Over Temperature [1]

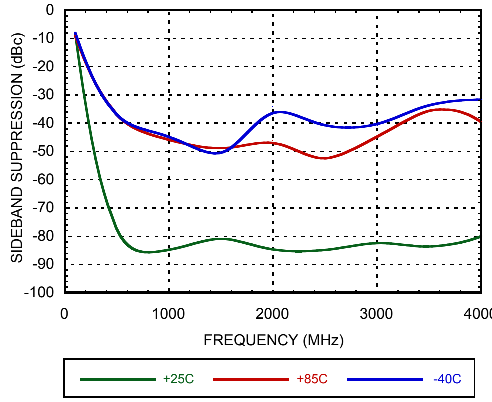


Figure 11. RF Output Power & SBR vs. Frequency Over Supply Voltage

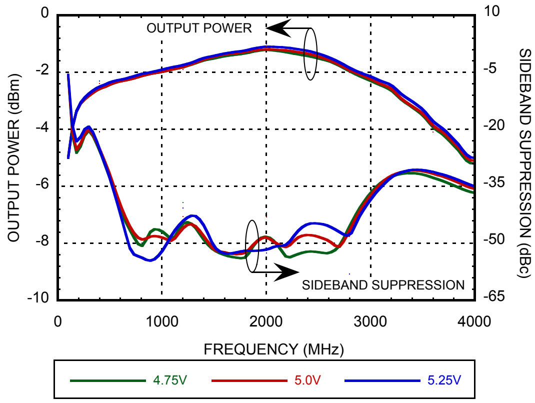
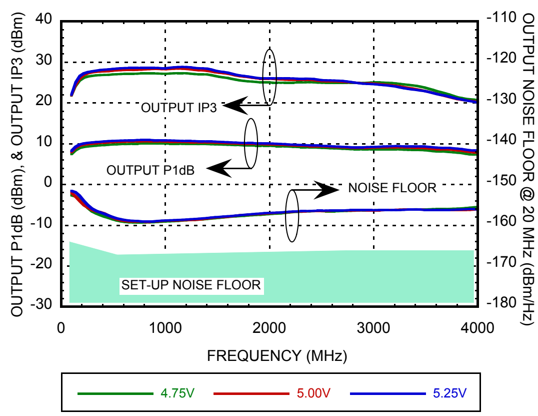


Figure 12. RF Output IP3, P1dB & NoiseFloor @ 20 MHz Offset vs. Frequency Over Supply Voltage



[1] See note titled “Calibrated vs. Uncalibrated test results” herein.

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Figure 13. RF Output Power vs. Baseband Voltage @ 2100 MHz

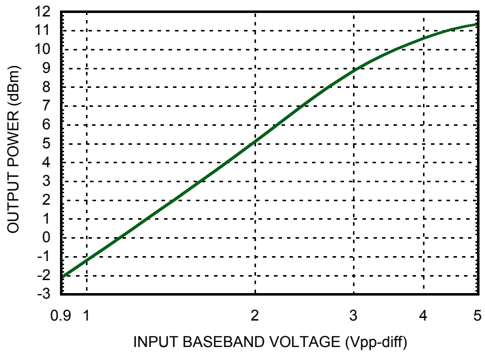


Figure 14. RF Output Noise @ 20 MHz Offset vs. Output Power Over LO Frequency

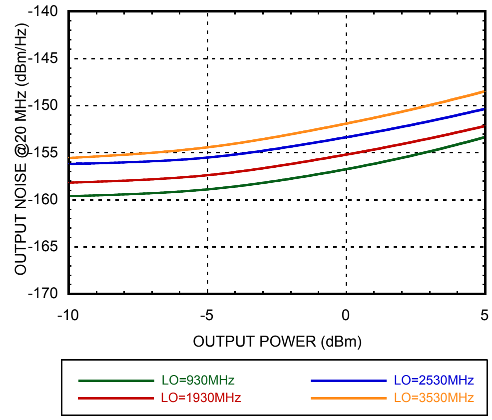
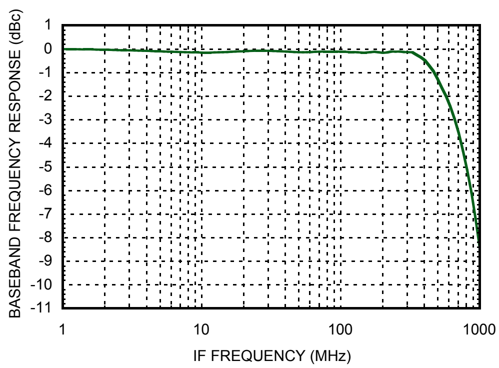


Figure 15. Normalized Baseband Frequency Response [1]



[1] I/Q input bandwidth normalized to gain at 1 MHz (fLO=1800 MHz). I/Q inputs are matched to 100 Ohms differentially.

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Figure 16. Auxiliary LO Output, Open Loop Phase Noise @ 3600 MHz

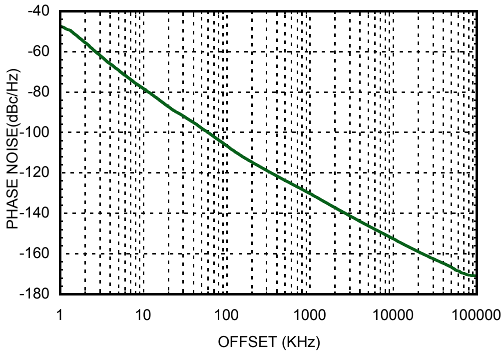


Figure 17. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @3600 MHz with various divider ratios [1]

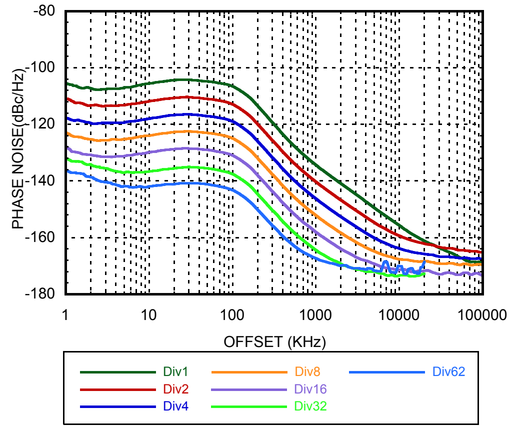


Figure 18. Auxiliary LO Output, Open Loop Phase Noise @ 4100 MHz

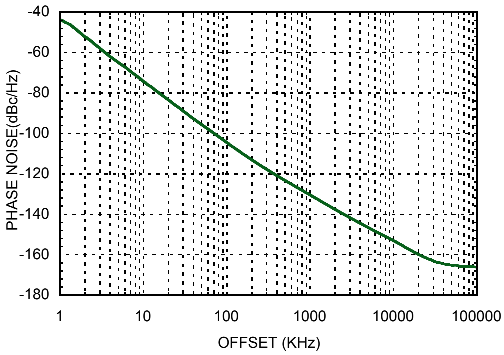


Figure 19. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @4100 MHz with various divider ratios [1]

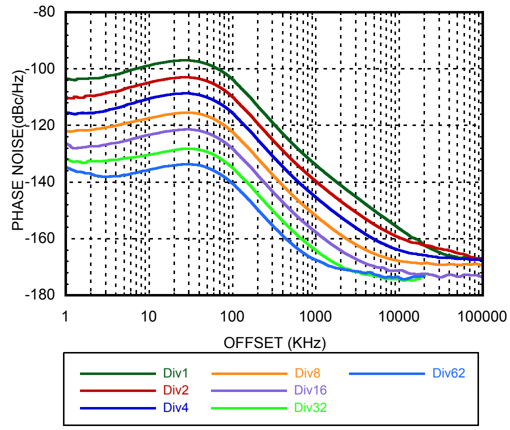
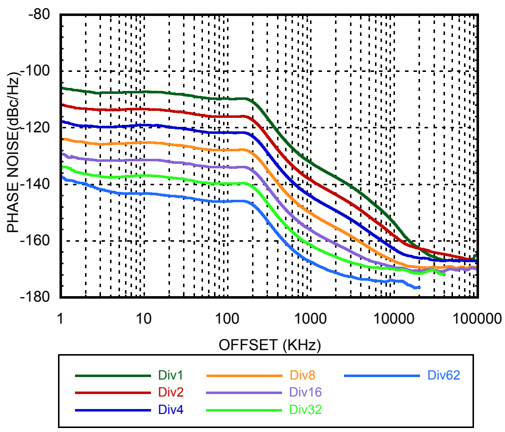


Figure 20. Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @ 3300 MHz with various divider ratios [2]



[1] Using 122.88 MHz clock input, 61.44 MHz PFD, 2.5 mA CP, 174 uA Leakage

[2] Using 100 MHz clock input, 50MHz PFD, 2.5 mA CP, 174 uA Leakage

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Figure 21. Auxiliary LO Output, Open Loop Phase Noise vs. Frequency

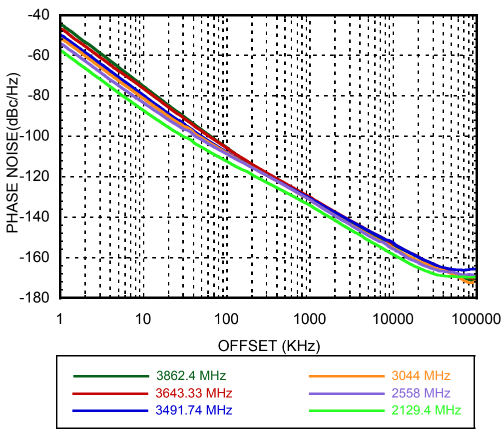


Figure 22. Auxiliary LO Output, Open Loop Phase Noise vs. Temperature

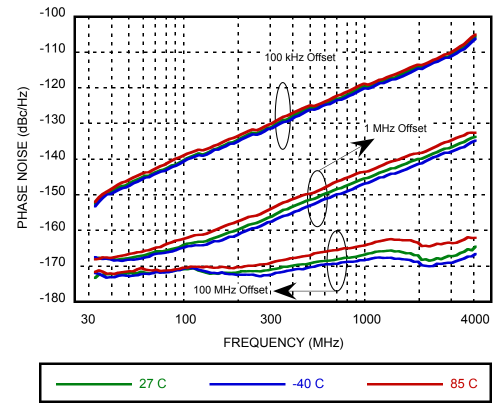


Figure 23. Auxiliary LO Output Power vs Temperature [1]

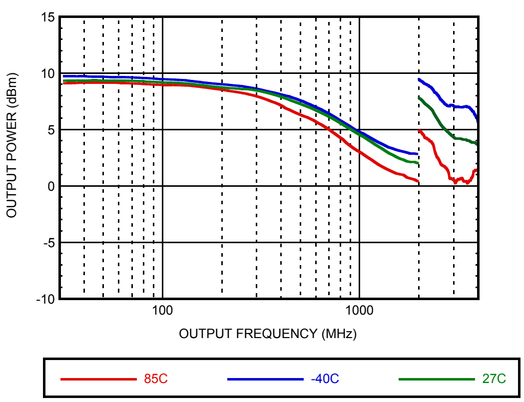


Figure 24. Integrated RMS Jitter [2]

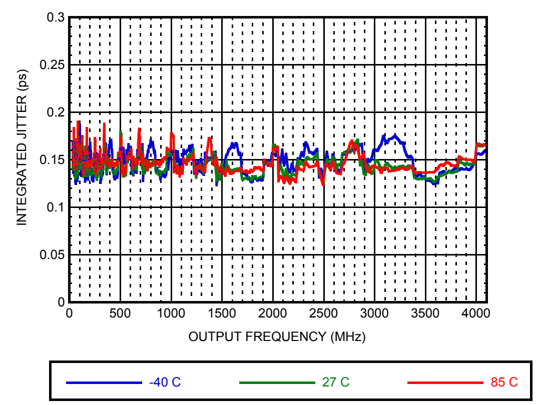


Figure 25. Typical VCO Sensitivity

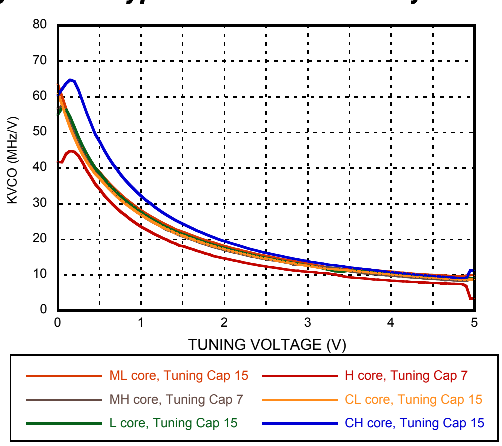
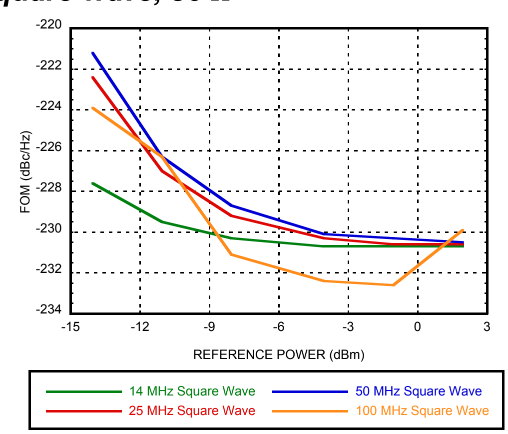


Figure 26. Reference Input Sensitivity, Square Wave, 50 Ω [3]



[1] Both Aux. LO and MOD LO Gain Set to '3' (Max Level), both Aux. LO and MOD LO Buffer Enabled, measured from Auxiliary LO Port.
[2] RMS Jitter data is measured in fractional mode using 50 MHz reference frequency, from 1 kHz to 100 MHz integration bandwidth.
[3] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

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Figure 27. Reference Input Sensitivity, Sinusoid Wave, 50 Ω [1]

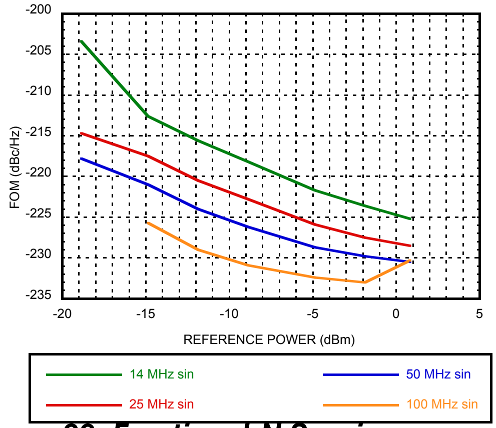


Figure 28. Figure of Merit for PLL/VCO

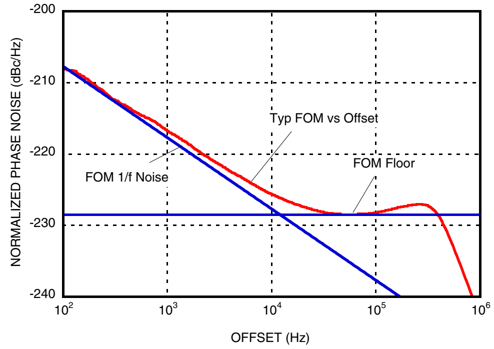


Figure 29. Fractional-N Spurious Performance @ 2646.96 MHz Exact Frequency Mode ON [2]

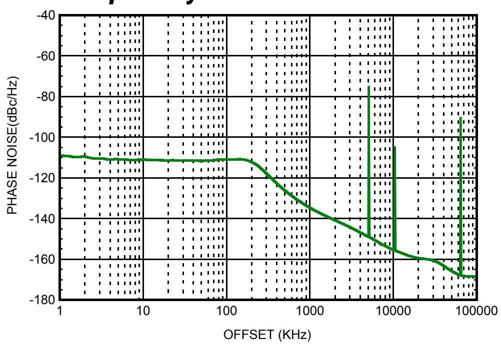


Figure 30. Fractional-N Spurious Performance @ 2646.96 MHz Exact Frequency Mode OFF [2]

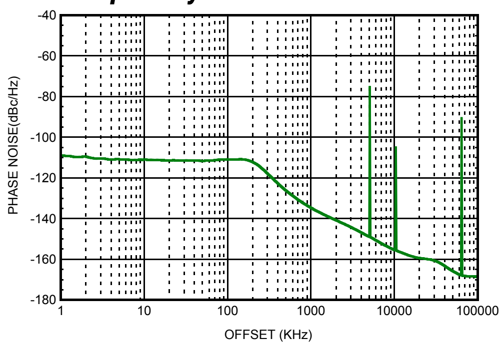


Figure 31. Forward Transmission Gain [3]

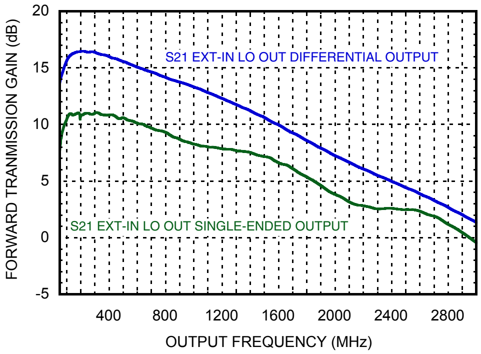
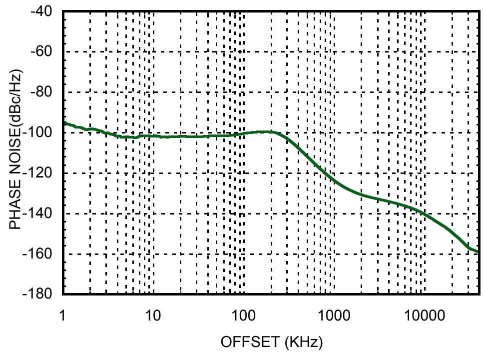


Figure 32. Closed Loop Phase Noise With External VCO HMC384LP4E @ 2200 MHz



[1] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.
[2] 122.88 MHz clock input, PFD = 61.44 MHz, Channel Spacing = 240 KHz.
[3] S21 from Ext_VCO (pin 43, 44) in and LO (pin32, 33) out.

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Figure 33. Auxiliary LO Differential Output Return Loss

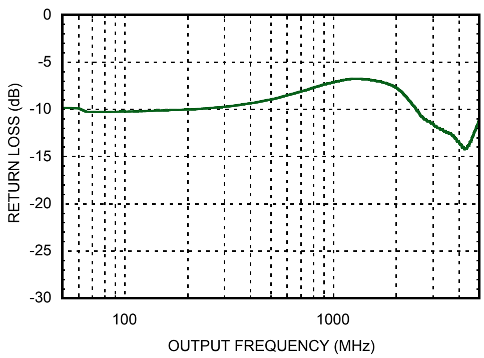


Figure 34. Auxiliary LO Single Ended Output Return Loss

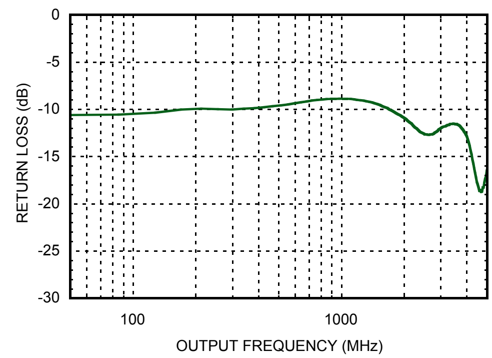


Table 5. Loop Filter Configuration

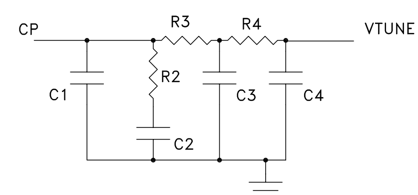
Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
156	180	6.8	47	47	2.2	1	1	

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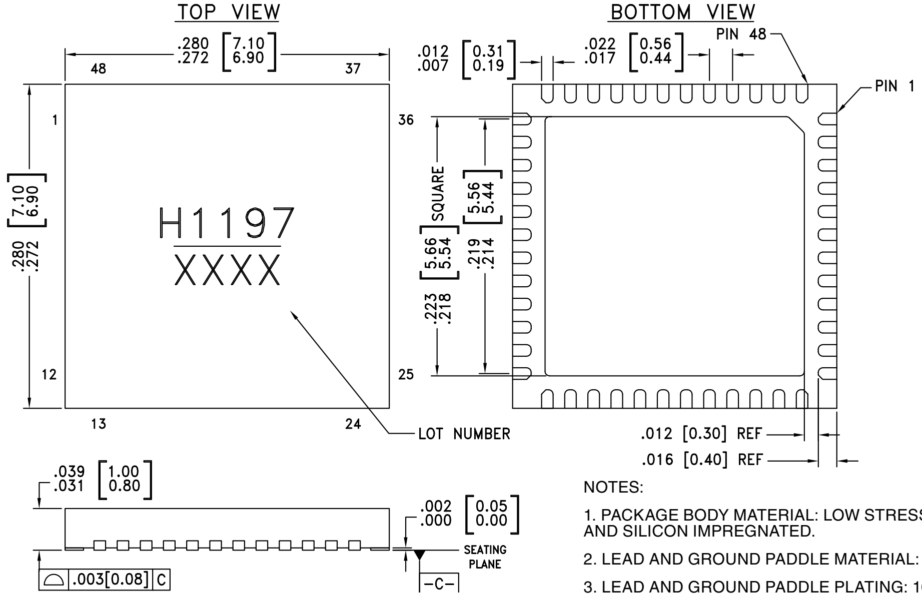
Table 6. Absolute Maximum Ratings

VCC1, VCC2, VCC3, VDDLS, VDDCP, BIAS, IF1P, EN_MOD	-0.3V to +5.5V
V3, DVDD, RVDD, VCCPD, VCCPS, VCCHF	-0.3V to +3.6V
Baseband Input Voltage (AC + DC) (Reference to GND)	-0.3V to + 1.3V
Junction Temperature	150°C
Thermal Resistance (R_{th}) (junction to ground paddle)	4.5 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 7. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC1197LP7FE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H1197 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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Table 8. Pin Descriptions

Pin Number	Function	Description
1	VDDCP	Power Supply for charge pump analog section, 5.0V nominal.
2	BIAS	External bypass decoupling for precision bias circuits, 5.0V nominal.
3,4	CP1,CP2	Charge Pump Outputs.
5	RVDD	Reference Supply, 3.3V nominal.
6	XREFP	Reference Input. DC bias is generated internally. Normally AC coupled externally.
7	DVDD	DC Power Supply for Digital (CMOS) Circuitry, 3.3V nominal.
8, 13, 14, 22, 23, 24, 28, 29, 30, 41, 42	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
9	EN_MOD	This pin has a 10 Kohm pulldown resistor to GND. When connected to GND or left floating the chip is fully enabled. When connected to VCC the LO amplifiers and the mixers are disabled.
10	IF1P	Supply voltage for the LO and mixer stage, 5.0V nominal.
11, 12	QN, QP	Q channel differential baseband input.These are high impedance ports. The nominal recommended bias voltage is 0.45V (0.4V-0.5V)[1].The nominal recommended baseband input AC voltage is 1.3V peak-to-peak differential.By adjusting the DC offsets on ports QN & QP , the Carrier Suppression of the device can be optimized for a specific frequency band and LO power level. The typical offset voltege for optimization is less than 15 mV. The amplitude and phase difference between The I and Q inputs can be adjusted in order to optimize the Sideband Suppression for a specific frequency band and LO power level
15, 16, 17, 18, 20	GND	These pins and package base must be connected to RF and DC ground.
19	RFOUT	DC coupled and matched to 50 Ohms. Output requires an external DC blocking capacitor.
21	VCC3	Supply voltage for the output stages, 5.0V nominal.
25, 26	IP, IN	I channel differential baseband input. These are high impedance ports. The nominal recommended bias voltage is 0.45V (0.4V-0.5V). The nominal recommended baseband input AC voltage is 1.3V peak-to-peak differential.By adjusting the DC offsets on ports IN & IP , the Carrier Suppression of the device can be optimized for a specific frequency band and LO power level. The typical offset voltege for optimization is less than 15 mV. The amplitude and phase difference between The I and Q inputs can be adjusted in order to optimize the Sideband Suppression for a specific frequency band and LO power level
27	V3	Supply pin for low pass filter, 3.3V nominal.
31	CHIP_EN	Chip Enable. Connect to logic high for normal operation.
32, 33	LON, LOP	LO outputs. AC coupled and matched to 50 Ohms single ended. Do not need external DC decoupling capacitors. The ports could be single-ended or differential.
34	VCC1	VCO analog supply 1, 5.0V nominal.
35	VCC2	VCO analog supply 2, 5.0V nominal.
36	VTUNE	VCO Varactor. Tuning Port Input.
37	SEN	PLL Serial Port Enable (CMOS) Logic Input.
38	SDI	PLL Serial Port Data (CMOS) Logic Input.
39	SCK	PLL Serial Port Clock (CMOS) Logic Input.

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Pin Descriptions

Pin Number	Function	Description
40	LD/SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO).
43	EXT_N	External VCO negative input.
44	EXT_P	External VCO positive input.
45	VCCHF	Analog supply, 3.3V nominal.
46	VCCPS	Analog supply, Prescaler, 3.3V nominal.
47	VCCPD	Analog supply, Phase Detector, 3.3 V nominal.
48	VDDLS	Analog supply, Charge Pump, 5.0 V nominal.

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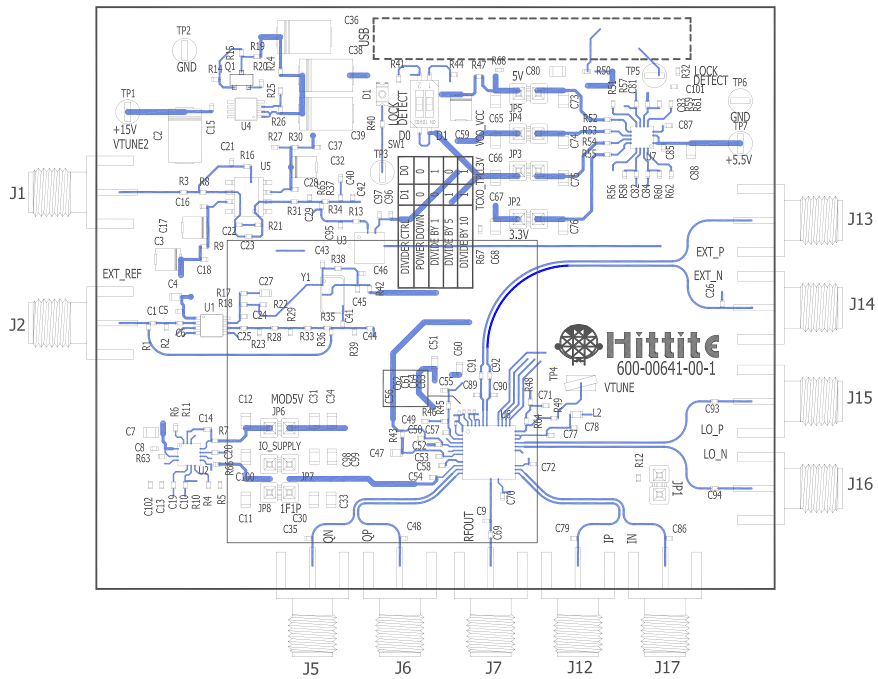
WIDEBAND DIRECT QUADRATURE MODULATOR w/ Fractional-N PLL & VCO, 100 - 4000 MHz

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC1197LP7FE from the "Search by Part Number" pull down menu to view the product splash page.

Table 9. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1197LP7FE Evaluation PCB	EVAL01-HMC1197LP7F
Evaluation Kit	HMC1197LP7FE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC1197LP7F

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1.0 Theory of Operation

The block diagram of HMC1197LP7FE PLL with Integrated VCO is shown in Figure 35

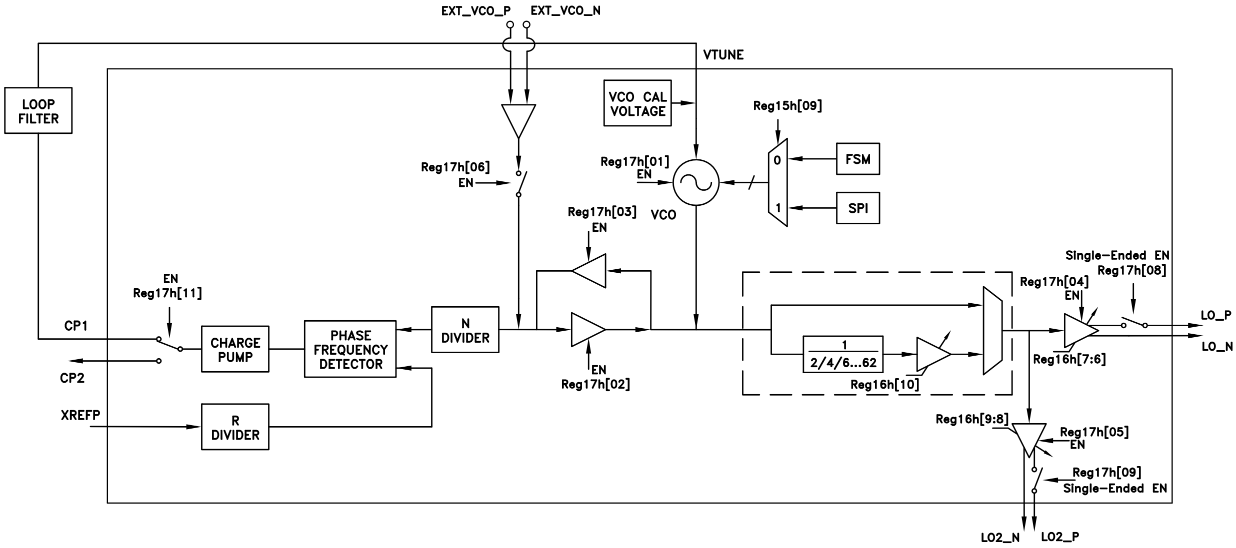

Figure 35. HMC1197LP7FE PLL VCO Block Diagram

1.1 PLL Overview

The PLL divides down the VCO output to the desired comparison frequency via the N-divider (integer value set in Reg 03h, fractional value set in Reg 04h), compares the divided VCO signal to the divided reference signal (reference divider set in Reg 02h) in the Phase Detector (PD), and drives the VCO tuning voltage via the Charge Pump (CP) (configured in Reg 09h) to the VCO subsystem. Some of the additional PLL subsystem functions include:

- Delta Sigma configuration (Reg 06h)
- Exact Frequency Mode (Configured in Reg 0Ch, Reg 06h,Reg 03h, and Reg 04h)
- Lock Detect (LD) Configuration (Reg 07h to configure LD, and Reg 0Fh to configure LD_SDO output pin)
- External CEN pin used as hardware enable pin.

Typically, only writes to the divider registers (integer part Reg 03h, fractional part Reg 04h,VCO Divide Ratio part Reg 04h) are required for HMC1197LP7FE output frequency changes.

Divider registers of the PLL (Reg 03h, and Reg 04h), set the fundamental frequency (2050 MHz to 4100 MHz) of the VCO. Output frequencies ranging from 33 MHz to 2050 MHz are generated by tuning to the appropriate fundamental VCO frequency (2050 MHz to 4100 MHz) by programming N divider (Reg 03h, and Reg 04h), and programming the output divider (divide by 1/2/4/6.../60/62, programmed in Reg 16h) in the VCO register.

For detailed frequency tuning information and example, please see "1.3.7 Frequency Tuning" section.

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1.2 VCO Overview

The VCO consists of a capacitor switched step tuned VCO and an output stage. In typical operation, the VCO is programmed with the appropriate capacitor switch setting which is executed automatically by the PLL AutoCal state machine if AutoCal is enabled (Reg 0Ah[11] = 0, see section "1.2.1 VCO Calibration" for more information). The VCO tunes to the fundamental frequency (2050 MHz to 4100 MHz), and is locked by the CP output from the PLL subsystem. The VCO controls the output stage of the HMC1197LP7FE enabling configuration of:

- VCO Output divider settings configured in Reg 16h (divide by 2/4/6...60/62 to generate frequencies from 33 MHz to 2050 MHz, or divide by 1 to generate fundamental frequencies between 2050 MHz and 4100 MHz)
- Output gain settings (Reg 16h[7:6], Reg 16h[9:8])
- Single-ended or differential output operation (Reg 17h[9:8])
- Always Mute (Reg 16h[5:0])
- Mute when unlock (Reg 17h[7])

1.2.1 VCO Calibration

1.2.1.1 VCO Auto-Calibration (AutoCal)

The HMC1197LP7FE uses a step tuned type VCO. A step tuned VCO is a VCO with a digitally selectable capacitor bank allowing the nominal center frequency of the VCO to be adjusted or 'stepped' by switching in/out VCO tank capacitors. A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the mid-voltage tuning point of the HMC1197LP7FE's charge pump. This enables the PLL charge pump to tune the VCO over the full range of operation with both a low tuning voltage and a low tuning sensitivity (kvco).

The VCO switches are normally controlled automatically by the HMC1197LP7FE using the Auto-Calibration feature. The Auto-Calibration feature is implemented in the internal state machine. It manages the selection of the VCO sub-band (capacitor selection) when a new frequency is programmed. The VCO switches may also be controlled directly via register Reg 15h for testing or for other special purpose operation.

To use a step tuned VCO in a closed loop, the VCO must be calibrated such that the HMC1197LP7FE knows which switch position on the VCO is optimum for the desired output frequency. The HMC1197LP7FE supports Auto-Calibration (AutoCal) of the step tuned VCO. The AutoCal fixes the VCO tuning voltage at the optimum mid-point of the charge pump output, then measures the free running VCO frequency while searching for the setting which results in the free running output frequency that is closest to the desired phase locked frequency. This procedure results in a phase locked oscillator that locks over a narrow voltage range on the varactor. A typical tuning curve for a step tuned VCO is shown in Figure 36.Note how the tuning voltage stays in a narrow range over a wide range of output frequencies such as fast frequency hopping.

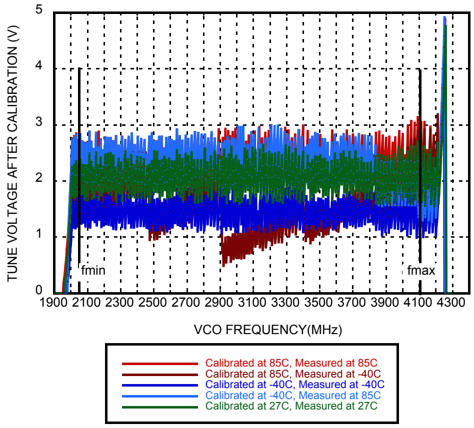

Figure 36. Typical VCO Tuning Voltage After Calibration

The calibration is normally run automatically once for every change of frequency. This ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally have to be concerned about which switch setting is used for a given frequency as this is handled by the AutoCal routine. The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency, and ensures that the VCO will stay locked and perform well over it's full temperature range without additional calibration, regardless of the temperature that the VCO was calibrated at.

Auto-Calibration can also be disabled allowing manual VCO tuning. Refer to section 1.2.1.5 for a description of manual tuning.

1.2.1.2.2 Auto-reLock on Lock Detect Failure

It is possible by setting Reg 0Ah[17] to have the VCO subsystem automatically re-run the calibration routine and re-lock itself if Lock Detect indicates an unlocked condition for any reason. With this option the system will attempt to re-Lock only once.

1.2.1.3.3 VCO AutoCal on Frequency Change

Assuming Reg 0Ah[11]=*0*, the VCO calibration starts automatically whenever a frequency change is requested. If it is desired to rerun the AutoCal routine for any reason, at the same frequency, simply rewrite the frequency change with the same value and the AutoCal routine will execute again without changing final frequency.

1.2.1.4.4 VCO AutoCal Time & Accuracy

The VCO frequency is counted for T_{mmt}, the period of a single AutoCal measurement cycle.

$$T_{mmt} = T_{xtal} \cdot R \cdot 2^n \quad \text{(EQ 1)}$$

n is set by Reg 0Ah[2:0] and results in measurement periods which are multiples of the PD period, $T_{xtal}R$.

R is the reference path division ratio currently in use, Reg 02h

T_{xtal} is the period of the external reference (crystal) oscillator.

The VCO AutoCal counter will, on average, expect to register N counts, rounded down (floor) to the nearest integer, every PD cycle.

N is the ratio of the target VCO frequency, f_{vco}, to the frequency of the PD, f_{pd}, where N can be any rational number supported by the N divider.

N is set by the integer (N_{int} = Reg 03h) and fractional (N_{frac} = Reg 04h) register contents

$$N = N_{int} + N_{frac} / 2^{24} \quad \text{(EQ 2)}$$

The AutoCal state machine runs at the rate of the FSM clock, T_{FSM}, where the FSM clock frequency cannot be greater than 50 MHz.

$$T_{FSM} = T_{xtal} \cdot 2^{m} \quad \text{(EQ 3)}$$

m is 0, 2, 4 or 5 as determined by Reg 0Ah[14:13]

The expected number of VCO counts, V, is given by

$$V = floor\ (N \cdot 2^{n}) \quad \text{(EQ 4)}$$

The nominal VCO frequency measured, f_{vcom}, is given by

$$f_{vcom} = V \cdot f_{xtal} / (2^{n} \cdot R) \quad \text{(EQ 5)}$$

where the worst case measurement error, f_{err} , is:

$$f_{err} \approx \pm f_{pd} / 2^{n+1} \quad \text{(EQ 6)}$$

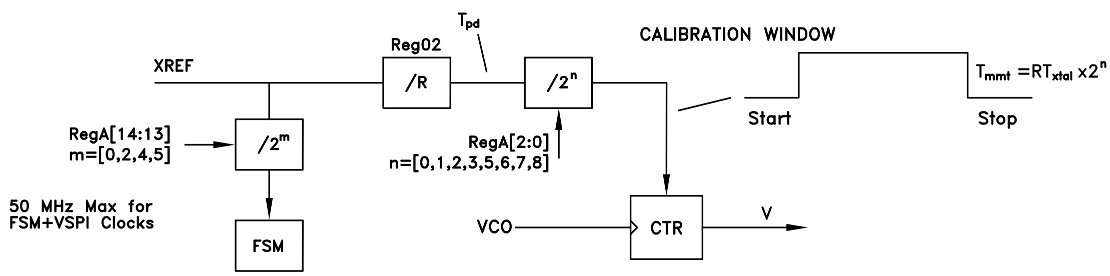

Figure 37. VCO Calibration

A 5-bit step tuned VCO, for example, nominally requires 5 measurements for calibration, worst case 6 measurements, and hence 7 VSPI data transfers of 20 clock cycles each. Total calibration time, worst case, is given by:

$$T_{cal} = k128T_{FSM} + 6T_{PD}\, 2^{n} + 7 \cdot 20T_{FSM} \quad \text{(EQ 7)}$$

or equivalently

$$T_{cal} = T_{xtal}\, (6R \cdot 2^{n} + (140+(3 \cdot 128)) \cdot 2^{m}) \quad \text{(EQ 8)}$$

For guaranteed hold of lock, across temperature extremes, the resolution should be better than 1/8th the frequency step caused by a VCO sub-band switch change. Better resolution settings will show no improvement.

1.2.1.4.1.1 VCO AutoCal Example

The HMC1197LP7FE must satisfy the maximum f_{pd} limited by the two following conditions:

a. N ≥ 16 (f_{int}), N ≥ 20.0 (f_{frac}), where N = f_{VCO}/ f_{pd}

b. f_{pd} ≤ 100 MHz

Suppose the HMC1197LP7FE output frequency is to operate at 2.01 GHz. Our example crystal frequency is f_{xtal} = *50 MHz, R=1, and m=0* (Figure 37), hence T_{FSM} = 20 ns (50 MHz). Note, when using AutoCal, the maximum AutoCal Finite State Machine (FSM) clock cannot exceed 50 MHz (see Reg 0Ah[14:13]). The FSM clock does not affect the accuracy of the measurement, it only affects the time to produce the result. This same clock is used to clock the 16 bit VCO serial port.

If time to change frequencies is not a concern, then one may set the calibration time for maximum accuracy, and therefore not be concerned with measurement resolution.

Using an input crystal of 50 MHz (R=1 and fpd=50 MHz) the times and accuracies for calibration using (EQ 6) and (EQ 8) are shown in Table 10 Where minimal tuning time is 1/8th of the VCO band spacing.

Across all VCOs, a measurement resolution better than 800 kHz will produce correct results. Setting m = 0, n = 5, provides 781 kHz of resolution and adds 8.6 µs of AutoCal time to a normal frequency hop. Once the AutoCal sets the final switch value, 8.64 µs after the frequency change command, the fractional register will be loaded, and the loop will lock with a normal transient predicted by the loop dynamics. Hence as shown in this example that AutoCal typically adds about 8.6 µs to the normal time to achieve frequency lock. Hence, AutoCal should be used for all but the most extreme frequency hopping requirements.

Table 10. AutoCal Example with F_{xtal} = 50 MHz, R = 1, m = 0

Control Value *Reg0Ah[2:0]*	n	2^n	T_{mmt} (µs)	T_{cal} (µs)	F_{err} Max
0	0	1	0.02	4.92	± 25 MHz
1	1	2	0.04	5.04	± 12.5 MHz
2	2	4	0.08	5.28	± 6.25 MHz
3	3	8	0.16	5.76	± 3.125 MHz
4	5	32	0.64	8.64	± 781 kHz
5	6	64	1.28	12.48	± 390 kHz
6	7	128	2.56	20.16	± 195 kHz
7	8	256	5.12	35.52	± 98 kHz

1.2.1.5 Manual VCO Calibration for Fast Frequency Hopping

If it is desirable to switch frequencies quickly it is possible to eliminate the AutoCal time by calibrating the VCO in advance and storing the switch number vs frequency information in the host. This can be done by initially locking the HMC1197LP7FE on each desired frequency using AutoCal, then reading, and storing the selected VCO switch settings. The VCO switch settings are available inReg 15h[8:1] after every AutoCal operation. The host must then program the VCO switch settings directly when changing frequencies. Manual writes to the VCO switches are executed immediately as are writes to the integer and fractional registers when AutoCal is disabled. Hence frequency changes with manual control and AutoCal disabled, requires a minimum of two serial port transfers to the HMC1197LP7FE, once to set the VCO switches, and once to set the PLL frequency.

If AutoCal is disabled Reg 0Ah[11]=1, the VCO will update its registers with the value written via Reg 15h[8:1] immediately.

1.2.2 Registers required for Frequency Changes in Fractional Mode

A large change of frequency, in fractional mode (Reg 06h[11]=1), may require Main Serial Port writes to:

1. The integer register intg, Reg 03h *(only required if the integer part changes)*
2. Manual VCO Tuning Reg 15h only required for manual control of VCO if Reg 0Ah[11]=1 *(AutoCal disabled)*

3. VCO Divide Ratio and Gain Register
    - Reg 16h[5:0] is required to change the VCO Output Divider value if needed.
    - Reg 16h[10:6] is required to change the Output Gain if needed.
4. The fractional register, Reg 04h. The fractional register write triggers AutoCal if Reg 0Ah[11]=0, and is loaded into the Delta Sigma modulator automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah[11]=1, the fractional frequency change is loaded into the Delta Sigma modulator immediately when the register is written with no adjustment to the VCO.

Small steps in frequency in fractional mode, with AutoCal enabled (Reg 0Ah[11]=0), usually only require a single write to the fractional register. Worst case, 3 Main Serial Port transfers to the HMC1197LP7FE could be required to change frequencies in fractional mode. If the frequency step is small and the integer part of the frequency does not change, then the integer register is not changed. In all cases, in fractional mode, it is necessary to write to the fractional register Reg 04h for frequency changes.

1.2.3 Registers Required for Frequency Changes in Integer Mode

A change of frequency, in integer mode (Reg 06h[11]=0), requires Main Serial Port writes to:

1. VCO register
    - Reg 15h only required for manual control of VCO if Reg 0Ah[11]=1 (AutoCal disabled)
    - Reg 16h is required to change the VCO Output Divider value if needed
2. The integer register Reg 03h.
    - In integer mode, an integer register write triggers AutoCal if Reg 0Ah[11]=0, and is loaded into the prescaler automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah[11]=1, the integer frequency change is loaded into the prescaler immediately when written with no adjustment to the VCO. Normally changes to the integer register cause large steps in the VCO frequency, hence the VCO switch settings must be adjusted. AutoCal enabled is the recommended method for integer mode frequency changes. If AutoCal is disabled (Reg 0Ah[11]=1), a prior knowledge of the correct VCO switch setting and the corresponding adjustment to the VCO is required before executing the integer frequency change.

1.2.4 VCO Output Mute Function

The HMC1197LP7FE features an intelligent output mute function with the capability to disable the VCO output while maintaining the PLL and VCO subsystems fully functional. The mute function is automatically controlled by the HMC1197LP7FE, and provides a number of mute control options including:

1. Always mute (Reg 16h[5:0] = 0d). This mode is used for manual mute control.
2. Automatically mute the outputs during VCO calibration (Reg 17h[7] = 1) that occurs during output frequency changes.

This mode can be useful in eliminating any out of band emissions during freqeuncy changes, and ensuring that the system emits only desired frequencies. It is enabled by writing Reg 17h[7] = 1. Typical isolation when the HMC1197LP7FE is muted is always better than 60 dB, and is ~ 30 dB better than disabling the output buffers of the HMC1197LP7FE via Reg 17h[5:4].

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1.3 PLL Overview

1.3.1 Charge Pump (CP) & Phase Detector (PD)

The Phase detector (PD) has two inputs, one from the reference path divider and one from the RF path divider. When in lock these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. We refer to the frequency of operation of the PD as f_{pd}. Most formulae related to step size, delta-sigma modulation, timers etc., are functions of the operating frequency of the PD, f_{pd}. f_{pd} is also referred to as the comparison frequency of the PD.

The PD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians (±360°) of input phase difference.

1.3.1.1 Charge Pump

A simplified diagram of the charge pump is shown in Figure 38. The CP consists of 4 programmable current sources, two controlling the CP Gain (Up Gain Reg 09h[13:7], and Down Gain Reg 09h[6:0]) and two controlling the CP Offset, where the magnitude of the offset is set by Reg 09h [20:14], and the direction is selected by Reg 09h [21]=1 for up and Reg 09h [22]=1 for down offset.

CP Gain is used at all times, while CP Offset is only recommended for fractional mode of operation. Typically the CP Up and Down gain settings are set to the same value (Reg 09h[13:7] = Reg 09h[6:0]).

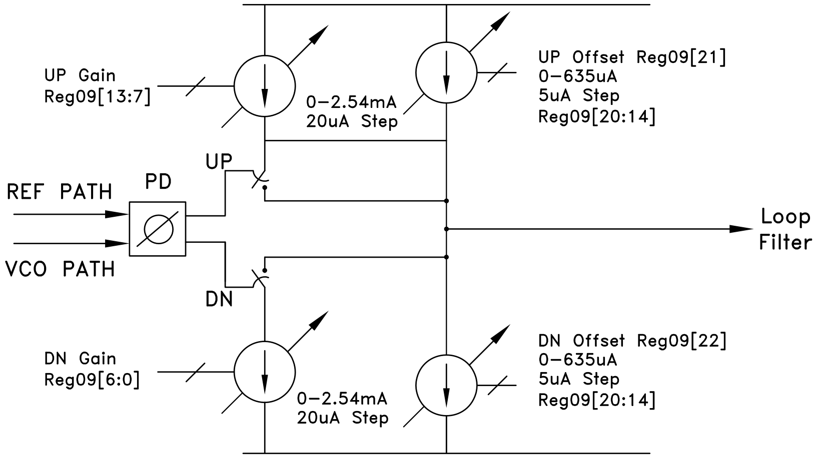

Figure 38. Charge Pump Gain & Offset Control

1.3.1.2 Charge Pump Gain

Charge pump Up and Down gains are set by Reg 09h[13:7] and Reg 09h[6:0] respectively. The current gain of the pump in Amps/radian is equal to the gain setting of this register divided by 2π.

Typical CP gain setting is set to 2 to 2.5 mA, however lower values can also be used. Values < 1 mA may result in degraded Phase Noise performance.

For example, if both Reg 09h[13:7] and Reg 09h[6:0] are set to ‘50d’ the output current of each pump will be 1 mA and the phase frequency detector gain k_p = 1 mA/2π radians, or 159 µA/rad.

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1.3.1.3 Charge Pump Phase Offset

In Integer Mode, the phase detector operates with zero offset. The divided reference signal and the divided VCO signal arrive at the phase detector inputs at the same time. Integer mode does not require any CP Offset current. When operating in Integer Mode simply disable CP offset in both directions (Up and down), by writing Reg 09h[22:21] = '00'b and set the CP Offset magnitude to zero by writingReg 09h[20:14]= 0.

In Fractional Mode CP linearity is of paramount importance. Any non-linearity degrades phase noise and spurious performance.

In fractional mode, these non-linearities are eliminated by operating the PD with an average phase offset, either positive or negative (either the reference or the VCO edge always arrives first at the PD ie. leads).

A programmable CP offset current source is used to add DC current to the loop filter and create the desired phase offset. Positive current causes the VCO to lead, negative current causes the reference to lead.

The CP offset is controlled via Reg 09h[20:14]. The phase offset is scaled from 0 degrees, that is the reference and the VCO path arrive in phase, to 360 degrees, where they arrive a full cycle late.

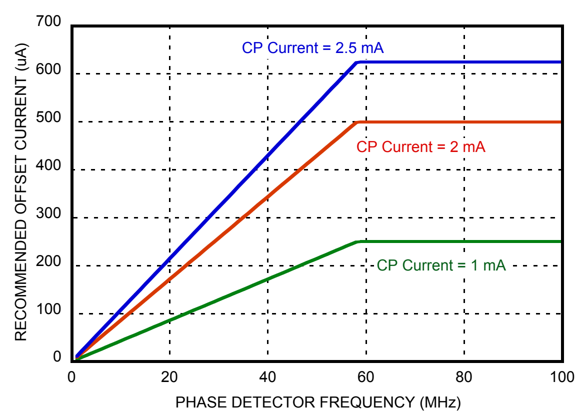
The specific level of charge pump offset current Reg 09h[20:14] is provided in (EQ 9). It is also plotted in Figure 39 vs. PD frequency for typical CP Gain currents.

$$\text{Required CP Offset} = \min\left[\left(4.3\times10^{-9}\times F_{PD}\times I_{CP}\right), 0.25\times I_{CP}\right] \qquad \text{(EQ 9)}$$

where:

F_{PD}: Comparison frequency of the Phase Detector (Hz)

I_{CP}: is the full scale current setting (A) of the switching charge pump (set in Reg 09h[6:0], [13:7]



Recommended CP offset current vs PD frequency for typical CP gain currents. Calculated using (EQ 9)

The required CP offset current should never exceed 25 % of the programmed CP current. It is recommended to enable the Up Offset and disable the Down Offset by writing Reg 09h[22:21] = '10'b.

Operation with CP offset influences the required configuration of the Lock Detect function. Refer to the description of Lock Detect function in section 1.3.5.

When operating with PD frequency >=80MHz, the CP Offset current should be disabled for the frequency change and then re-enabled after the PLL has settled. If the CP Offset current is enabled during a frequency change it may not lock.

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1.3.1.4 Phase Detector Functions

Phase detector register Reg 0Bhallows manual access to control special phase detector features.

Setting Reg 0Bh[5] = 0, masks the PD up output, which prevents the charge pump from pumping up.`

Setting (Reg 0Bh[6]) = 0*,* masks the PD down output, which prevents the charge pump from pumping down.

Clearing both Reg 0Bh[5] and Reg 0Bh[6] tri-states the charge pump while leaving all other functions operating internally.

PD Force UP Reg 0Bh[9] = 1 and PD Force DN Reg 0Bh[10] = 1 allows the charge pump to be forced up or down respectively. This will force the VCO to the ends of the tuning range which can be useful in VCO testing.

1.3.2 Reference Input Stage

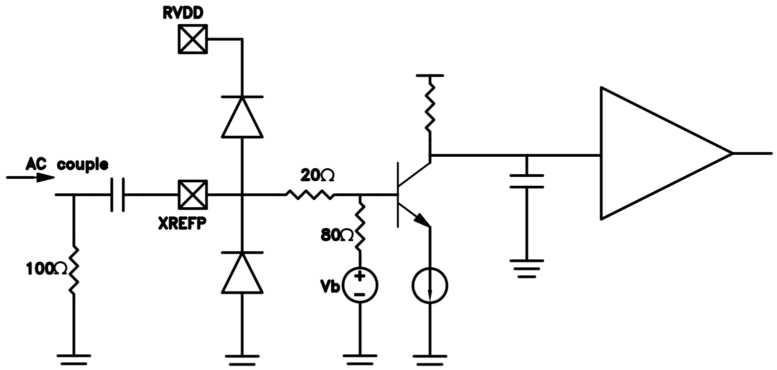

Figure 39. Reference Path Input Stage

The reference buffer provides the path from an external reference source (generally crystal based) to the R divider, and eventually to the phase detector. The buffer has two modes of operation controlled by Reg 08h[21]. High Gain (Reg 08h[21] = 0), recommended below 200 MHz, and High frequency (Reg 08h[21] = 1), for 200 to 350 MHz operation. The buffer is internally DC biased, with 100 Ω internal termination. For 50 Ω match, an external 100 Ω resistor to ground should be added, followed by an AC coupling capacitor (impedance < 1 Ω), then to the XREFP pin of the part.

At low frequencies, a relatively square reference is recommended to keep the input slew rate high. At higher frequencies, a square or sinusoid can be used. The following table shows the recommended operating regions for different reference frequencies. If operating outside these regions the part will normally still operate, but with degraded reference path phase noise performance.

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Table 11. Reference Sensitivity Table

	Square Input			Sinusoidal Input		
Reference Input Frequency (MHz)	Slew > 0.5V/ns	Recommended Swing (Vpp)			Recommended Power Range (dBm)	
	Recommended	Min	Max	Recommended	Min	Max
< 10	YES	0.6	2.5	x	x	x
10	YES	0.6	2.5	x	x	x
25	YES	0.6	2.5	ok	8	15
50	YES	0.6	2.5	YES	6	15
100	YES	0.6	2.5	YES	5	15
150	ok	0.9	2.5	YES	4	12
200	ok	1.2	2.5	YES	3	8

Input referred phase noise of the PLL when operating at 50 MHz is between -148 and -150 dBc/Hz at 10 kHz offset depending upon the mode of operation. The input reference signal should be 10 dB better than this floor to avoid degradation of the PLL noise contribution. It should be noted that such low levels are only necessary if the PLL is the dominant noise contributor and these levels are required for the system goals.

1.3.3 Reference Path 'R' Divider

The reference path "R" divider is based on a 14-bit counter and can divide input signals by values from 1 to 16,383 and is controlled via Reg 02h.

1.3.4 RF Path 'N' Divider

The main RF path divider is capable of average divide ratios between 2^{19}-5 (524,283) and 20 in fractional mode, and 2^{19}-1 (524,287) to 16 in integer mode.

1.3.5 Lock Detect

The Lock Detect (LD) function indicates that the HMC1197LP7FE is indeed generating the desired frequency. It is enabled by writing Reg 07h[11]=1. The HMC1197LP7FE provides LD indicator in one of two ways:

- As an output available on the LD_SDO pin of the HMC1197LP7FE, (Configuration is required to use the LD_SDO pin for LD purpose, for more information please see "1.8 Serial Port Open Mode" and "1.3.5.3 Configuring LD_SDO Pin for LD Output" section).
- Or reading from Reg 12h[1], where Reg 12h[1] = 1 indicates locked and Reg 12h[1] = 0 indicates an unlocked condition.

The LD circuit expects the divided VCO edge and the divided reference edge to appear at the PD within a user specified time period (window), repeatedly. Either signal may arrive first, only the difference in arrival times is significant. The arrival of the two edges within the designated window increments an internal counter. Once the count reaches and exceeds a user specified value (Reg 07h[2:0]) the HMC1197LP7FE declares lock.

Failure in registering the two edges in any one window resets the counter and immediately declares an un-locked condition. Lock is deemed to be reestablished once the counter reaches the user specified value (Reg 07h[2:0]) again.

1.3.5.1 Lock Detect Configuration

Optimal spectral performance in fractional mode requires CP current and CP offset current configuration discussed in detail in section "1.3.1".

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These settings in Reg 09h impact the required LD window size in fractional mode of operation. To function, the required lock detect window size is provided by (EQ 10).

$$\text{LD Window}\left(\text{seconds}\right)=\frac{\left(\frac{I_{CP\,Offset}\left(A\right)}{F_{PD}\left(Hz\right)\times I_{CP}\left(A\right)}+2.66\times10^{-9}\left(\text{sec}\right)+\frac{1}{F_{PD}\left(Hz\right)}\right)}{2}\text{ in Fractional Mode} \qquad \text{(EQ 10)}$$

$$\text{LD Window}\left(\text{seconds}\right)=\frac{1}{2\times F_{PD}}\text{in Integer Mode}$$

where:

F_{PD}: is the comparison frequency of the Phase Detector

$I_{CP\,Offset}$: is the Charge Pump Offset Current Reg 09h[20:14]

I_{CP}: is the full scale current setting of the switching charge pump Reg 09h[6:0], or Reg 09h[13:7]

If the result provided by (EQ 10) is equal to 10 ns Analog LD can be used (Reg 07h[6] = 0). Otherwise Digital LD is necessary Reg 07h[6] = 1.

Table 12 provides the required Reg 07h settings to appropriately program the Digital LD window size. From Table 12, simply select the closest value in the “Digital LD Window Size” columns to the one calculated in (EQ 10) and program Reg 07h[9:8] and Reg 07h[7:5] accordingly.

Table 12. Typical Digital Lock Detect Window

LD Timer Speed Reg07[9:8]	**Digital Lock Detect Window Size Nominal Value (ns)**							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	7.1	9.2	13.3	22	38	72	138	272
Slowest 11	7.6	10.2	15.4	26	47	88	172	338
LD Timer Divide Setting Reg07[7:5]	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**

1.3.5.2 Digital Window Configuration Example

Assuming, fractional mode, with a 50 MHz PD and

- Charge Pump gain of 2 mA (Reg 09h[13:7] = 64h, Reg 09h[6:0] = 64h),
- Down Offset (Reg 09h[22:21] = ‘10’b)
- Offset current magnitude of +400 µA (Reg 09h[20:14] = 50h)

Applying (EQ 11), the required LD window size is:

$$\text{LD Window}\left(\text{seconds}\right)=\frac{\left(\frac{0.4x10^{-3}\left(A\right)}{50\times10^{6}\left(Hz\right)\times2x10^{-3}\left(A\right)}+2.66\times10^{-9}\left(\text{sec}\right)+\frac{1}{50\times10^{6}\left(Hz\right)}\right)}{2}=13.33\text{ nsec} \qquad \text{(EQ 11)}$$

Locating the Table 12 value that is closest to the (EQ 11) result, in this case 13.3 ≈ 13.33. To set the Digital LD window size, simply program Reg 07h[9:8] = ‘10’b and Reg 07h[7:5] = ‘010’b according to Table 12.

There is always a good solution for the lock detect window for a given operating point. The user should understand however that one solution does not fit all operating points. As observed from (EQ 11), If charge pump offset or PD frequency are changed significantly then the lock detect window may need to be adjusted.

1.3.5.3 Configuring LD_SDO Pin for LD Output

Setting Reg 0Fh*[4:0]=1* will display the Lock Detect Flag on LD_SDO pin of the HMC1197LP7FE. If locked, LD_SDO will be high. As the name suggests, LD_SDO pin is multiplexed between LD and SDO (Serial Data Out) signals. Hence LD is available on the LD_SDO pin at all times except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin, and returns to the Lock Detect Flag after the read is completed.

LD can be made available on LD_SDO pin at all times by writing Reg 0Fh*[6]* = 1. In that case the HMC1197LP7FE will not provide any read-back functionality because the SDO signal is not available.

1.3.6 Cycle Slip Prevention (CSP)

When changing VCO frequency and the VCO is not yet locked to the reference, the instantaneous frequencies of the two PD inputs are different, and the phase difference of the two inputs at the PD varies rapidly over a range much greater than ±2π radians. Since the gain of the PD varies linearly with phase up to ±2π, the gain of a conventional PD will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. The output current from the charge pump will cycle from maximum to minimum even though the VCO has not yet reached its final frequency.

The charge on the loop filter small cap may actually discharge slightly during the low gain portion of the cycle. This can make the VCO frequency actually reverse temporarily during locking. This phenomena is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically. Cycle Slipping increases the time to lock to a value greater than that predicted by normal small signal Laplace analysis.

The HMC1197LP7FE PD features an ability to reduce cycle slipping during frequency tunning. The Cycle Slip Prevention (CSP) feature increases the PD gain during large phase errors.

1.3.7 Frequency Tuning

HMC1197LP7FE VCO subsystem always operates in fundamental frequency of operation (2050 MHz to 4100 MHz). The HMC1197LP7FE generates frequencies below its fundamental frequency (33 MHz to 2050 MHz) by tuning to the appropriate fundamental frequency and selecting the appropriate Output Divider setting (divide by 2/4/6.../60/62) in Reg 16h[5:0].

The HMC1197LP7FE automatically controls frequency tuning in the fundamental band of operation, for more information see “1.2.1 VCO Calibration”.

To tune to frequencies below the fundamental frequency range (<2050 MHz) it is required to tune the HMC1197LP7FE to the appropriate fundamental frequency, then select the appropriate output divider setting (divide by 2/4/6.../60/62) in Reg 16h[5:0].

1.3.7.1 Integer Mode

The HMC1197LP7FE is capable of operating in integer mode. For Integer mode set the following registers

a. Disable the Fractional Modulator, Reg 06h*[11]=0*
b. Bypass the Modulator circuit, Reg 06h*[7]=1*

In integer mode the VCO step size is fixed to that of the PD frequency. Integer mode typically has 3 dB lower phase noise than fractional mode for a given PD operating frequency. Integer mode, however, often requires a lower PD frequency to meet step size requirements. The fractional mode advantage is that higher PD frequencies can be used, hence lower phase noise can often be realized in fractional mode. Charge Pump offset should be disabled in integer mode Reg 09h[22:14] = 0h.

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1.3.7.2 Integer Frequency Tuning

In integer mode the digital ΔΣ modulator is shut off and the N divider (Reg 03h) may be programmed to any integer value in the range 16 to 2^{19}-1. To run in integer mode configure Reg 06h as described, then program the integer portion of the frequency as explained by (EQ 12), ignoring the fractional part.

a. Disable the Fractional Modulator, Reg 06h[11] = 0
b. Bypass the delta-sigma modulator Reg 06h[7] = 1
c. To tune to frequencies (<2050 MHz), select the appropriate output divider valueReg 16h[5:0].

1.3.7.3 Fractional Mode

The HMC1197LP7FE is placed in fractional mode by setting the following registers:

a. Enable the Fractional Modulator, Reg 06h*[11]=1*
b. Connect the delta sigma modulator in circuit, Reg 06h*[7]=0*

1.3.7.4 Fractional Frequency Tuning

This is a generic example, with the goal of explaining how to program the output frequency. Actual variables are dependant upon the reference in use.

The HMC1197LP7FE in fractional mode can achieve frequencies at fractional multiples of the reference. The frequency of the HMC1197LP7FE, f_{vco}, is given by

$$f_{vco} = \frac{f_{xtal}}{R}\left(N_{int} + N_{frac}\right) = f_{int} + f_{frac} \qquad \text{(EQ 12)}$$

$$f_{out} = f_{vco} / k \qquad \text{(EQ 13)}$$

Where:

f_{out}	is the output frequency after any potential dividers.
k	is 1 for fundamental, or k = 2,4,6,…58,60,62 depending on the selected output divider value (Reg 16h[5:0])
N_{int}	is the integer division ratio, Reg 03h, an integer number between 20 and 524,284
N_{frac}	is the fractional part, from 0.0 to 0.99999...,N_{frac}=Reg 04h/2^{24}
R	is the reference path division ratio, Reg 02h
f_{xtal}	is the frequency of the reference oscillator input
f_{pd}	is the PD operating frequency, f_{xtal}/R

As an example:

f_{out}	1402.5 MHz
k	2
f_{vco}	2,805 MHz
f_{xtal}	= 50 MHz
R	= 1
f_{pd}	= 50 MHz
N_{int}	= 56
N_{frac}	= 0.1

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Reg 04h = round(0.1 x 2^{24}) = round(1677721.6) = 1677722

$$f_{VCO} = \frac{50e6}{1}\left(56 + \frac{1677722}{2^{24}}\right) = 2805\ MHz + 1.192\ Hz\ error \quad \text{(EQ 14)}$$

$$f_{out} = \frac{f_{VCO}}{2} = 1402.5\ MHz + 0.596\ Hz\ error \quad \text{(EQ 15)}$$

In this example the output frequency of 1402.5 MHz is achieved by programming the 19-bit binary value of 56d = 38h into *intg_reg* in Reg 03h, and the 24-bit binary value of 1677722d = 19999Ah into *frac_reg* in Reg 04h. The 0.596 Hz quantization error can be eliminated using the exact frequency mode if required. In this example the VCO output fundamental 2805 MHz is divided by 2 (Reg 16h[5:0] = 2h) = 1402.5 MHz.

1.3.7.5 Exact Frequency Tuning

Due to quantization effects, the absolute frequency precision of a fractional PLL is normally limited by the number of bits in the fractional modulator. For example, a 24 bit fractional modulator has frequency resolution set by the phase detector (PD) comparison rate divided by 2^{24}. The value 2^{24} in the denominator is sometimes referred to as the modulus. Hittite PLLs use a fixed modulus which is a binary number. In some types of fractional PLLs the modulus is variable, which allows exact frequency steps to be achieved with decimal step sizes. Unfortunately small steps using small modulus values results in large spurious outputs at multiples of the modulus period (channel step size). For this reason Hittite PLLs use a large fixed modulus. Normally, the step size is set by the size of the fixed modulus. In the case of a 50 MHz PD rate, a modulus of 2^{24} would result in a 2.98 Hz step resolution, or 0.0596 ppm. In some applications it is necessary to have exact frequency steps, and even an error of 3 Hz cannot be tolerated.

Fractional PLLs are able to generate exact frequencies (with zero frequency error) if N can be exactly represented in binary (eg. N = 50.0,50.5,50.25,50.75 etc.). Unfortunately, some common frequencies cannot be exactly represented. For example, N_{frac} = 0.1 = 1/10 must be approximated as round((0.1 x 2^{24})/ 2^{24}) ≈ 0.100000024. At f_{PD} = 50 MHz this translates to 1.2 Hz error. Hittite's exact frequency mode addresses this issue, and can eliminate quantization error by programming the channel step size to F_{PD}/10 in Reg 0Ch to 10 (in this example). More generally, this feature can be used whenever the desired frequency, f_{VCO}, can be exactly represented on a step plan where there are an integer number of steps (<2^{24}) across integer-N boundaries. Mathematically, this situation is satisfied if:

$$f_{VCOk} \bmod \left(f_{gcd}\right) = 0 \quad \text{where}\ f_{gcd} = \gcd(f_{VCO1}, f_{PD})\ and\ f_{gcd} \geq \left(\frac{f_{PD}}{2^{24}}\right) \quad \text{(EQ 16)}$$

Where:

gcd stands for Greatest Common Divisor

f_N = maximum integer boundary frequency < f_{VCO1}

f_{PD} = frequency of the Phase Detector

and f_{VCOk} are the channel step frequencies where 0 < k < 2^{24}-1, As shown in Figure 40.

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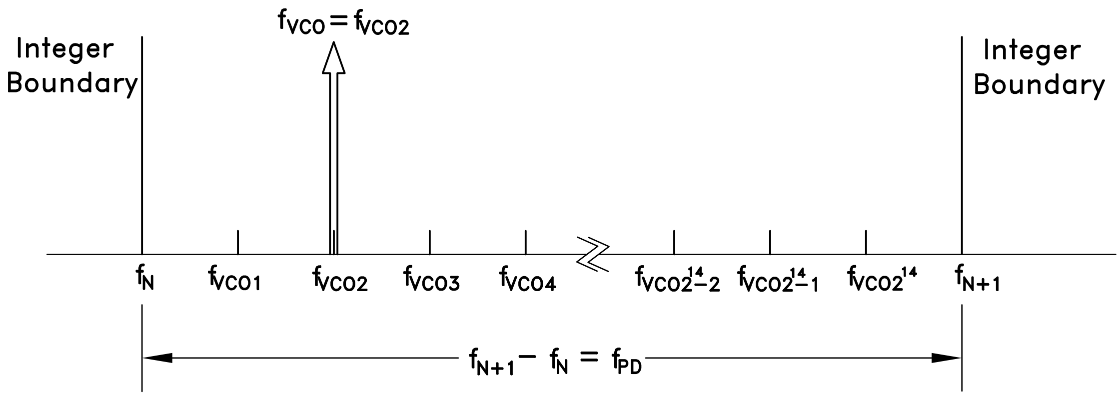

Figure 40. Exact Frequency Tuning

Some fractional PLLs are able to achieve this by adjusting (shortening) the length of the Phase Accumulator (the denominator or the modulus of the Delta-Sigma modulator) so that the Delta-Sigma modulator phase accumulator repeats at an exact period related to the interval frequency (f_{VCOk} - $f_{VCO(k-1)}$) in Figure 40. Consequently, the shortened accumulator results in more frequent repeating patterns and as a result often leads to spurious emissions at multiples of the repeating pattern period, or at harmonic frequencies of f_{VCOk} - $f_{VCO(k-1)}$. For example, in some applications, these intervals might represent the spacing between radio channels, and the spurious would occur at multiples of the channel spacing.

The Hittite method on the other hand is able to generate exact frequencies between adjacent integer-N boundaries while still using the full 24 bit phase accumulator modulus, thus achieving exact frequency steps with a high phase detector comparison rate, which allows Hittite PLLs to maintain excellent phase noise and spurious performance in the Exact Frequency Mode.

1.3.7.6 Using Hittite Exact Frequency Mode

If the constraint in (EQ 16) is satisfied, HMC1197LP7FE is able to generate signals with zero frequency error at the desired VCO frequency. Exact Frequency Mode may be re-configured for each target frequency, or be set-up for a fixed f_{gcd} which applies to all channels.

1.3.7.6.1.1 Configuring Exact Frequency Mode For a Particular Frequency

1. Calculate and program the integer register setting Reg 03h = N_{INT} = floor(f_{VCO}/f_{PD}), where the floor function is the rounding down to the nearest integer. Then the integer boundary frequency $f_N = N_{INT} \cdot f_{PD}$
2. Calculate and program the exact frequency register value Reg 0Ch = f_{PD}/f_{gcd}, where f_{gcd} = gcd(f_{VCO},f_{PD})
3. Calculate and program the fractional register setting Reg 04h $N_{FRAC} = \text{ceil}\left(\frac{2^{24}\left(f_{VCOk} - f_N\right)}{f_{PD}}\right)$, where ceil is the ceiling function meaning "round up to the nearest integer."

Example: To configure the HMC1197LP7FE for exact frequency mode at f_{VCO} = 2800.2 MHz where Phase Detector (PD) rate f_{PD} = 61.44 MHz Proceed as follows:

Check (EQ 16) to confirm that the exact frequency mode for this f_{VCO} is possible.

$$f_{gcd} = \text{gcd}(f_{VCO}, f_{PD})\ and\ f_{gcd} \geq \left(\frac{f_{PD}}{2^{24}}\right)$$

$$f_{gcd} = \text{gcd}\left(2800.2 \times 10^6, 61.44 \times 10^6\right) = 120 \times 10^3 > \frac{61.44 \times 10^6}{2^{24}} = 3750$$

Since (EQ 16) is satisfied, the HMC1197LP7FE can be configured for exact frequency mode at f_{VCO} = 2800.2 MHz as follows:

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1. N_{INT} = Reg 03h = $floor\left(\frac{f_{VCO1}}{f_{PD}}\right) = floor\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45d = 2Dh$

2. Reg 0Ch = $\frac{f_{PD}}{\gcd\left(\left(f_{VCOk+1} - f_{VCOk}\right), f_{PD}\right)} = \frac{61.44\times10^6}{\gcd\left(100\times10^3, 61.44\times10^6\right)} = \frac{61.44\times10^6}{20000} = 3072d = C00h$

3. To program Reg 04h, the closest integer-N boundary frequency f_N that is less than the desired VCO frequency f_{VCO} must be calculated. $f_N = f_{PD} \cdot N_{INT}$. Using the current example: $f_N = f_{PD} \times N_{INT} = 45 \times 61.44 \times 10^6 = 2764.8\,MHz$.

   Then $\text{Reg04h} = ceil\left(\frac{2^{24}\left(f_{VCO} - f_N\right)}{f_{PD}}\right) = ceil\left(\frac{2^{24}\left(2800.2\times10^6 - 2764.8\times10^6\right)}{61.44\times10^6}\right) = 9666560d = 938000h$

1.3.7.6.2.2 Hittite Exact Frequency Channel Mode

If it is desirable to have multiple, equally spaced, exact frequency channels that fall within the same interval (ie. $f_N \leq f_{VCOk} < f_{N+1}$) where f_{VCOk} is shown in Figure 40 and $1 \leq k \leq 2^{24}$, it is possible to maintain the same integer-N (Reg 03h) and exact frequency register (Reg 0Ch) settings and only update the fractional register (Reg 04h) setting. The Exact Frequency Channel Mode is possible if (EQ 16) is satisfied for at least two equally spaced adjacent frequency channels, i.e. the channel step size.

To configure the HMC1197LP7FE for Exact Frequency Channel Mode, initially and only at the beginning, integer (Reg 03h) and exact frequency (Reg 0Ch) registers need to be programmed for the smallest f_{VCO} frequency (f_{VCO1} in Figure 40), as follows:

1. Calculate and program the integer register setting Reg 03h = N_{INT} = floor(f_{VCO1}/f_{PD}), where f_{VCO1} is shown in Figure 40 and corresponds to minimum channel VCO frequency. Then the lower integer boundary frequency is given by $f_N = N_{INT} \cdot f_{PD}$.
2. Calculate and program the exact frequency register value Reg 0Ch = f_{PD}/f_{gcd}, where f_{gcd} = gcd((f_{VCOk+1} - f_{VCOk}),f_{PD}) = greatest common divisor of the desired equidistant channel spacing and the PD frequency ((f_{VCOk+1} - f_{VCOk}) and f_{PD}).

Then, to switch between various equally spaced intervals (channels) only the fractional register (Reg 04h) needs to be programmed to the desired VCO channel frequency f_{VCOk} in the following manner:

Reg04h = $N_{FRAC} = \text{ceil}\left(\frac{2^{24}\left(f_{VCOk} - f_N\right)}{f_{PD}}\right)$ where f_N=floor(f_{VCO1}/f_{PD}), and f_{VCO1}, as shown in Figure 40, represents the smallest channel VCO frequency that is greater than f_N.

Example: To configure the HMC1197LP7FE for Exact Frequency Mode for equally spaced intervals of 100 kHz where first channel (Channel 1) = f_{VCO1} = 2800.200 MHz and Phase Detector (PD) rate f_{PD} = 61.44 MHz proceed as follows:

First check that the exact frequency mode for this f_{VCO1} = 2800.2 MHz (Channel 1) and f_{VCO2} = 2800.2 MHz + 100 kHz = 2800.3 MHz (Channel 2) is possible.

$$f_{gcd1} = \gcd(f_{VCO1}, f_{PD})\; and\; f_{gcd1} \geq \left(\frac{f_{PD}}{2^{24}}\right) and\; f_{gcd2} = \gcd(f_{VCO2}, f_{PD})\; and\; f_{gcd2} \geq \left(\frac{f_{PD}}{2^{24}}\right)$$

$$f_{gcd1} = \gcd\left(2800.2\times10^6, 61.44\times10^6\right) = 120\times10^3 > \frac{61.44\times10^6}{2^{24}} = 3750$$

$$f_{gcd2} = \gcd\left(2800.3\times10^6, 61.44\times10^6\right) = 20\times10^3 > \frac{61.44\times10^6}{2^{24}} = 3750$$

If (EQ 16) is satisfied for at least two of the equally spaced interval (channel) frequencies $f_{VCO1}, f_{VCO2}, f_{VCO3}, \ldots f_{VCON}$, as it is above, Hittite Exact Frequency Channel Mode is possible for all desired channel frequencies, and can be configured as follows:

1. Reg 03h $= floor\left(\frac{f_{VCO1}}{f_{PD}}\right) = floor\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45d = 2Dh$
2. Reg 0Ch $= \frac{f_{PD}}{\gcd\left(\left(f_{VCOk+1} - f_{VCOk}\right), f_{PD}\right)} = \frac{61.44\times10^6}{\gcd\left(100\times10^3, 61.44\times10^6\right)} = \frac{61.44\times10^6}{20000} = 3072d = C00h$

   where (f_{VCOk+1} - f_{VCOk}) is the desired channel spacing (100 kHz in this example).
3. To program Reg 04h the closest integer-N boundary frequency f_N that is less than the smallest channel VCO frequency f_{VCO1} must be calculated. f_N = floor(f_{VCO1}/f_{PD}). Using the current example:

$$f_N = f_{PD}\times floor\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45\times61.44\times10^6 = 2764.8\,MHz$$

Then

$$\text{Reg 04h} = ceil\left(\frac{2^{24}\left(f_{VCO1} - f_N\right)}{f_{PD}}\right) \text{ for channel 1 where } f_{VCO1} = 2800.2\,MHz$$

$$= ceil\left(\frac{2^{24}\left(2800.2\times10^6 - 2764.8\times10^6\right)}{61.44\times10^6}\right) = 9666560d = 938000h$$

4. To change from channel 1 (f_{VCO1} = 2800.2 MHz) to channel 2 (f_{VCO2} = 2800.3 MHz), only Reg 04h needs to be programmed, as long as all of the desired exact frequencies f_{VCOk} (Figure 40) fall between the same integer-N boundaries ($f_N < f_{VCOk} < f_{N+1}$). In that case

$$\text{Reg 04h} = ceil\left(\frac{2^{24}\left(2800.3\times10^6 - 2764.8\times10^6\right)}{61.44\times10^6}\right) = 9693867d = 93EAABh$$

, and so on.

1.3.8 Seed Register

The start phase of the fractional modulator digital phase accumulator (DPA) may be set to any desired phase relative to the reference frequency, The phase is programmed in Reg 1Ah, and Exact Frequency Mode is required. Phase = 2π x Reg1Ah/(2^{24}) via the seed register Reg 1Ah[23:0]. The HMC1197LP7FE will automatically reload the start phase (seed value) into the DPA every time a new fractional frequency is selected. Certain zero or binary seed values may cause spurious energy correlation at specific frequencies. For most cases a random, or non zero, non-binary start seed is recommended.

1.4 Soft Reset & Power-On Reset

The HMC1197LP7FE features a hardware Power on Reset (POR). All chip registers will be reset to default states approximately 250 μs after power up.

The PLL subsystem SPI registers may also be soft reset by an SPI write to register Reg 00h.

1.5 Power Down Mode

Power down the HMC1197LP7FE by pulling CEN pin (pin 17) low (assuming no SPI overrides(Reg 01h[0]=1)). This will result in all analog functions and internal clocks disabled. Current consumption will typically drop below 10 μA in Power Down state. The serial port will still respond to normal communication in Power Down mode.

It is possible to ignore the CEN pin, by setting Reg 01h[0]=0. Control of Power Down Mode then comes from the serial port register Reg 01h[1].

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It is also possible to leave various blocks on when in Power Down *(see* Reg 01h*)*, including:

a. Internal Bias Reference Sources	Reg 01h*[2]*
b. PD Block	Reg 01h*[3]*
c. CP Block	Reg 01h*[4]*
d. Reference Path Buffer	Reg 01h*[5]*
e. VCO Path buffer	Reg 01h*[6]*
f. Digital I/O Test pads	Reg 01h*[7]*

To mute the output but leave the PLL and VCO locked please refer to 1.2.4 section.

1.6 General Purpose Output (GPO) Pin

The PLL shares the LD_SDO (Lock-Detect/Serial Data Out) pin to perform various functions. While the pin is most commonly used to read back registers from chip via the SPI, it is also capable of exporting a variety of signals and real time test waveforms (including Lock Detect). It is driven by a tri-state CMOS driver with ~200 Ω Rout. It has logic associated with it to dynamically select whether the driver is enabled, and to decide which data to export from the chip.

In its default configuration, after power-on-reset, the output driver is disabled, and only drives during appropriately addressed SPI reads. This allows it to share the output with other devices on the same bus.

The pin driver is enabled if the chip is addressed - ie. The last 3 bits of SPI cycle = ‘000’b before the rising edge of SEN. If SEN rises before SCK has clocked in an ‘invalid’ (non-zero) chip -address, the HMC1197LP7FE will start to drive the bus.

The WIDEBAND DIRECT QUADRATURE MODULATOR w/ Fractional- N PLL & VCO will naturally switch away from the GPO data and export the SDO during an SPI read. To prevent this automatic data selection, and always select the GPO signal, set “Prevent AutoMux of SDO” (Reg 0Fh[6] = 1). The phase noise performance at this output is poor and uncharacterized. The GPO output should not be toggling during normal operation because it may degrade the spectral performance.

Note that there are additional controls available, which may be helpful if sharing the bus with other devices:

- To disable the driver completely, set Reg 08h[5] = 0 (it takes precedence over all else).
- To disable either the pull-up or pull-down sections of the driver, Reg 0Fh[8] = 1 or Reg 0Fh[9] = 1 respectively.

Example Scenarios:

- Drive SDO during reads, tri-state otherwise (to allow bus-sharing)
  - No action required.
- Drive SDO during reads, Lock Detect otherwise
  - Set GPO Select Reg 0Fh [4:0] = ‘00001’b (which is default)
  - Set “Prevent GPO driver disable” (Reg 0Fh[7] = 1)
- Always drive Lock Detect
  - Set “ Prevent AutoMux of SDO” Reg 0Fh[6] = 1
  - Set GPO Select Reg 0Fh[4:0]= 00001 (which is default)
  - Set “Prevent GPO driver disable” (Reg 0Fh[7] = 1))

The signals available on the GPO are selected in Reg 0Fh[4:0].

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1.7 Chip Identification

The chip id information may be read by reading the content of read only register, chip_ID in Reg 00h. For HMC1197LP7FE, chip id is C7701Ah.

1.8 SERIAL PORT Overview

The SPI protocol has the following general features:

a. 3-bit chip address , enable the use of up to 8 devices connected to the serial bus
b. Simultaneous Write/Read during the SPI cycle
c. 5-bit address space
d. 3 wire for Write Only capability, 4 wire for Read/Write capability
Typical serial port operation can be run with SCLK at speeds up to 50 MHz.

1.8.1 Serial Port WRITE Operation

AVDD = DVDD = 3V, AGND = DGND = 0V

Table 13. SPI WRITE Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCLK Rising Edge	3			ns
t_2	SCLK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCLK 32 Rising Edge to SEN Rising Edge	10			ns
t_6	Recovery Time	10			ns
	Max Serial port Clock Speed		50		MHz

A typical WRITE cycle is shown in Figure 41.

a. The Master (host) places 24-bit data, d23:d0, MSB first, on SDI on the first 24 falling edges of SCLK.
b. the slave (HMC1197LP7FE) shifts in data on SDI on the first 24 rising edges of SCLK
c. Master places 5-bit register address to be written to, r4:r0, MSB first, on the next 5 falling edges of SCLK (25-29)
d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).
e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32). Hittite reserves chip address a2:a0 = 000 for HMC1197LP7FE.
f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).
g. Master asserts SEN after the 32nd rising edge of SCLK.
h. Slave registers the SDI data on the rising edge of SEN.
i. Master clears SEN to complete the WRITE cycle.

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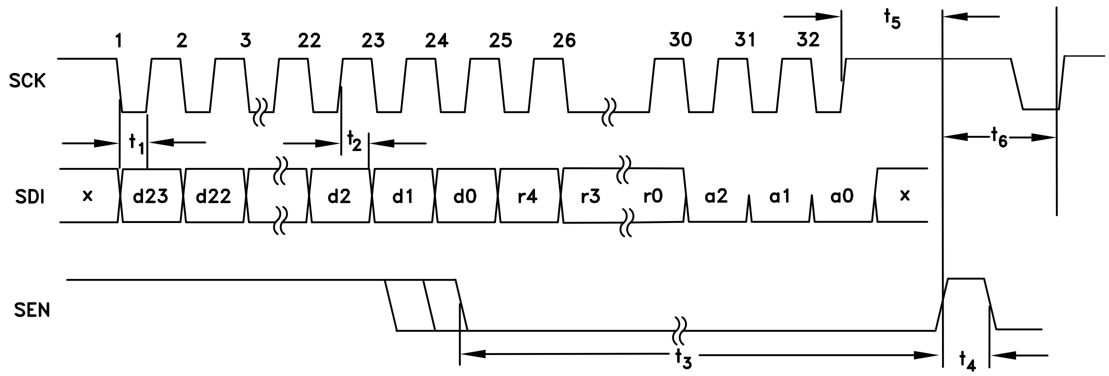

Figure 41. Serial Port Timing Diagram - WRITE

1.8.2 Serial Port READ Operation

A typical READ cycle is shown in Figure 42.

In general, the LD_SDO line is always active during the WRITE cycle. During any SPI cycle LD_SDO will contain the data from the current address written in Reg 00h[4:0]. If Reg 00h[4:0] is not changed then the same data will always be present on LD_SDO when an Open Mode cycle is in progress. If it is desired to READ from a specific address, it is necessary in the first SPI cycle to write the desired address to Reg 00h[4:0], then in the next SPI cycle the desired data will be available on LD_SDO.

An example of the two cycle procedure to read from any address follows:

a. The Master (host), on the first 24 falling edges of SCLK places 24-bit data, d23:d0, MSB first, on SDI as shown in Figure 42. d23:d5 should be set to zero. d4:d0 = address of the register to be READ on the next cycle.
b. the slave (HMC1197LP7FE) shifts in data on SDI on the first 24 rising edges of SCK
c. Master places 5-bit register address , r4:r0, (the READ ADDRESS register), MSB first, on the next 5 falling edges of SCK (25-29). r4:r0=00000.
d. Slave shifts the register bits on the next 5 rising edges of SCK (25-29).
e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCK (30-32). Chip address is always ‘000’b.
f. Slave shifts the chip address bits on the next 3 rising edges of SCK (30-32).
g. Master asserts SEN after the 32nd rising edge of SCK.
h. Slave registers the SDI data on the rising edge of SEN.
i. Master clears SEN to complete the the address transfer of the two part READ cycle.
j. If one does not wish to write data to the chip during the second cycle , then it is recommended to simply rewrite the same contents on SDI to Register zero on the READ back part of the cycle.
k. Master places the same SDI data as the previous cycle on the next 32 falling edges of SCK.
l. Slave (HMC1197LP7FE) shifts the SDI data on the next 32 rising edges of SCK. On these same edges, the slave places the desired read data (ie. data from the address specified in Reg 00h[4:0] of the first cycle) on LD_SDO which automatically switches to SDO mode from LD mode, disabling the LD output.
m. Master asserts SEN after the 32nd rising edge of SCK to complete the cycle and revert back to Lock Detect on LD_SDO.

Table 14. SPI Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCK Rising Edge	3			ns
t_2	SCK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCK Rising Edge to SDO time		8.2ns+0.2ns/pF		ns
t_6	Recovery TIme	10			ns
t_7	SCK 32 Rising Edge to SEN Rising Edge	10			ns

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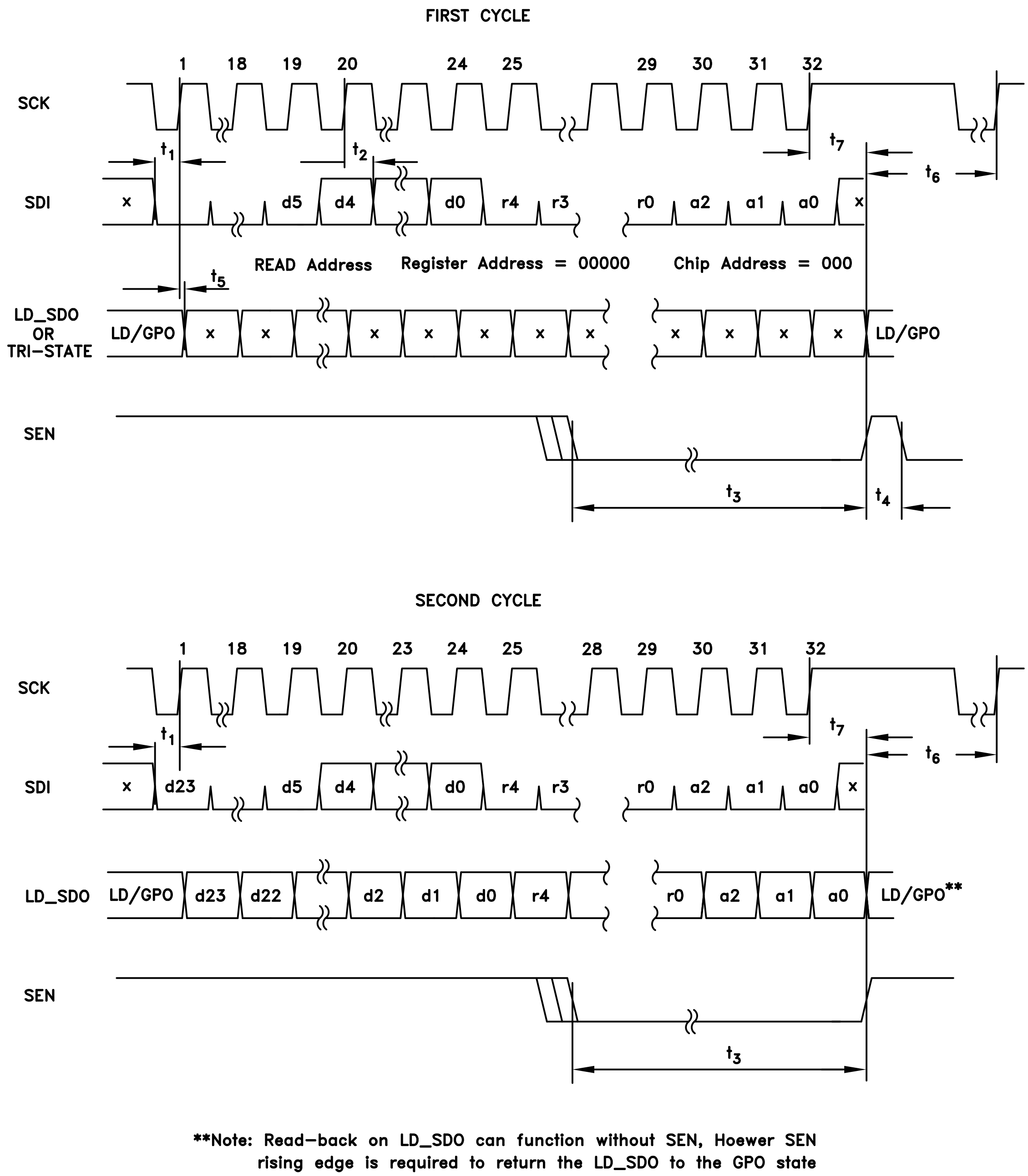

Figure 42. Serial Port Timing Diagram - READ

For more information on using the GPO pin while in SPI Mode please see section 1.8 Serial Port Overview

2.0 PLL Register Map

2.1 Reg 00h ID Register (Read Only) DEFAULT C7701A h

Bit	Type	Name	Width	Default	Description
[23:0]	RO	chip_ID	24	C7701A	Chip ID Number

2.2 Reg 00h Open Mode Read Address/RST Strobe Register (Write Only)

Bit	Type	Name	Width	Default	Description
[4:0]	WO	Read Address	5	-	(WRITE ONLY) Read Address for next cycle
[5]	WO	Soft Reset	1	-	(WRITE ONLY) Soft Reset - (set to 0 during operation)
[23:6]	WO	Not Defined	18	-	Not Defined (set to write 0h)

2.3 Reg 01h Chip Enable Register DEFAULT 3h

Bit	Type	Name	Width	Default	Description
[0]	R/W	Chip Enable Pin Select	1	1	1 = Chip enable via CHIP_EN pin, Reg 01h[0]=1 and CHIP_EN pin low places the HMC1197LP7FE in Power Down Mode 0 = Chip enable via SPI - Reg 01h[0] = 0, CHIP_EN pin ignored (see Power Down Mode description for more details)
[1]	R/W	SPI Chip Enable	1	1	Controls Chip Enable (Power Down) if Reg 01h[0] =0 Reg 01h[0]=0 and Reg 01h[1]=1 - chip is enabled, CHIP_EN pin don't care Reg 01h[0]=0 and Reg 01h[1]=0 - chip disabled, CHIP_EN pin don't care (see Power Down Mode description for more information)
[2]	R/W	Keep Bias On	1	0	keeps internal bias generators on, ignores Chip enable control
[3]	R/W	Keep PFD Pn	1	0	keeps PFD circuit on, ignores Chip enable control
[4]	R/W	Keep CP On	1	0	keeps Charge Pump on, ignores Chip enable control
[5]	R/W	Keep Reference Buffer ON	1	0	keeps Reference buffer block on, ignores Chip enable control
[6]	R/W	Keep VCO on	1	0	keeps VCO divider buffer on, ignores Chip enable control
[7]	R/W	Keep GPO Driver ON	1	0	keeps GPO output Driver ON, ignores Chip enable control
[9:8]	R/W	Reserved	2	0	reserved

2.4 Reg 02h REFDIV Register DEFAULT 1h

Bit	Type	Name	Width	Default	Description
[13:0]	R/W	rdiv	14	1	Reference Divider 'R' Value (EQ 8) min 1 max max 2^{14}-1 = 3FFFh = 16383d

2.5 Reg 03h Frequency Register - Integer Part DEFAULT 19h

Bit	Type	Name	Width	Default	Description
[18:0]	R/W	Integer Setting	19	25d 19h	Divider Integer part, used in all modes, see (EQ 10) Fractional Mode min 20d max 2^{19} - 4 = 7FFFCh = 524,284d Integer Mode min 16d max 2^{19}-1 = 7FFFFh = 524,287d

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2.6 Reg 04h Frequency Register - Fractional Part DEFAULT 0h

Bit	Type	Name	Width	Default	Description
[23:0]	R/W	Fractional Setting	24	0	Divider Fractional part (24 bit unsigned) see Fractional Frequency Tuning Fractional Division Value = Reg4[23:0]/2^24 Used in Fractional Mode only min 0 max 2^{24}-1 = FFFFFFh = 16,777,215d

2.7 Reg 05h Reserved

Bit	Type	Name	Width	Default	Description
[23:0]	R/W	Reserved	24	0	Reserved

2.8 Reg 06h Delta Sigma Modulator Register DEFAULT 30F0Ah

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[1:0]	R/W	Reserved	2	2	Reserved, Program to 0h
[3:2]	R/W	DSM Order	2	2	Select the Delta Sigma Modulator Type 0: 1st order 1: 2nd Order 2: 3rd Order - Recommended 3: Reserved
[4]	R/W	Synchronous SPI Mode	1	0	0: Normal SPI Load - all register load on rising edge of SEN 1: Synchronous SPI - registers Reg 03h, Reg 04h , Reg 1Ah wait to load synchronously on the next internal clock cycle. Normally (When this bit is 0) SPI writes into the internal state machines/counters happen asynchronously relative to the internal clocks. This can create freq/phase disturbances if writing register 3, 4 or 1A. When this bit is enabled, the internal SPI registers are loaded synchronously with the internal clock. This means that the data in the SPI shifter should be held constant for at least 2 PFD clock periods after SEN is asserted to allow this retiming to happen cleanly.
[5]	R/W	Exact Frequency Mode Enable	1	0	1: Exact Frequency Mode Enabled 0: Exact Frequency Mode Disabled
[6]	R/W	Reserved	1	0	Reserved
[7]	R/W	Fractional Bypass	1	0	0: Use Modulator, Required for Fractional Mode, 1: Bypass Modulator, Required for Integer Mode Note: When enabled fractional modulator output is ignored, but fractional modulator continues to be clocked if Reg 06h[11] =1. This feature can be used to test the isolation of the digital fractional modulator from the VCO output in integer mode.
[8]	R/W	Autoseed EN	1	1	1: loads the modulator seed (start phase) whenever the fractional register (Reg 04h) is written 0: when fractional register (Reg 04h) write changes frequency, modulator starts at previous value (phase)
[10:9]	R/W	Reserved	2	3	Reserved
[11]	R/W	Delta Sigma Modulator Enable	1	1	0: Disable DSM, used for Integer Mode 1: Enable DSM Core, required for Fractional Mode
[23:12]	R/W	Reserved	12	48d 30h	Reserved

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2.9 Reg 07h Lock Detect Register DEFAULT 200844 h

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	lkd_wincnt_max	3	4	lock detect window sets the number of consecutive counts of divided VCO that must land inside the Lock Detect Window to declare LOCK 0: 5 1: 32 2: 96 3: 256 4: 512 5: 2048 6: 8192 7: 65535
[10:3]	R/W	Reserved	8	8	Reserved
[11]	R/W	LD Enable	1	1	0: LD disable 1: LD enable
[19:12]	R/W	Reserved	8	0	Reserved
[20]	R/W	Lock Detect Training	9	0	0 to 1 transition triggers the training. Lock Detect Training is only required after changing Phase Detector frequency. After changing PD frequency a toggle Reg 07h[20] from 0 to 1 retrains the Lock Detect.
[21]	R/W	CSP Enable	1	1	Cycle Slip Prevention enable. When enabled, if the phase error becomes larger than approx 70% of the PFD period, the charge-pump gain is increased by approx 6mA for the duration of the cycle..
[23:22]	R/W	Reserved	2	0	Reserved

2.10 Reg 08h Analog EN Register DEFAULT 1BFFF h

Bit	Type	Name	Width	Default	Description
[4:0]	R/W	Reserved	5	31d	Reserved
[5]	R/W	GPO(General Purpose Output Pin Enable)	1	1d	0 - Pin LD_SDO disabled 1 - and RegFh[7]=1 , Pin LD_SDO is always driven, this is required for use of GPO port 1 - and RegFh[7]=0 LDO_SPI is off if chip address not equal to ‘000’b, allowing a shared SPI with other compatible parts
[9:6]	R/W	Reserved	4	15d	Reserved
[10]	R/W	VCO Buffer and Prescaler Bias Enable	1	1d	0: VCO Buffer and Prescaler Bias Disable 1: VCO Buffer and Prescaler Bias Enable Only applies to External VCO
[20:11]	R/W	Reserved	10	55d	Reserved
[21]	R/W	High Frequency Reference	1	0	Program to 1 for XTAL > 200 MHz, 0 otherwise
[22]	R/W	SDO Output Level	1	0d	Output Logic Level on LD/SDO pin 0: 1.8 V Logic Levels 1: DVDD3V Logic Level
[23]	R/W	Reserved	1	0d	Reserved

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2.11 Reg 09h Charge Pump Register DEFAULT 547264 h

Bit	Type	Name	Width	Default	Description
[6:0]	R/W	CP DN Gain	7	100d 64h	Charge Pump DN Gain Control 20 µA/step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 20 µA 2d = 40 µA ... 127d = 2.54mA Default 2mA
[13:7]	R/W	CP UP Gain	7	100d 64h	Charge Pump UP Gain Control 20 µA per step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 20 µA 2d = 40 µA ... 127d = 2.54mA Default 2mA
[20:14]	R/W	Offset Magnitude	7	81d	Charge Pump Offset Control 5 µA/step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 5 µA 2d = 10 µA ... 127d = 635 µA Default 405µA
[21]	R/W	Offset UP enable	1	0	Sets Direction of Reg 09h[20:14] Up, 0- UP Offset Off
[22]	R/W	Offset DN enable	1	1	Sets Direction of Reg 09h[20:14] Down, 0- DN Offset Off
[23]	R/W	HiK charge pump Mode	1	0	Only recommended with external VCOs and Active Loop Filters. When enabled the HMC1197LP7FE increases CP current by 3 mA, thereby improving phase noise performance, and increasing loop bandwidth

2.12 Reg 0Ah VCO AutoCal Configuration Register DEFAULT 2046 h

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	Vtune Resolution	3	6d	Used by internlan AutoCal state machine R Divider Cycles 0 - 1 1 - 2 2 - 4 3 - 8 4 - 32 5 - 64 6 - 128 7 - 256 div cycles for frequency measurement. Measurement should last > 4 µsec. Note: 1 does not work if R divider = 1.
[10:3]	R/W	Reserved	8	16d	Reserved
[11]	R/W	AutoCal Disable	1	0	0 = AutoCal Enabled 1 = AutoCal disabled
[12]	R/W	Reserved	1	0	Reserved
[14:13]	R/W	FSM/VSPI Clock Select	2	1	Set the AutoCal FSM and VSPI Clock (50 MHz maximum) 0: Input Crystal Reference 1: Input Crystal Reference/4 2: Input Crystal Reference/16 3: Input Crystal Reference/32
[16:15]	R/W	Reserved	2	0	Reserved
[17]	R/W	Auto relock - one Try	1	0	0: Does not attempt to relock if lock is lost 1: Attempts to relock if Lock Detect fails for any reason. Only tries once.
[23:18]	R/W	Reserved	5	0	Reserved

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2.13 Reg 0Bh PD/CP Register DEFAULT 78061 h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[3:0]	R/W	Reserved	4	1	Reserved
[4]	R/W	PD Phase Select	1	0	Inverts the PD polarity (program to 0) 0- Use with a positive tuning slope VCO and Passive Loop Filter (default when using internal VCO) 1- Use with a Negative Slope VCO or with an inverting Active Loop Filter with a Positive Slope VCO (Only recommended when using an External VCO, and an active loop filter)
[5]	R/W	PD Up Output Enable	1	1	Enables the PD UP output, see also Reg 0Bh[9]
[6]	R/W	PD Down Output Enable	1	1	Enables the PD DN output, see also Reg 0Bh[10]
[8:7]	R/W	Reserved	2	0	Reserved, Program to 0d.
[9]	R/W	Force CP UP	1	0	Forces CP UP output on if CP is not forced down - Use for Test only
[10]	R/W	Force CP DN	1	0	Forces CP DN output on if CP is not forced up - Use for Test only
[11]	R/W	Force CP Mid Rail	1	0	Force CP MId Rail - Use for Test only (if Force CP UP or Force CP DN are enabled they have precedence)
[23:12]	R/W	Reserved	12	120d 78h	Reserved.

2.14 Reg 0Ch Exact Frequency Register

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[23:0]	R/W	Number of Channels per Fpd	24	0	Comparison Frequency divided by the correction rate. Must be an integer. Frequencies at exactly the correction rate will have zero frequency error. Only works in modulator Mode B(3rd order recommended modulator type in Reg06[3:2]). Reg 0Ch must be 0 if using ohter DSM type 0: Disabled 1: Invalid ≥ 2 valid max 2^{24}-1 = FFFFFFh = 16,777,215d

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2.15 Reg 0Fh GPO Register

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[4:0]	R/W	GPO	5	1	Select signal to be output to SDO pin when enabled DEFAULT LOCK DETECT 0: Data from Reg0F[5] 1: Lock Detect Output 2. Lock Detect Trigger 3: Lock Detect Window Output 4: Ring Osc Test 5. Pullup Hard from CSP 6. PullDN hard from CSP 7. Reserved 8: Reference Buffer Output 9: Ref Divider Output 10: VCO divider Output 11. Modulator Clock from VCO divider 12. Auxiliary Clock 13. Aux SPI Clock 14. Aux SPI Enable 15. Aux SPI Data Out 16. PD DN 17. PD UP 18. SD3 Clock Delay 19. SD3 Core Clock 20. AutoStrobe Integer Write 21. Autostrobe Frac Write 22. Autostrobe Aux SPI 23. SPI Latch Enable 24. VCO Divider Sync Reset 25. Seed Load Strobe 26.-29 Not Used 30. SPI Output Buffer En 31. Soft RSTB
[5]	R/W	GPO Test Data	1	0	1 - GPO Test Data when GPO_Select = 0
[6]	R/W	Prevent Automux SDO	1	0	1- Outputs GPO data only 0- Automuxes between SDO and GPO data
[7]	R/W	Reserved	1	0	Reserved
[8]	R/W	Disable PFET	1	0	Program to 1 if external pull-ups are used on the SDO line (Prevents conflicts on the SPI bus)
[9]	R/W	Disable NFET	1	0	Program to 1 if external pull-downs are used on the SDO line (Prevents conflicts on the SPI bus)
[23:10]	R/W	Reserved	14	0	Reserved

2.16 Reg 10h Tuning Register DEFAULT 80 h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[7:0]	R	VCO Tune Curve	8	16d 10h	VCO selection resulting from AutoCalibration. 0- maximum frequency '1111 1111'b- minimum frequency
[8]	R	VCO Tuning Busy	1	0	Indicates if the VCO tuning is in process 1- Busy 0- Not Busy

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2.17 Reg 11h SAR Register (Read Only)

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[18:0]	R	SAR Error Magnitude Count	19	2^{19}- 1d 7FFFFh	SAR Error Magnitude Count
[19]	R	SAR Error Sign	1	0	SAR Error Sign 0: positive 1: negative
[23:20]	R	Reserved	4	0	Reserved

2.18 Reg 12h GPO/LD Register (Read Only)

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[0]	R	GPO Out	1	0	GPO Output
[1]	R	Lock Detect Out	1	0	Lock Detect Output
[23:2]	R	Reserved	22	7h	Reserved

2.19 Reg 13h BIST Register (Read Only)

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[16:0]	R	Reserved	16	4697d 1259h	Reserved

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2.20 Reg 14h Auxiliary SPI Register

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[0]	R/W	Aux SPI Mode	1	0	1- Use the 3 outputs as an SPI port 0- Use the 3 outputs as a static GPO port along with Reg 14h[3:1]
[3:1]	R/W	Aux GPO Values	3	0	3 Output values can be set indivually when Reg 10h [0] = 1
[4]	R/W	Aux GPO 3.3 V	1	0	0- 1.8 V output out of the Auxiliary GPO pins when Reg 10h [0] = 1 1- 3.3 V output out of the Auxiliary GPO pins when Reg 10h [0] = 1
[8:5]	R/W	Reserved	4	1	Reserved
[9]	R/W	Phase Sync	1	1	When set, CHIP_EN pin is used as a trigger for phase synchronization. Can be used to synchronize multiple HMC1197LP7FE, or to along with the Reg 1Ah value to phase step the output. (Exact Frequency Mode must be enabled)
[11:10]	R/W	Aux SPI GPO Output	2	0	Option to send GPO multiplexed data (ex Lock Detect) to one of the auxiliary outputs 0- None 1 - to [0] 2 - to [1] 3 - to [2]
[13:12]	R/W	Aux SPI Outputs	2	0	When disabled: 0 - Outputs Hi Z 1 - Outputs stay driven 2 - Outputs driven to high 3 - Outputs driven to low
[23:14]	R/W	Reserved	10	0	Reserved

2.21 Reg 15h Manual VCO Config Register Default F48A0 h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[0]	R/W	Manual Calibration Mode	1	0	1- VCO subsystem manual calibration enabled 0- VCO subsystem manual calibration disabled
[5:1]	R/W	Capacitor Switch Setting	5	16d 10h	capacitor switch setting
[8:6]	R/W	Manual VCO Selection	3	2	selects the VCO core sub-band
[9]	R/W	Manual VCO Tune Enable	1	0	1- Manual VCO tuning enabled 0- Manual VCO tuning disabled
[15:10]	R/W	Reserved	6	18d 12h	Reserved
[16]	R/W	Enable Auto-Scale CP current	1	1	1 - Automatically scale CP current based on VCO frequency and capacitor setting 0- Don't scale CP current
[23:17]	R/W	Reserved	7	7d	Reserved

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2.22 Reg 16h Gain Divider Register Default 6C1 h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[5:0]	R/W	RF Divide Ratio	6	1	0 - Mute, VCO and PLL buffer On, RF output stages Off 1 - Fo 2 - Fo/2 3 - invalid, defaults to 2 4 - Fo/2 5 - invalid, defaults to 4 6 - Fo/6 ... 60 - Fo/60 61 - invalid, defaults to 60 62 - Fo/62 > 62 - invalid, defaults to 62
[7:6]	R/W	LO Output Buffer Gain Control	2	3	3 - Max Gain 2 - Max Gain - 3 dB 1 - Max Gain - 6 dB 0 - Max Gain - 9 dB
[9:8]	R/W	LO2 Output Buffer gain Control	2	2	3 - Max Gain 2 - Max Gain - 3 dB 1 - Max Gain - 6 dB 0 - Max Gain - 9 dB
[10]	R/W	Divider Output Stage Gain Control	1	1	1 - Max Gain 0 - Max Gain - 3 dB
[23:11]	R/W	Reserved	13	0	Reserved

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2.23 Reg 17h Modes Register Default 1AB h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[0]	R/W	VCO SubSys Master Enable	1	1	Master enable for the entire VCO Subsystem 1 - Enable 0 - Disable Chip Enable is also required to set as enable mode.
[1]	R/W	VCO Enable	1	1	
[2]	R/W	External VCO Buffer Enable	1	0	External VCO Buffer to output stage enable. Only used when locking an external VCO.
[3]	R/W	PLL Buffer Enable	1	1	PLL Buffer Enable. Used when using an internal VCO.
[4]	R/W	LO1 Output Buffer Enable	1	0	Enables LO1 (LO_P & LO_N pins) output buffer.
[5]	R/W	LO2 Output Buffer Enable	1	1	Enables the LO2 (LO2_N & LO2_P pins) output buffer
[6]	R/W	External Input Enable	1	0	Enables External VCO input
[7]	R/W	Pre Lock Mute Enable	1	1	Mute both output buffers until the PLL is locked
[8]	R/W	LO1 Output Single-Ended Enable	1	1	Enables Single-Ended output mode for LO output 1- Single-ended mode, LO_N pin is enabled, and LO_P pin is disabled 0- Differential mode, both LO_N and LO_P pins enabled Please note that single-ended output is only available on LO_N pin.
[9]	R/W	LO2 Output Single-Ended Enable	1	0	Enables Single-Ended output mode for LO2 output 1- Single-ended mode, LO2_N pin is enabled, and LO2_P pin is disabled 0- Differential mode, both LO2_N and LO2_P pins enabled Please note that single-ended output is only available on LO2_N pin.
[10]	R/W	Reserved	1	0	Reserved
[11]	R/W	Charge Pump Output Select	1	0	Connects CP to CP1 or CP2 output. 0: CP1 1: CP2
[23:12]	R/W	Reserved	12	0	Reserved

2.24 Reg 18h Bias Register Default 54C1 h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[18:0]	R/W	Reserved	19	21697d 54C1h	Reserved
[19]	R/W	External Input buffer BIAS bit0	1	0	External Input buffer BIAS bit0
[20]	R/W	External Input buffer BIAS bit1	1	0	External Input buffer BIAS bit1
[23:21]	R/W	Reserved	3	0	Reserved

2.25 Reg 19h Cals Register Default AAA h

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[23:0]	R/W	Reserved	2	2730d AAAh	Reserved. Program to AB2h.

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2.26 Reg 1Ah Seed Register Default B29D0Bh

BIT	TYPE	NAME	Width	Default	DESCRIPTION
[23:0]	R/W	Delta Sigma Modulator Seed	24	11705611d B29D0Bh	Used to program output phase relative to the reference frequency. (Exact Frequency Mode required). When not using Exact Frequency Mode and Auto seed Enable Reg06h[8] =1, Reg1Ah sets the start phase of output signal. If AutoSeed disable Reg06h[8] =0, Reg1Ah is the start phase of the signal after every frequency changel. (LO Phase = 2π x Reg1Ah/(2^{24})

2.27 Reg 21h Programmable Harmonic LPF Register
Chip ID = 6h, Regaddress = 01h, (Reg01h) (Write Only)[1]

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[15:0]	W	Harmonic LPF Band select	16	15d Fh	Low Pass Filter 3 dB bandwidth setting on the output of LO pins (LO_N & LO_P pins) 0: 970 MHz 1: 1000 MHz 2: 1030 MHz 3: 1055 MHzl 4: 1085 MHz 5: 1120 MHz 6: 1155 MHz 7: 1195 MHz 8: 2335 MHz 9: 2430 MHz 10: 2530 MHz 11: 2655 MHz 12: 2770 MHz 13: 2940 MHz 14: 3145 MHz 15: 3400 MHz
[23:16]	W	Reserved	8		Reserved A write of C1h is required every time bandwidth setting in Reg 21h [15:0] is changed.

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3.0 Application Information

3.1 Principle of Operation

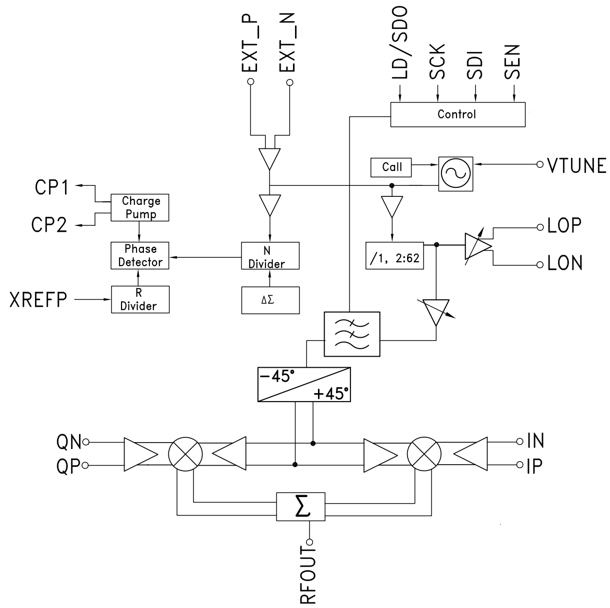

Figure 43. The HMC1197LP7FE Simplified Block Diagram

The HMC1197LP7FE is a low-noise, high-linearity, Direct Quadrature Modulator with Fractional-N PLL&VCO RFIC designed for directly converting complex modulated baseband signals from zero IF or low IF to RF transmission levels from 100 MHz to 4 GHz. The HMC1197LP7FE's excellent noise and linearity performance makes it suitable for a wide range of transmission standards, including single and multicarrier CDMA, UMTS, CDMA2000, GSM/EDGE, W-CDMA, TD-SCDMA, and WiMAX/LTE applications.

As shown in the simplified block diagram (Figure 43) the HMC1197LP7FE offers an easy-to-use, complete direct conversion solution in a highly compact 7 x 7 mm plastic package thereby reducing cost, area, and power consumption.

The HMC1197LP7FE modulator consists of the following functional blocks:

1. PLL & VCO "1.0 Theory of Operation"

2. I/Q modulator: I and Q input differential voltage-to-current converters, I and Q upconverting mixers and the differential-to-single-ended converter, high Accuracy LO quadrature phase splitter and LO limiting amplifiers

3. Harmonic Low Pass Filter

3.2 I/Q Modulator

The differential baseband inputs (QP, QN, IP, and IN) present a high impedance. The DC common-mode voltage at the baseband inputs sets the currents in the I and Q double-balanced mixers. The nominal baseband input DC common-mode voltage used in the characterization of the HMC1197LP7FE is 0.45V, which should be externally applied. The baseband input DC common-mode voltage can be varied between 0.4V and 0.5V to optimize overall modulator performance. It is not recommended to leave the baseband inputs floating which generates excessive current flow that may cause damage to the IC. The baseband inputs should be pulled down to GND in shutdown mode. The nominal baseband input AC Voltage used in the characterization of the HMC1197LP7FE is 1.3Vpp differential. The baseband input AC voltage can be varied to optimize overall modulator performance.

It is recommended to drive the baseband inputs differentially to reduce even-order distortion products and also use reconstruction filters at the baseband inputs to avoid aliasing

I/Q modulator includes a LO quadrature phase splitter that generates two carrier signals in quadrature followed by LO limiting amplifiers which are used to drive the I and Q mixers with saturated signal levels. Therefore, the LO path is immune to large variations in the LO input signal level and the modulator performance does not vary much with LO input power.

After upconversion, the outputs of the I and Q mixers are summed together differentially and converted to single- ended RF output. The single-ended RF output port is internally matched to 50 Ohms and does not require any external matching components. Only a standard DC-blocking capacitor is required at this interface.

3.3 Harmonic Low Pass Filter

High LO harmonic content causes amplitude and phase mismatches and ultimately performance degradation in modulator sideband rejection.

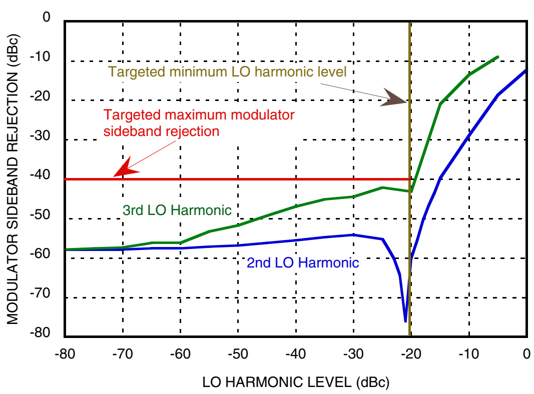

Figure 44. Typical impact of 2nd and 3rd LO harmonic on sideband rejection.

As shown in Figure 44, in a typical modulator with 1xLO input both the 2nd and 3rd LO harmonics affect the modulator sideband rejection performance at levels > -20 dBc relative to the LO signal power. It also shows that the 3rd LO harmonic has greater impact on modulator sideband rejection performance than the 2nd, and that there is little effect of the 2nd LO harmonic on modulator sideband rejection once the 2nd LO harmonic is below -20 dBc levels, relative to the LO signal level.

Figure 45 shows the typical insertion loss of the low pass filter.

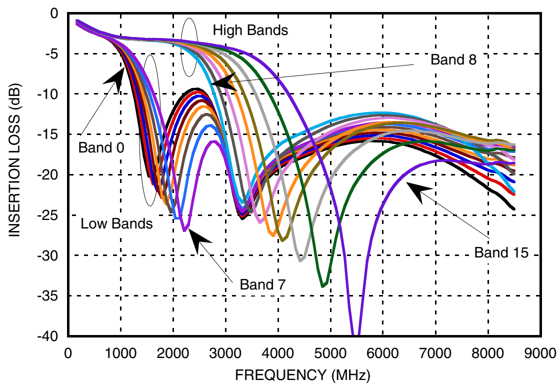

Figure 45. Insertion loss of the low pass filter.

LO harmonic filter's 16 user programmable bands enable the user to optimally attenuate 2nd and/or 3rd LO harmonics in order to maximize sideband rejection performance.

Table 15. The frequency band selection for optimal 3rd harmonic attenuation.

Frequency (MHz)	**≤500**	**600**	**700**	**800**	**900/1000**	**1100**	**1200**	**1300**	**1400**	**1500**	**1600**	**1700**	**≥1800**
Filter Bank Selection	0	1	4	6	7	8	9	11	12	13	13	14	15

Table 16. The frequency band selection for optimal 2nd harmonic attenuation.

Frequency (MHz)	**≤700**	**800/900**	**1000**	**1100**	**1200/1300/1400**	**1500/1600/1700**	**1800**	**1900**	**2000**	**2100**	**2200/2300**	**2400/2500/2600**	**≥2700**
Filter Bank Selection	0	1	4	5	7	8	9	10	11	12	13	14	15

Uncalibrated sideband rejection can be further improved by empirically selecting the filter bank that provides the highest rejection for a given frequency . See Table 15, Table 16 and Figure 46

Table 17. Empirical filter band selection.

Frequency (MHz)	**≤500**	**600**	**700**	**800**	**900**	**1000/1100**	**1200**	**1300/1400/1500**	**1600**	**1700/1800**	**1900/2000**	**>2000**
Filter Bank Selection	0	1	5	7	8	0	7	8	9	10	11	15

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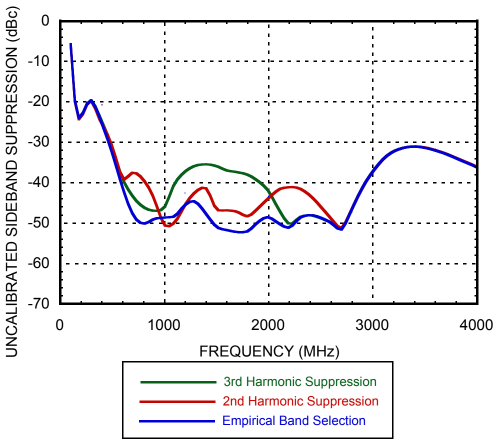

Figure 46.Sideband suppression vs. frequency for different filter band selections.

The filter bank selection process for optimal sideband rejection performance also depends on the LO power level at the output of the PLL/VCO. LO power in this example set to maximum power level.

3.4 Carrier Feedthrough Calibration

Carrier feedthrough is related to the DC offsets at the differential baseband inputs of the modulator. If exactly the same DC common-mode voltage is applied to each of the baseband inputs, and there were no DC offsets at the differential baseband inputs, the LO leakage at the RF output would be perfectly suppressed.

By adding small DC offset voltages at the differential baseband inputs, the carrier feedthrough can be optimized for a specific frequency band and LO power level. The carrier feedthrough can not be calibrated by the DC common-mode level at the I and Q baseband inputs. DC offsets at the differential I and Q baseband inputs should be iteratively adjusted until a minimum carrier feedthrough level is obtained. Externally available offset voltage step resolution and the modulator's noise floor limit the minimum achievable calibrated carrier feedthrough level. The typical offset voltages for optimization are less than 15mV. Figure 47 illustrates the typical calibrated carrier feedthrough performance of the HMC1197LP7FE. In this characterization of the HMC1197LP7FE, carrier feedthrough was calibrated with 500MHz LO frequency steps at 25C and external offset voltage settings were held constant during tests over temperature.

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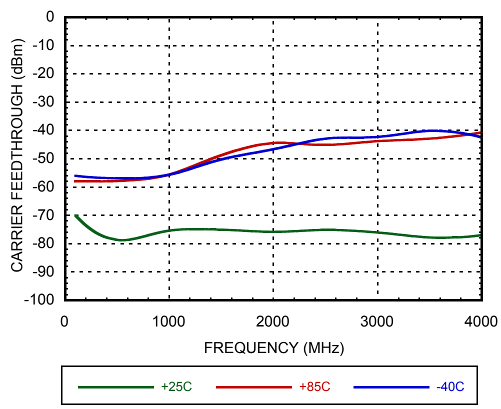

Figure 47. The HMC1197LP7FE Calibrated Carrier Feedthrough

3.5 Sideband Suppression Calibration

Sideband suppression is related to relative gain and relative phase offsets between the I-channel and Q-channel. The amplitude and phase difference between the I and Q inputs can be adjusted in order to optimize the sideband suppression for a specific frequency band and LO power level. The amplitude and phase offsets at the I and Q inputs should be iteratively adjusted until a minimum sideband suppression level is obtained. The externally available amplitude and phase steps and the modulator's noise floor limit the minimum achievable calibrated sideband suppression level. Figure 48 illustrates the typical calibrated sideband suppression performance of the HMC1197LP7FE. In this characterization of the HMC1197LP7FE, sideband suppression was calibrated at every 500MHz LO frequency steps at 25C and external amplitude and phase offset settings were held constant during tests over temperature.

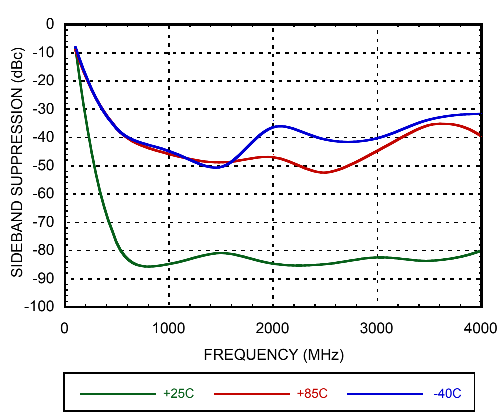

Figure 48.The HMC1197LP7FE Calibrated Sideband Suppression

3.6 Linearity Optimization

Output IP3 (OIP3) of the HMC1197LP7FE depends on the DC common-mode level at the I and Q baseband inputs. The DC common-mode level at the I and Q baseband inputs can be adjusted in order to optimize the OIP3 for a specific frequency band. Figure 49 illustrates the typical relationship between OIP3 and the DC common-mode level at the I and Q baseband inputs for different LO frequencies. As shown in Figure 49, OIP3 of the HMC1197LP7FE can be optimized up to 35dBm.

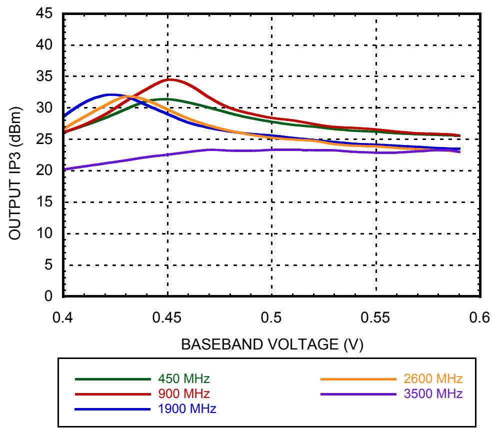

Figure 49.The HMC1197LP7FE Linearity Optimization

3.7 GSM/EDGE Operation

The HMC1197LP7FE is suitable for GSM/EDGE applications. The EVM performance of the HMC1197LP7FE in a GSM/EDGE environment is shown in Figure 50

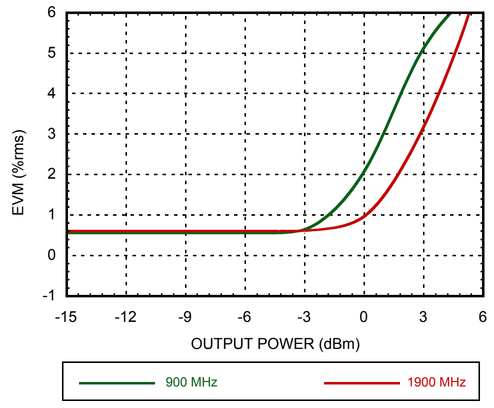

Figure 50.The HMC1197LP7FE EVM vs. Output Power @ GSM/EDGE(8-PSK)

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3.8 W-CDMA Operation

The HMC1197LP7FE is suitable for W-CDMA operation. Figure 51 shows the adjacent and alternate channel power ratios for the HMC1197LP7FE at an LO frequency of 2140 MHz. The HMC1197LP7FE is able to deliver about –72 dBc ACPR and –77 dBc AltCPR at an output power of –10 dBm. ACPR and AltCPR performances of the HMC1197LP7FE can be improved by adjusting the DC common-mode level on the I and Q baseband inputs.

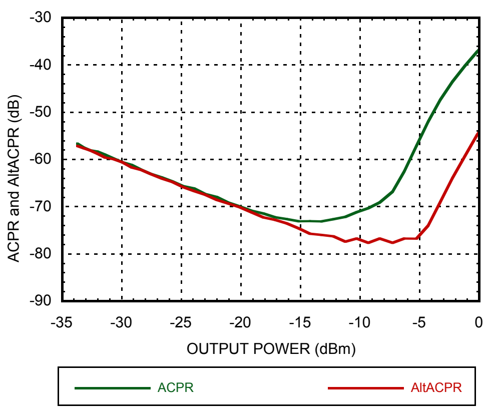

Figure 51.The HMC1197LP7FE ACPR and AltCPR vs. Output Power @ WCDMA

3.9 LTE Operation

The HMC1197LP7FE is suitable for LTE applications. The EVM performance of the HMC1197LP7FE in a LTE environment is shown in Figure 52

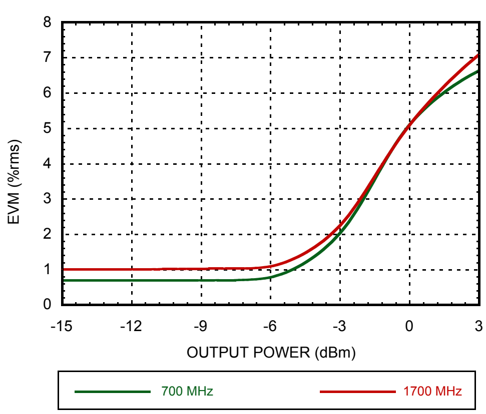

Figure 52.The HMC1197LP7FE EVM vs. Output Power @ LTE Downlink 25RB QPSK

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3.10 Using an External VCO

In order to configure HMC1197LP7FE to use with an external VCO, Register 17 needs to be configured to disable the on chip VCO and VCO to PLL path. Enable External Buffer, second CP link and External I/O switch. To make these changes Reg 17 [0:11] should be configured as 3157d.

HMC1197LP7FE is configured as PLL alone used with External VCO HMC384LP4E. Loop Filter components are used as in Figure 53

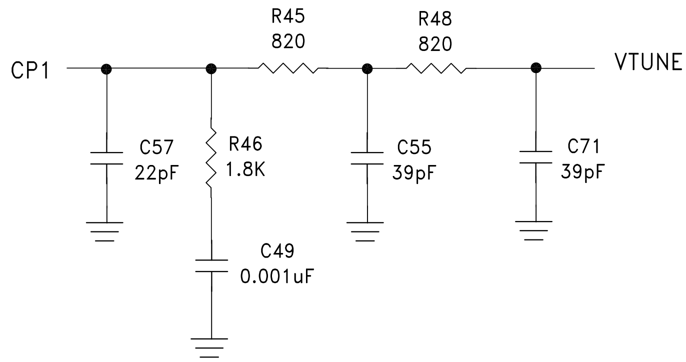

Figure 53.Loop filter components for HMC1197LP7FE is configured as PLL alone used with external VCO HMC384LP4E

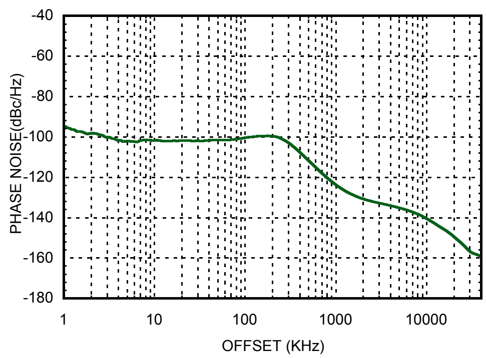

Figure 54.Closed Loop Phase Noise with External HMC384LP4E VCO @ 2200 MHz.

For detailed theory of operation of PLL/VCO, please refer to the "PLLs with Integrated VCOs - RF VCOs Operating Guide"

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