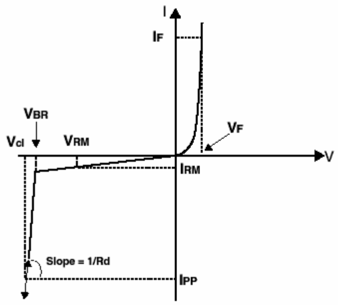
1 Characteristics

Table 1. Absolute ratings

Symbol	Parameter			Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge		8 15	kV
I_{PP}	Peak pulse current	I/O to GND Pulse waveform = 8/20 μs	SOT-666	5	A
			Flip-Chip	7	
P_{PP}	Peak pulse power		SOT-666	90	W
			Flip-Chip	120	
T_{stg}	Storage temperature range			-55 to +150	°C
T_j	Maximum junction temperature			125	°C
T_L	Lead solder temperature (10 seconds duration)			260	°C

Table 2. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameter	
V_{RM}	Reverse stand-off voltage	
I_{RM}	Leakage current	
V_{BR}	Breakdown voltage	
V_F	Forward voltage	
V_{CL}	Clamping voltage	
I_{PP}	Peak pulse current	

Symbol	Parameter	Test Conditions		Value			Unit
				Min	Typ	Max	
I_{RM}	Leakage current	V_{RM} = 5 V				0.5	μA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1 mA		6			V
V_F	Forward voltage	I_F = 10 mA				1	V
$C_{i/o\text{-}GND}$	Capacitance between I/O and GND	$V_{I/O}$ = 0 V, F = 1 MHz, V_{OSC} = 30 mV	SOT-666		2	2.5	pF
			Flip-Chip		2.5	3	
		$V_{I/O}$ = 1.65 V, V_{CC} = 4.3 V, F = 1 MHz, V_{OSC} = 400 mV	SOT-666		1.5	1.8	
			Flip-Chip		1.8	2.0	
$C_{i/o\text{-}i/o}$	Capacitance between I/O	$V_{I/O}$ = 0 V, F = 1 MHz, V_{OSC} = 30 mV	SOT-666		1.0	1.25	
			Flip-Chip		1.25	1.5	
		$V_{I/O}$ = 1.65 V, V_{CC} = 4.3 V, F = 1 MHz, V_{OSC} = 400 mV	SOT-666		0.75	0.9	
			Flip-Chip		0.9	1.20	
$\Delta C_{i/o\text{-}GND}$		$V_{I/O}$ = 0 V, F = 1 MHz, V_{OSC} = 30 mV				0.06	
$\Delta C_{i/o\text{-}i/o}$		$V_{I/O}$ = 0 V, F = 1 MHz, V_{OSC} = 30 mV				0.05	

Figure 1. Relative variation of leakage current versus junction temperature - SOT-666 (typical values)

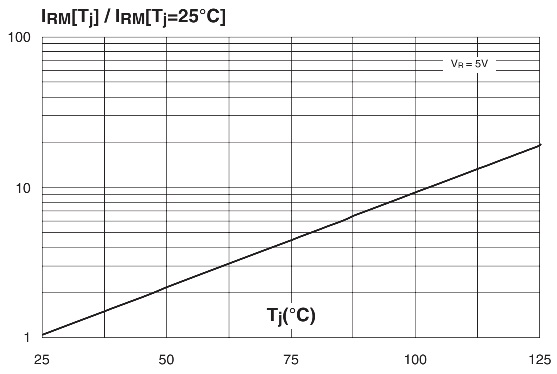


Figure 2. Relative variation of leakage current versus junction temperature Flip-Chip (typical values)

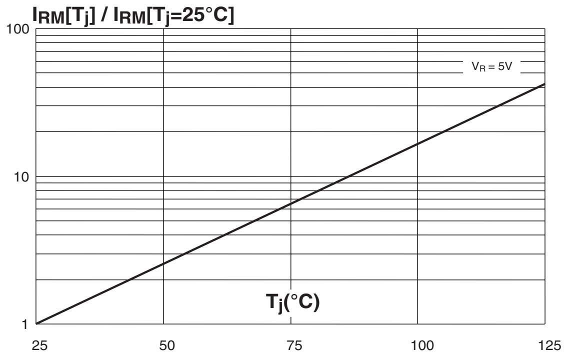


Figure 3. Remaining voltage after DSILC6-4P6 during ESD 15 kV positive surge (air discharge)

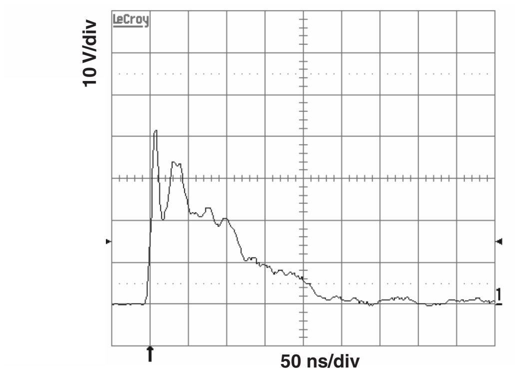


Figure 4. Remaining voltage after DSILC6-4F2 during ESD 15 kV positive surge (air discharge)

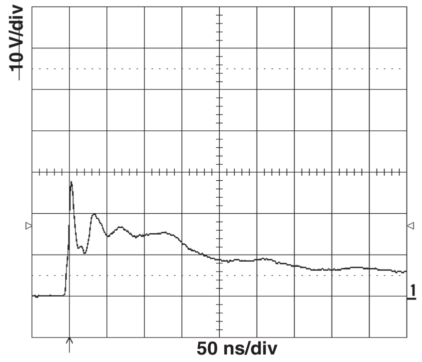


Figure 5. Remaining voltage after DSILC6-4P6 during ESD 15 kV negative surge (air discharge)

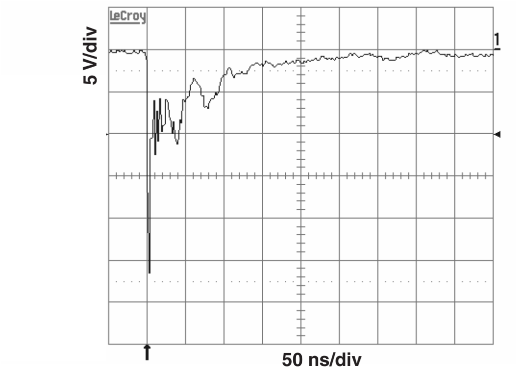


Figure 6. Remaining voltage after DSILC6-4F2 during ESD 15 kV negative surge (air discharge)

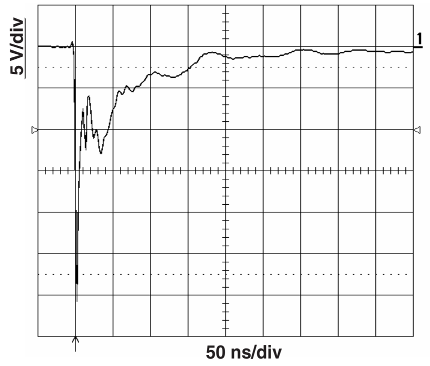


Figure 7. Frequency responses of all lines DSILC6-4P6

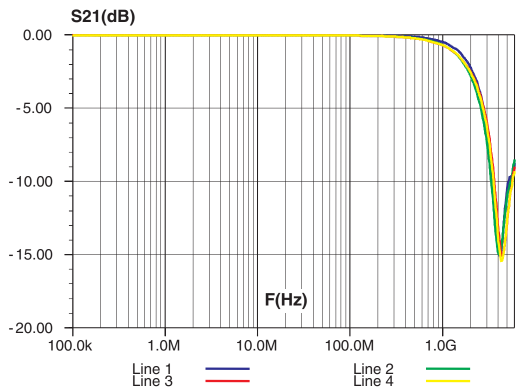


Figure 8. Frequency response of all lines DSILC6-4F2

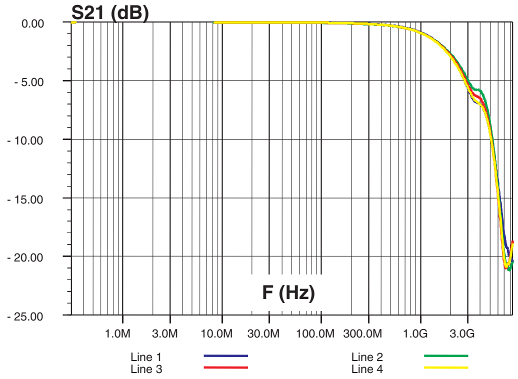


Figure 9. Crosstalk results for lines 1/2 and 1/3 DSILC6-4P6

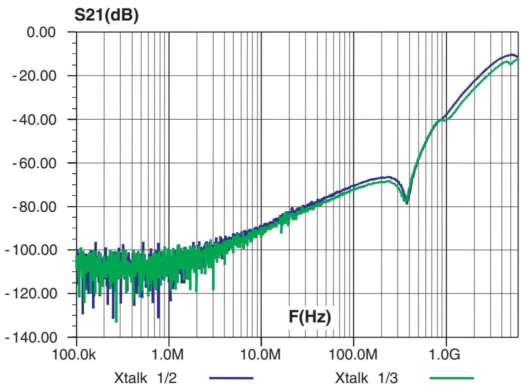
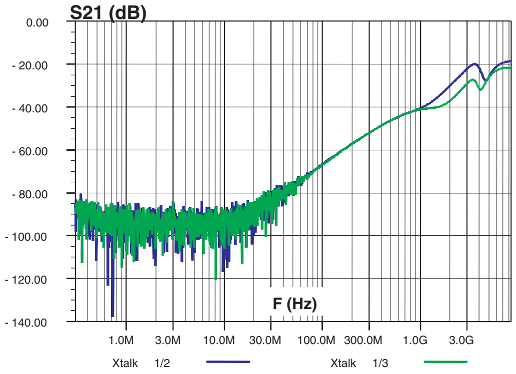
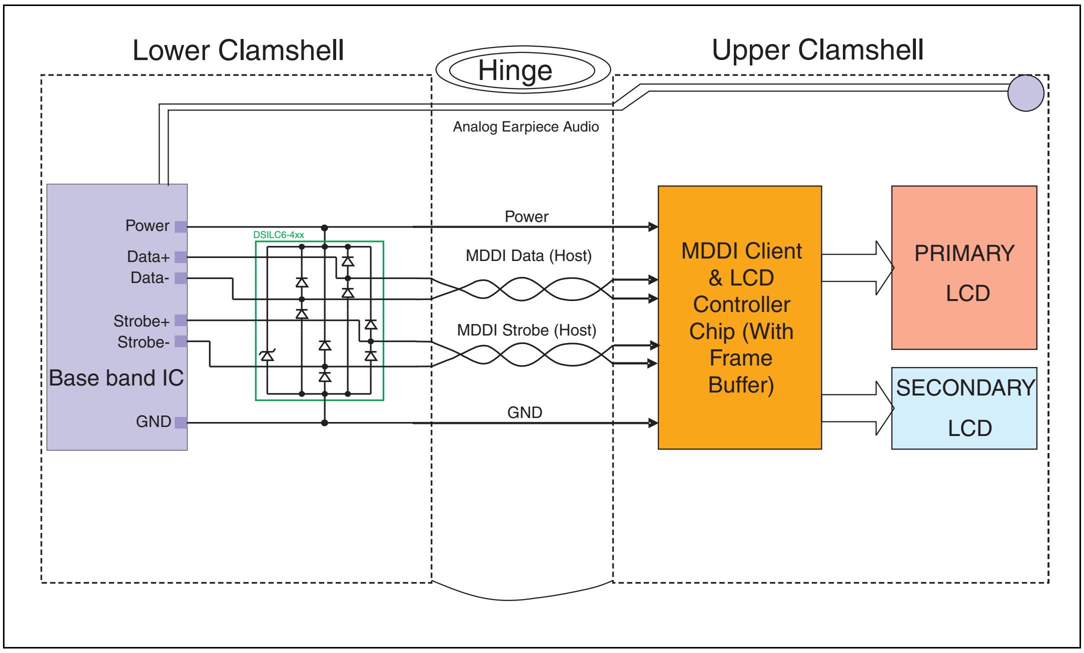


Figure 10. Crosstalk results for lines 1/2 and 1/3 DSILC6-4F2

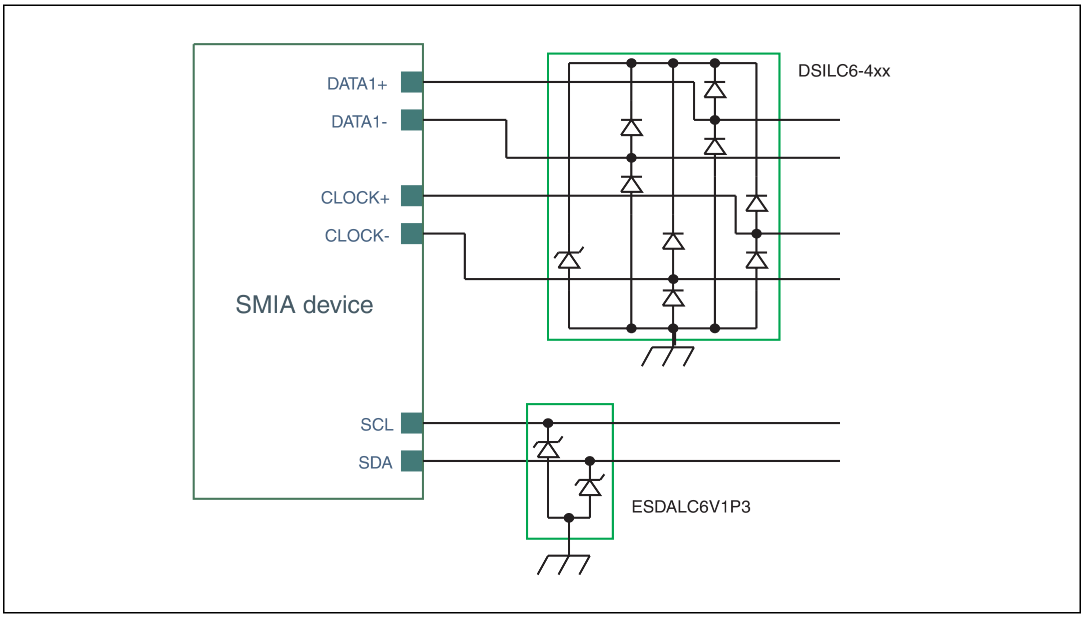


2 Application examples

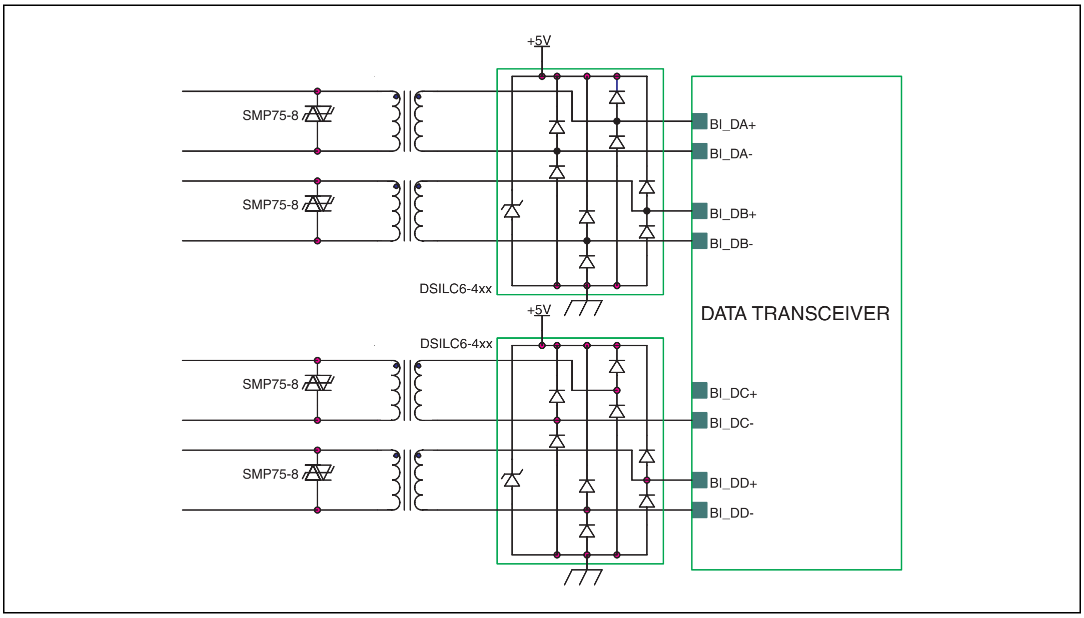
2.1 MDDI



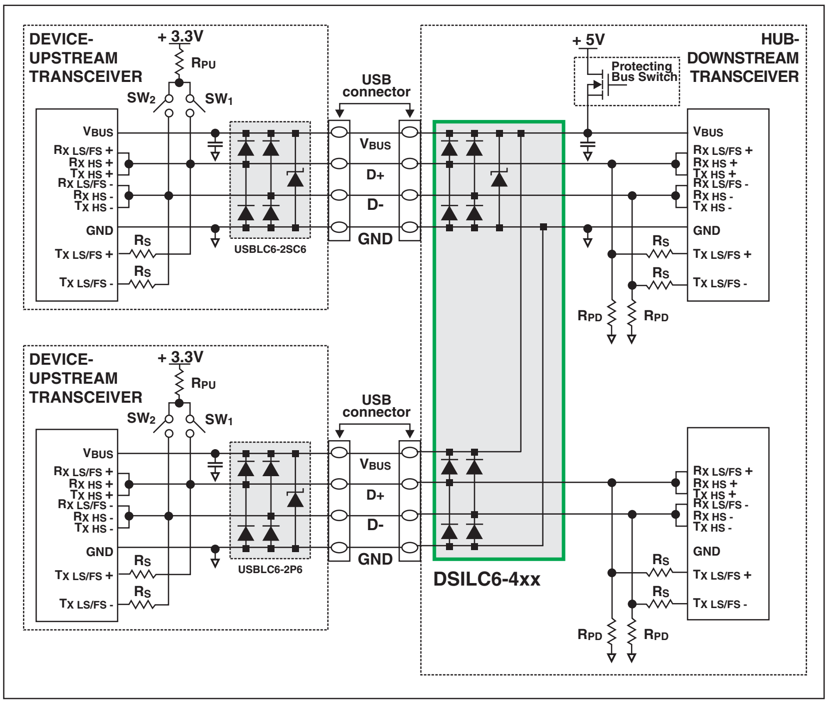
2.2 SMIA



2.3 Ethernet 1 Gb

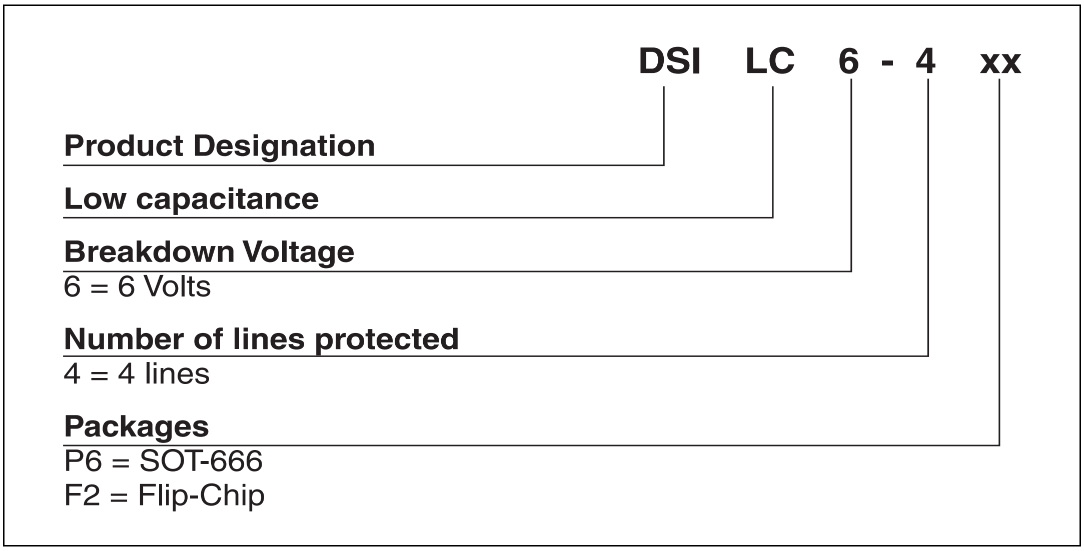


2.4 USB 2.0



Mode	SW1	SW2
Low Speed LS	Open	Closed
Full Speed FS	Closed	Open
High Speed HS	Closed then open	Open

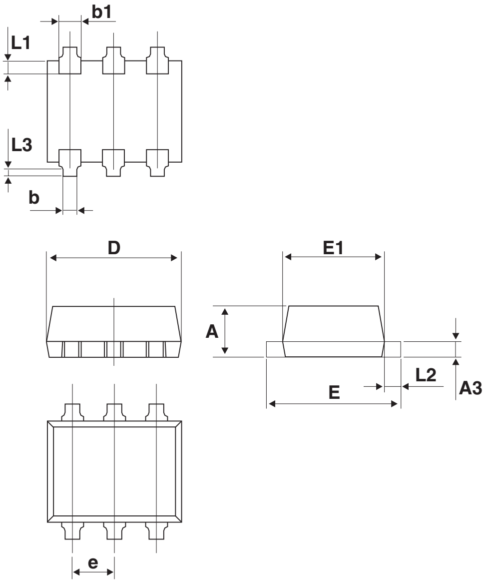
3 Ordering information scheme



4 Package information

- Epoxy meets UL94, V0

Table 3. SOT-666 Dimensions

	Ref.	Dimensions					
		Millimeters			Inches		
		Min.	Typ.	Max.	Min.	Typ.	Max.
	A	0.45		0.60	0.018		0.024
	A3	0.08		0.18	0.003		0.007
	b	0.17		0.34	0.007		0.013
	b1	0.19	0.27	0.34	0.007	0.011	0.013
	D	1.50		1.70	0.059		0.067
	E	1.50		1.70	0.059		0.067
	E1	1.10		1.30	0.043		0.051
	e		0.50			0.020	
	L1		0.19			0.007	
	L2	0.10		0.30	0.004		0.012
	L3		0.10			0.004	

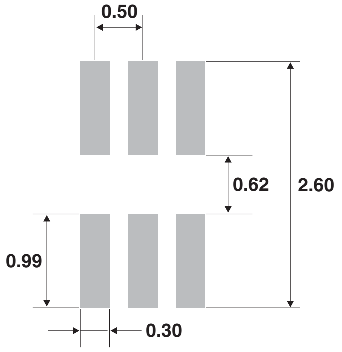


Figure 11. SOT-666 footprint

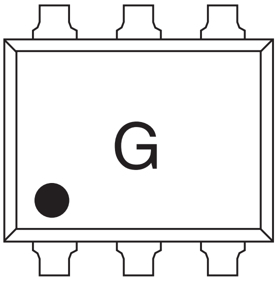


Figure 12. SOT-666 marking

Figure 13. Flip-Chip Dimensions

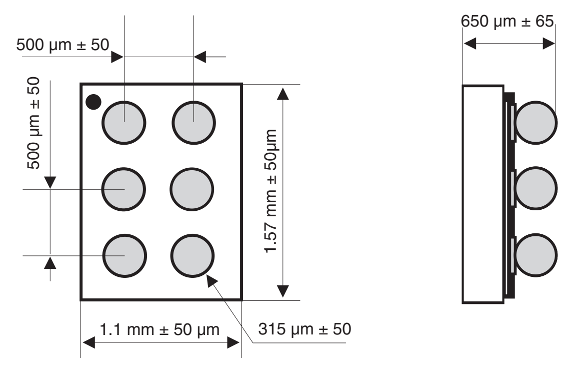


Figure 14. Flip-Chip footprint

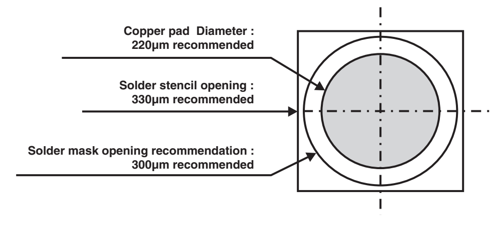


Figure 15. Flip-Chip marking

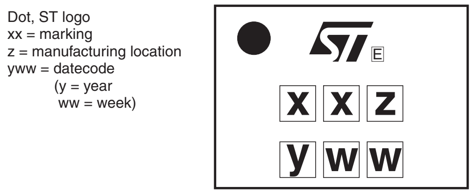
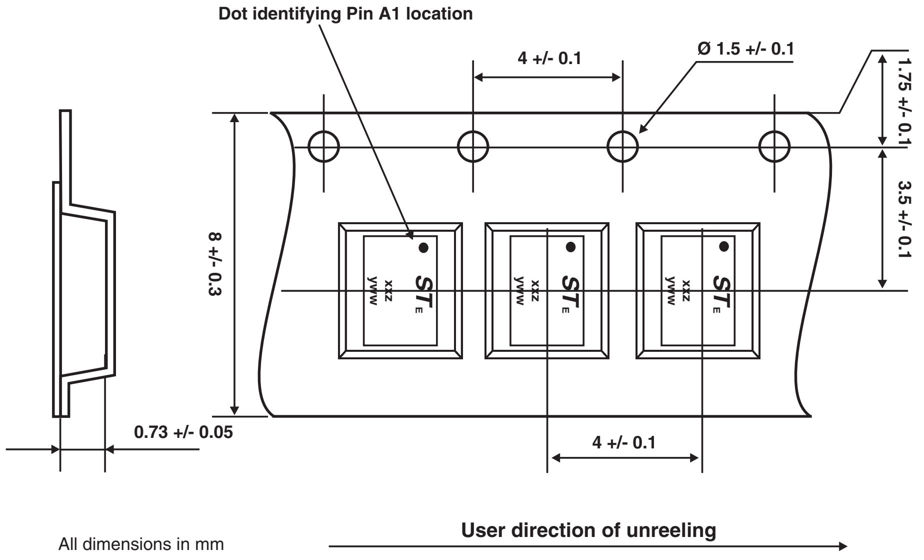


Figure 16. Flip-Chip tape and reel specifications



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
DSILC6-4P6	G	SOT-666	2.9 mg	3000	Tape and reel
DSILC6-4F2	EI	Flip-Chip	2.22 mg	5000	Tape and reel

6 Revision history

Date	Revision	Description of Changes
10-Aug-2006	1	Initial release.
04-Jan-2007	2	Added Flip-Chip package. Added applications examples for SMIA, Ethernet 1 Gb, and USB. Updated Tj max to 150. Added V_{RM} line in Table 2. Modified MDDI example figure.
28-May-2007	3	Modified Functional diagram on page 1 to show Top side view instead of Bump side view of DSILC64F2. Removed V_{RM} line in Table 2. Added characteristic curves specific to each package for ESD, Frequency response and Crosstalk

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