

Vishay Siliconix

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ -0.3 to +6 V

IN, COM, NC, NO^a -0.3 to (V+ + 0.3 V)

Continuous Current (NO, NC, COM) ± 300 mA

Peak Current ± 500 mA

(Pulsed at 1 ms, 10% duty cycle)

Storage Temperature (D Suffix) -65 to 150°C

ESD per Method 3015.7 >2 kV

Power Dissipation (Packages)^bMSOP-10^c 320 mW

Notes:

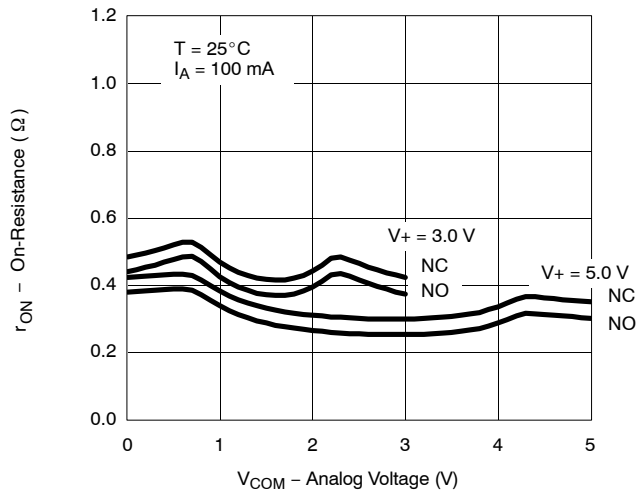
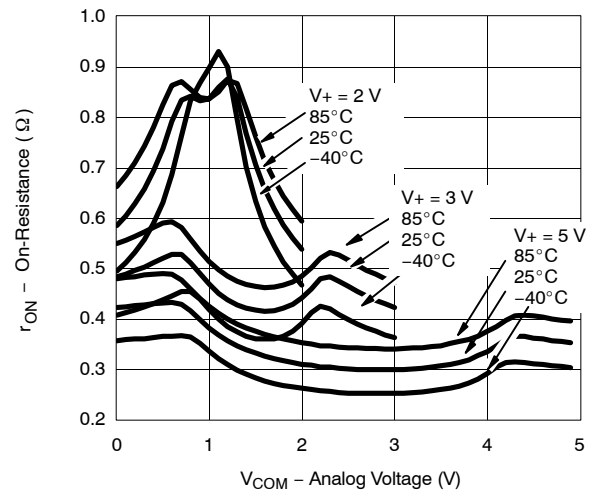
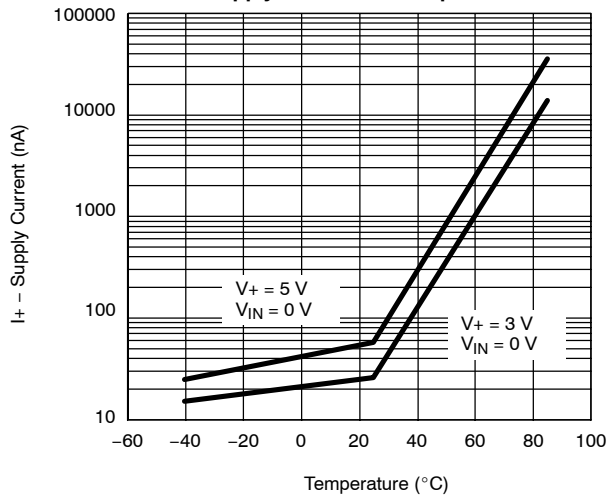
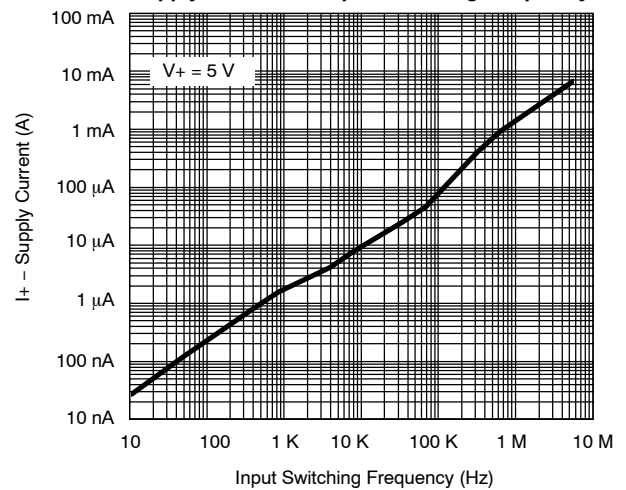
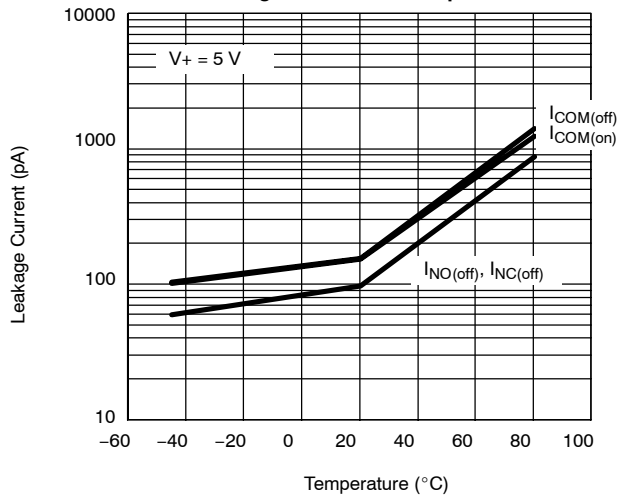
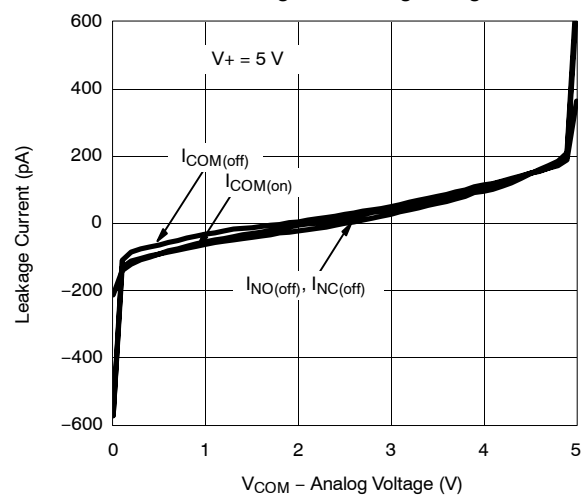
- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 4.0 mW/°C above 70°C

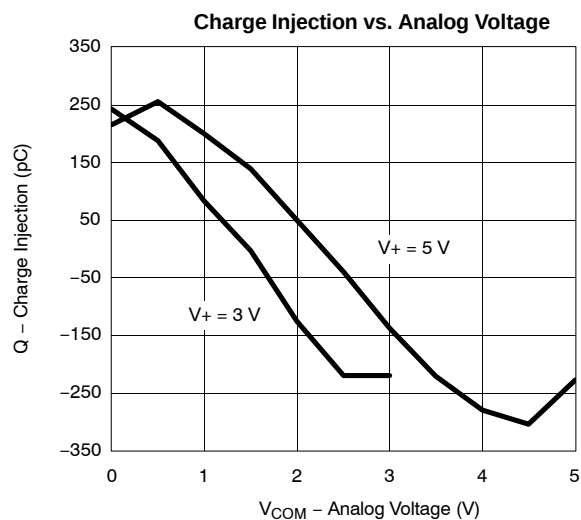
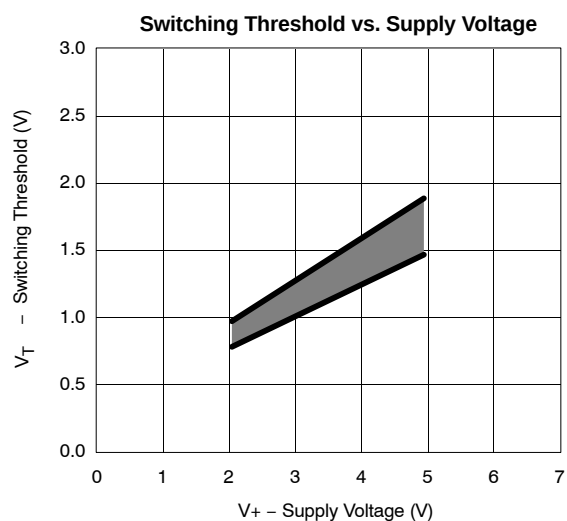
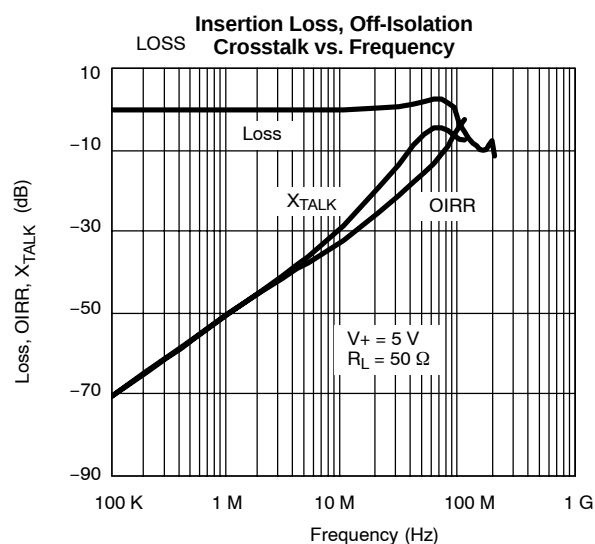
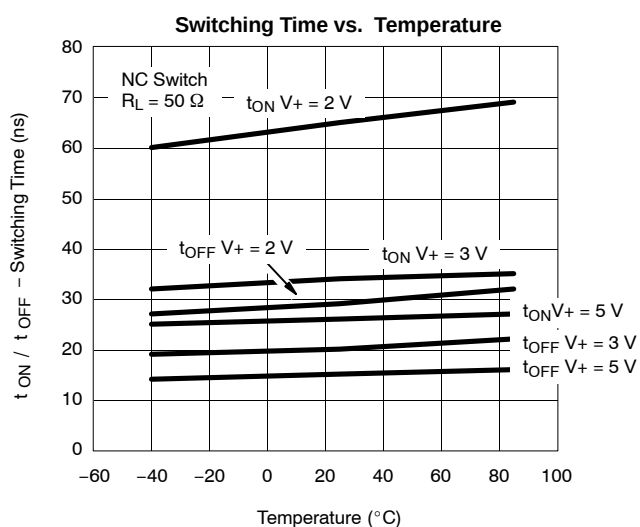
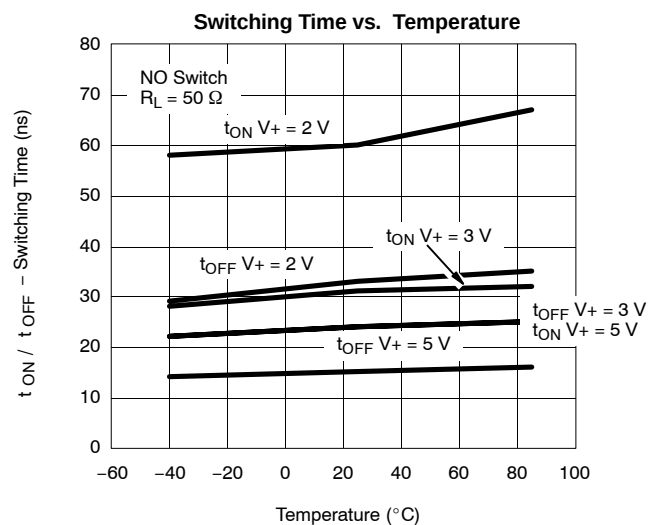
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

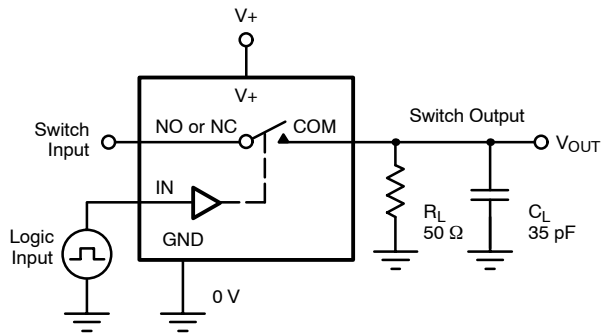
SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10%, VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits −40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VNO, VNC, VCOM		Full	0		V+	V
On-Resistance	rON	V+ = 2.7 V, VCOM = 0.6/1.5 V INO, INC = 100 mA	Room Full		0.50	0.75 0.8	Ω
rON Flatness ^d	rON Flatness		Room		0.12	0.2	
On-Resistance Match Between Channels ^d	ΔrDS(on)		Room			0.05	
Switch Off Leakage Current	INO(off), INC(off)	V+ = 3.3 V, VNO, VNC = 0.3 V/3 V VCOM = 3 V/0.3 V	Room Full	−1 −10		1 10	nA
	ICOM(off)		Room Full	−1 −10		1 10	
Channel-On Leakage Current	ICOM(on)	V+ = 3.3 V, VNO, VNC = VCOM = 0.3 V/3 V	Room Full	−1 −10		1 10	
Digital Control							
Input High Voltage ^d	VINH		Full	1.6			V
Input Low Voltage	VINL		Full			0.4	
Input Capacitance	Cin		Full		9		pF
Input Current	IINL or IINH	VIN = 0 or V+	Full	1		1	μA
Dynamic Characteristics							
Turn-On Time	tON	VNO or VNC = 2.0 V, RL = 50 Ω, CL = 35 pF	Room Full		34	58 59	ns
Turn-Off Time	tOFF		Room Full		24	49 50	
Break-Before-Make Time	td	VNO or VNC = 2.0 V, RL = 50 Ω, CL = 35 pF	Full	2	10		
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 1.5 V, RGEN = 0 Ω	Room		4		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 100 KHz	Room		−71		dB
Crosstalk ^d	XTALK		Room		−71		
NO, NC Off Capacitance ^d	CNO(off)	VIN = 0 or V+, f = 1 MHz	Room		117		pF
	CNC(off)		Room		115		
Channel-On Capacitance ^d	CNO(on)		Room		367		
	CNC(on)		Room		368		
Power Supply							
Power Supply Range	V+			1.8		5.5	V
Power Supply Current	I+	VIN = 0 or V+	Full		0.01	1.0	μA

Notes:

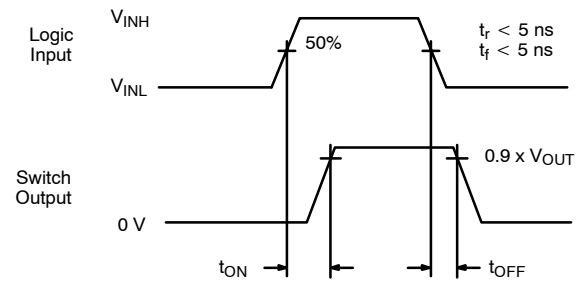
- Room = 25°C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guarantee by design, nor subjected to production test.
- VIN = input voltage to perform proper function.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)** **r_{ON} vs. V_{COM} and Supply Voltage** **r_{ON} vs. Analog Voltage and Temperature (NC1)****Supply Current vs. Temperature****Supply Current vs. Input Switching Frequency****Leakage Current vs. Temperature****Leakage vs. Analog Voltage**

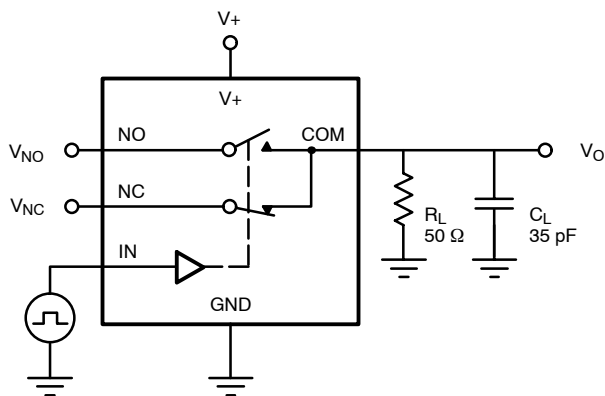
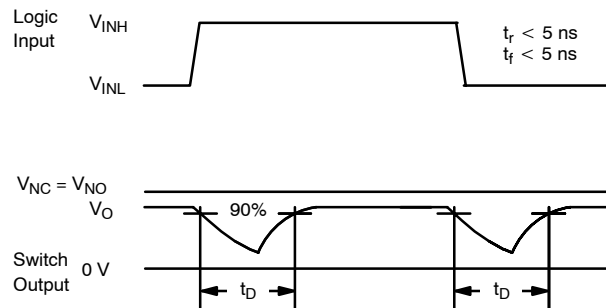
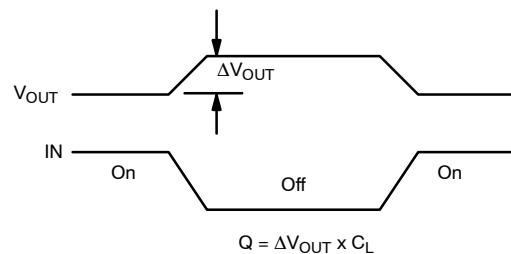
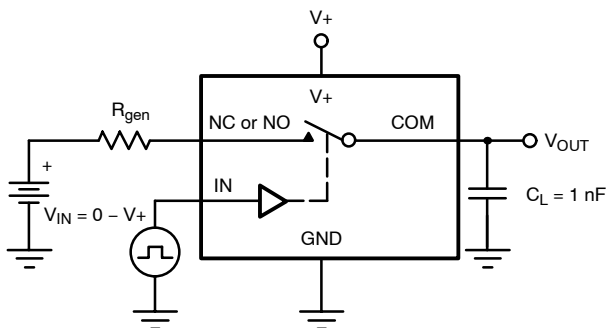
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)


TEST CIRCUITS

 C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time

 C_L (includes fixture and stray capacitance)

FIGURE 3. Break-Before-Make Interval


IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection

TEST CIRCUITS

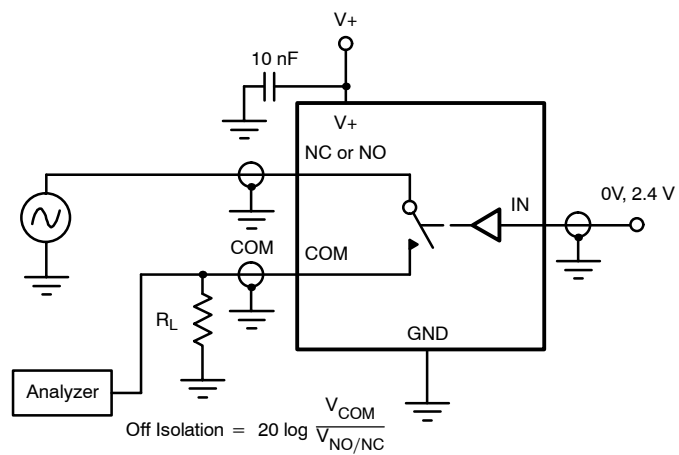


FIGURE 4. Off-Isolation

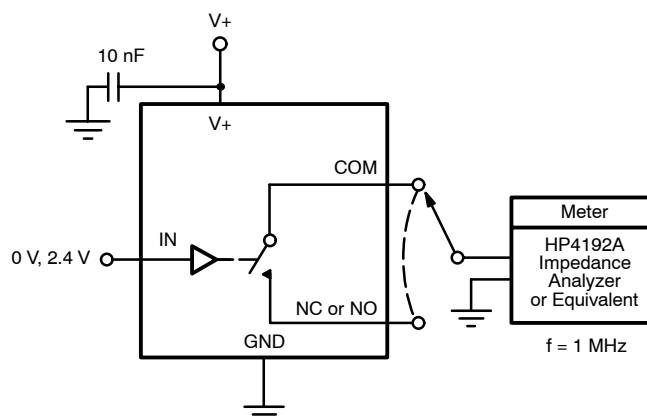


FIGURE 5. Channel Off/On Capacitance



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