Pin Configuration

Figure 1. 68-Pin PLCC (Top View)

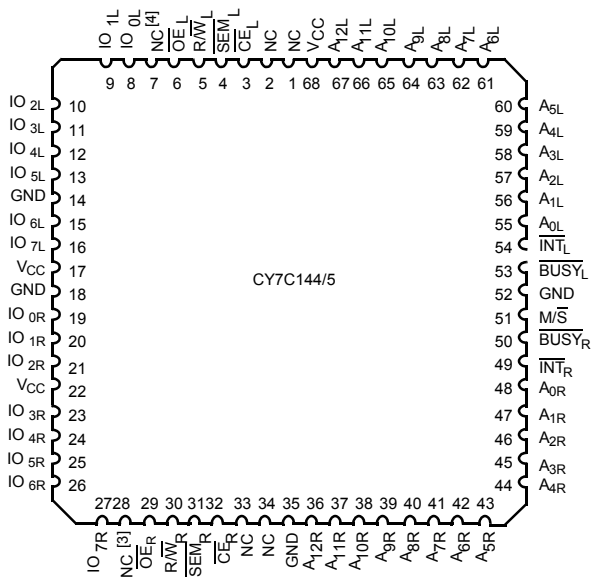


Figure 2. 64-Pin TQFP (Top View)

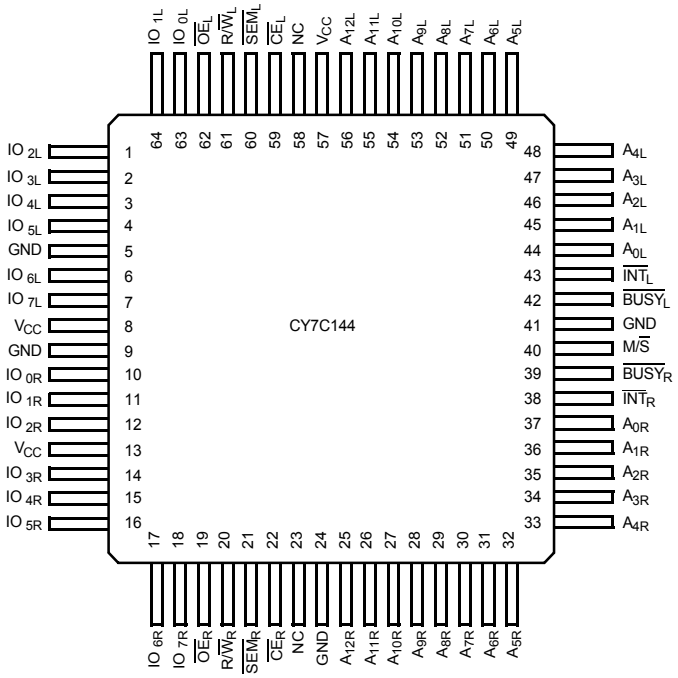
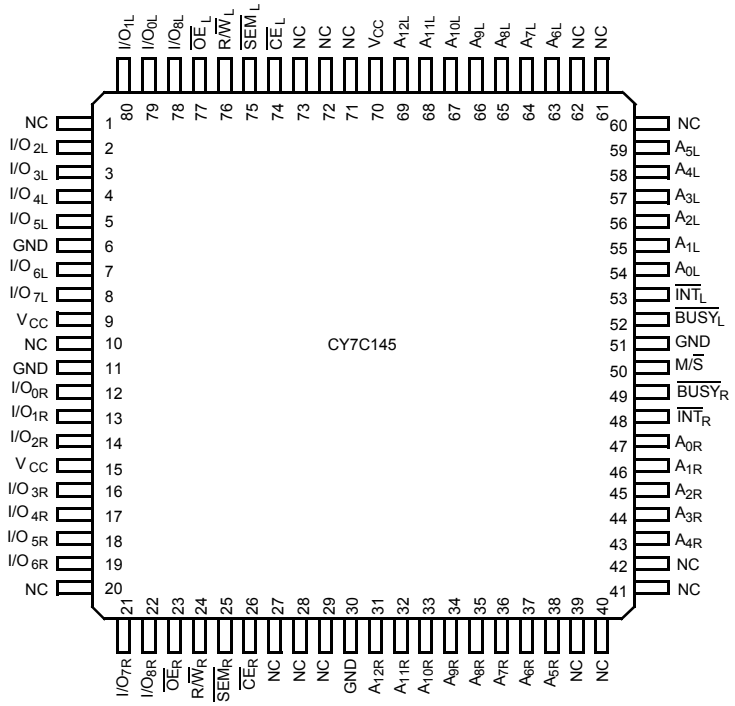


Figure 3. 80-Pin TQFP (Top View)



Notes:
3. I/O_{8R} on the CY7C145.
4. I/O_{8L} on the CY7C145.

Table 1. Selection Guide

Description	7C144-15 7C145-15	7C144-25 7C145-25	7C144-35 7C145-35	7C144-55 7C145-55	Unit
Maximum Access Time	15	25	35	55	ns
Maximum Operating Current	220	180	160	160	mA
Maximum Standby Current for I_{SB1}	60	40	30	30	mA

Table 2. Pin Definitions

Left Port	Right Port	Description
$I/O_{0L–7L(8L)}$	$I/O_{0R–7R(8R)}$	Data bus Input/Output
$A_{0L–12L}$	$A_{0R–12R}$	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 1FFE and is cleared when left port reads location 1FFE. $\overline{INT}_R$ is set when left port writes location 1FFF and is cleared when right port reads location 1FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Architecture

The CY7C144/5 consists of a an array of 8K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes or reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be used for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7C144/5 can function as a Master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7C144/5 has an automatic power down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Figure 8 on page 11) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in Table 3.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7C144/5 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports.When the left port writes to location 1FFF, the right port's interrupt flag ($\overline{INT}_R$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT}_L$) is accomplished when the right port writes to location 1FFE. This flag is cleared when the left port reads location 1FFE. The message at 1FFF or 1FFE is user-defined. See Table 4 for input requirements for $\overline{INT}$. $\overline{INT}_R$ and $\overline{INT}_L$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C144/5 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic determines which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This enables the device to interface to a master device with no external components.Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation.When presented a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C144/5 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports.The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available t_{SWRD} + t_{DOE} after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore.When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). $A_{0–2}$ represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access.When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. Table 5 shows sample semaphore operations.

When reading a semaphore, all eight/nine data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power up. All Semaphores on both sides should have a one written into them at initialization from both sides to assure that they are free when needed.

Table 3. Non-Contending Read/Write

Inputs				Outputs	Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_{0–7/8}$	
H	X	X	H	High Z	Power Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	↑	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 4. Interrupt Operation Example (assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = HIGH)

Function	Left Port					Right Port				
	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	$A_{0–12}$	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	$A_{0–12}$	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	1FFE	X
Reset Left $\overline{INT}$	X	L	L	1FFE	H	X	L	L	X	X
Set Right $\overline{INT}$	L	L	X	1FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	1FFF	H

Table 5. Semaphore Operation Example

Function	$I/O_{0-7/8}$ Left	$I/O_{0-7/8}$ Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.[5]

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage[6]..... –0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		7C144-15 7C145-15		7C144-25 7C145-25		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Commercial		220		180	mA
			Industrial				190	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[7]	Commercial		60		40	mA
			Industrial				50	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[7]	Commercial		130		110	mA
			Industrial				120	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[7]	Commercial		15		15	mA
			Industrial				30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[7]	Commercial		125		100	mA
			Industrial				115	

Notes
5. The Voltage on any input or I/O pin cannot exceed the power pin during power up.
6. Pulse width < 20 ns.
7. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}

Electrical Characteristics

Over the Operating Range (continued)

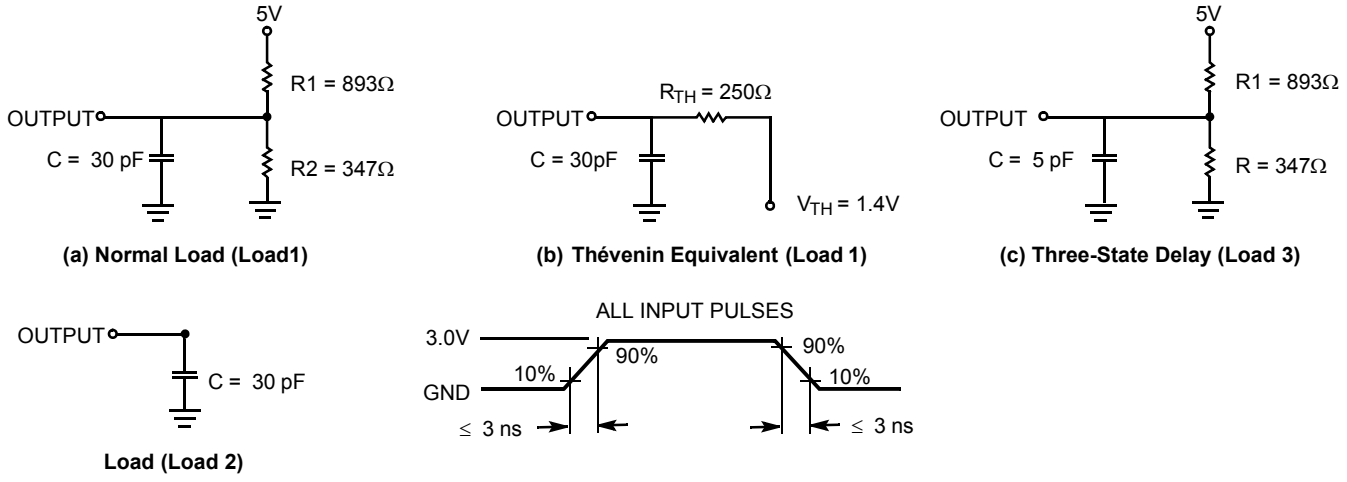
Parameter	Description	Test Conditions		7C144-35 7C145-35 Min	7C144-35 7C145-35 Max	7C144-55 7C145-55 Min	7C144-55 7C145-55 Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Commercial		160		160	mA
			Industrial		180		180	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[7]	Commercial		30		30	mA
			Industrial		40		40	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[7]	Commercial		100		100	mA
			Industrial		110		110	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[7]	Commercial		15		15	mA
			Industrial		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[7]	Commercial		90		90	mA
			Industrial		100		100	

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		15	pF

Figure 4. AC Test Loads and Waveforms



(a) Normal Load (Load1)

(b) Thévenin Equivalent (Load 1)

(c) Three-State Delay (Load 3)

Load (Load 2)

Switching Characteristics

Over the Operating Range[8]

Parameter	Description	7C144-15 7C145-15		7C144-25 7C145-25		7C144-35 7C145-35		7C144-55 7C145-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20		25	ns
t_{LZOE}[9, 10,11]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[9, 10,11]	$\overline{OE}$ HIGH to High Z		10		15		20		25	ns
t_{LZCE}[9, 10,11]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[9, 10,11]	$\overline{CE}$ HIGH to High Z		10		15		20		25	ns
t_{PU}[11]	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}[11]	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		45		ns
t_{AW}	Address Set-Up to Write End	12		20		30		45		ns
t_{HA}	Address Hold From Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		40		ns
t_{SD}	Data Set-Up to Write End	10		15		15		25		ns
t_{HD}	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[10,11]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[10,11]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[12]	Write Pulse to Data Delay		30		50		60		70	ns
t_{DDD}[12]	Write Data Valid to Read Data Valid		25		30		35		40	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. Test conditions used are Load 3.
11. This parameter is guaranteed but not tested.
12. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.

Switching Characteristics (continued)

Over the Operating Range[8]

Parameter	Description	7C144-15 7C145-15		7C144-25 7C145-25		7C144-35 7C145-35		7C144-55 7C145-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
BUSY TIMING[13]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20		30	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		30		30		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Data Valid		15		25		35		55	ns
INTERRUPT TIMING[13]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		35	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		35	ns
SEMAPHORE TIMING										
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

Note
13. Test conditions used are Load 2.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Either Port Address Access)[14, 15]

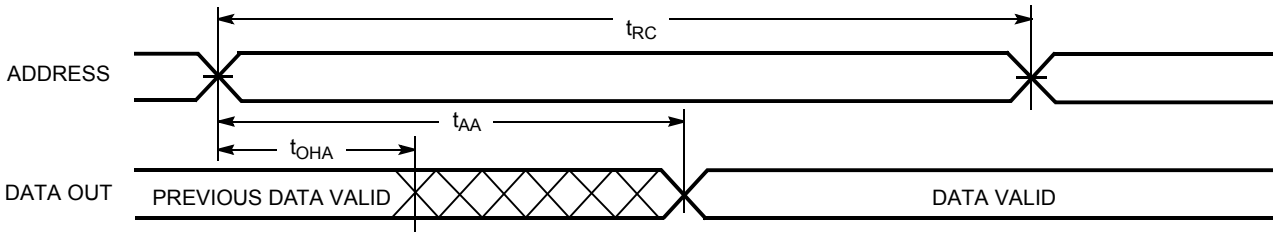


Figure 6. Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[14, 16, 17]

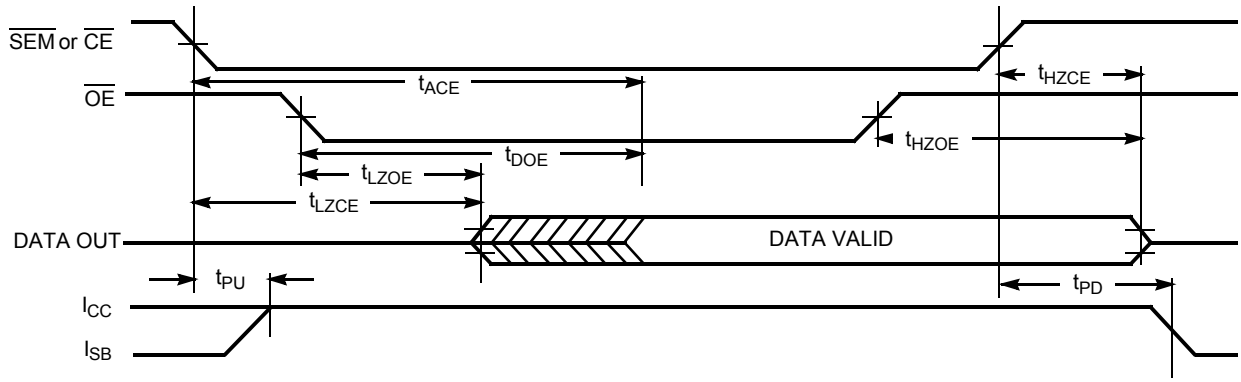
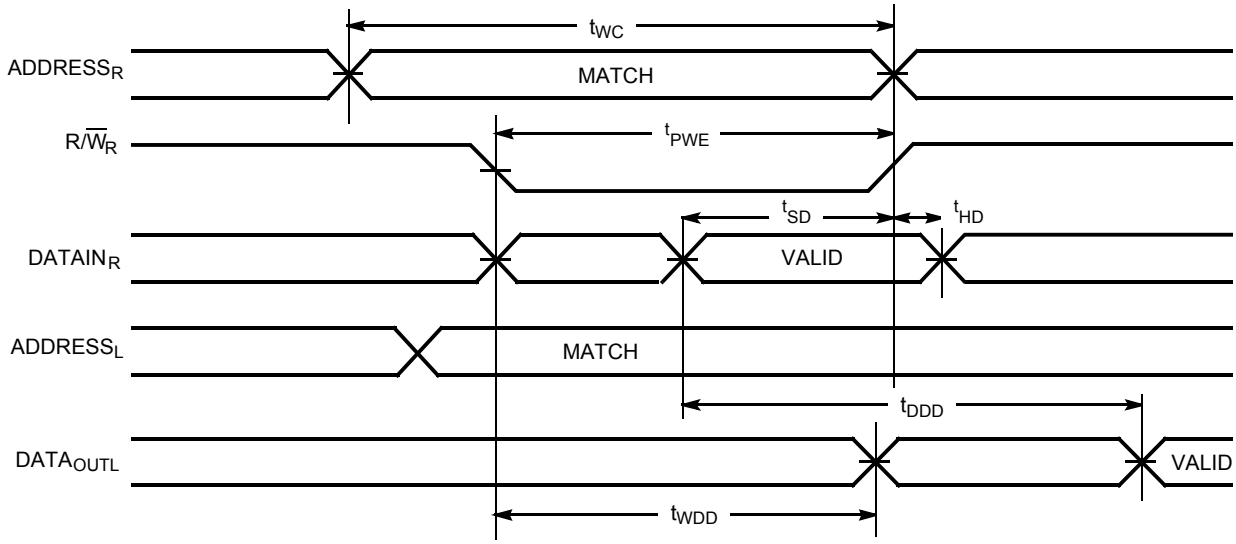


Figure 7. Read Timing with Port-to-Port Delay (M/$\overline{S}$=L)[18, 19]



Notes
14. R/$\overline{W}$ is HIGH for read cycle.
15. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
17. $\overline{CE_L}$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
18. $\overline{BUSY}$ = HIGH for the writing port.
19. $\overline{CE_L}$ = $\overline{CE_R}$ = LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1: $\overline{OE}$ Three-State Data I/Os (Either Port)[20, 21, 22]

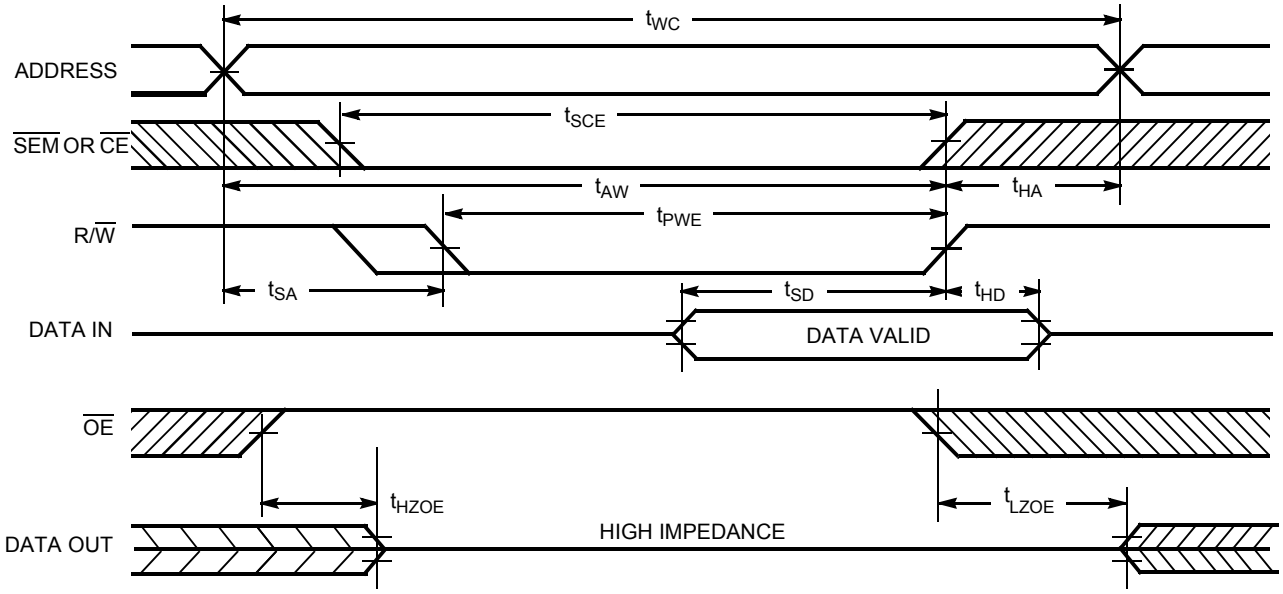
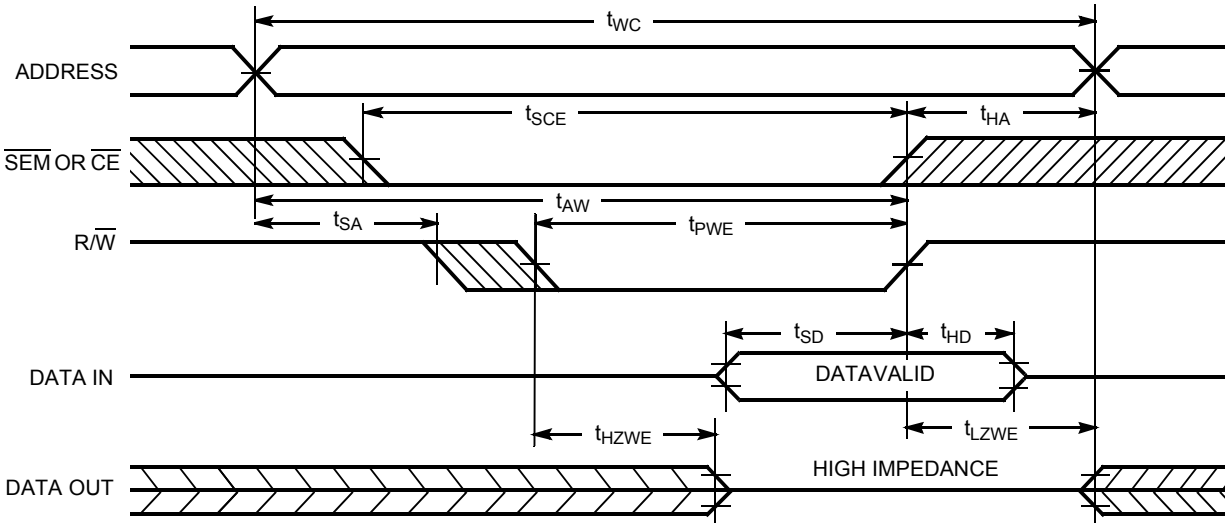


Figure 9. Write Cycle No. 2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[20, 22, 23]



Notes

20. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
21. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/W controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
22. R/$\overline{W}$ must be HIGH during all address transitions.
23. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Figure 10. Semaphore Read After Write Timing, Either Side[24]

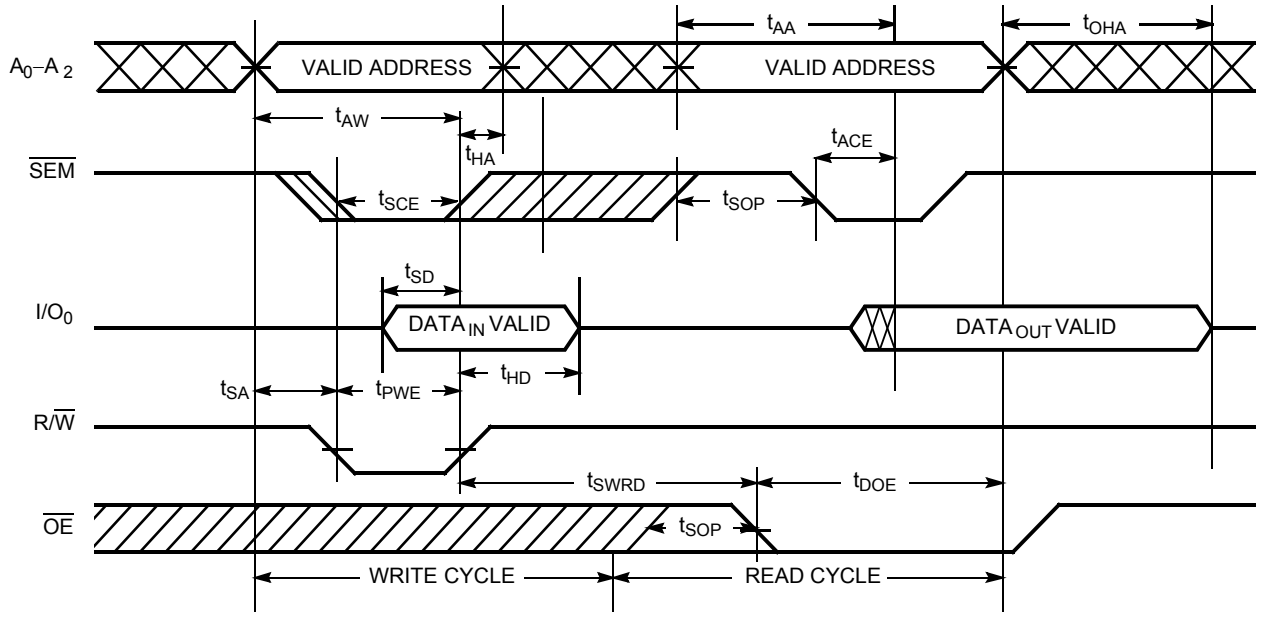
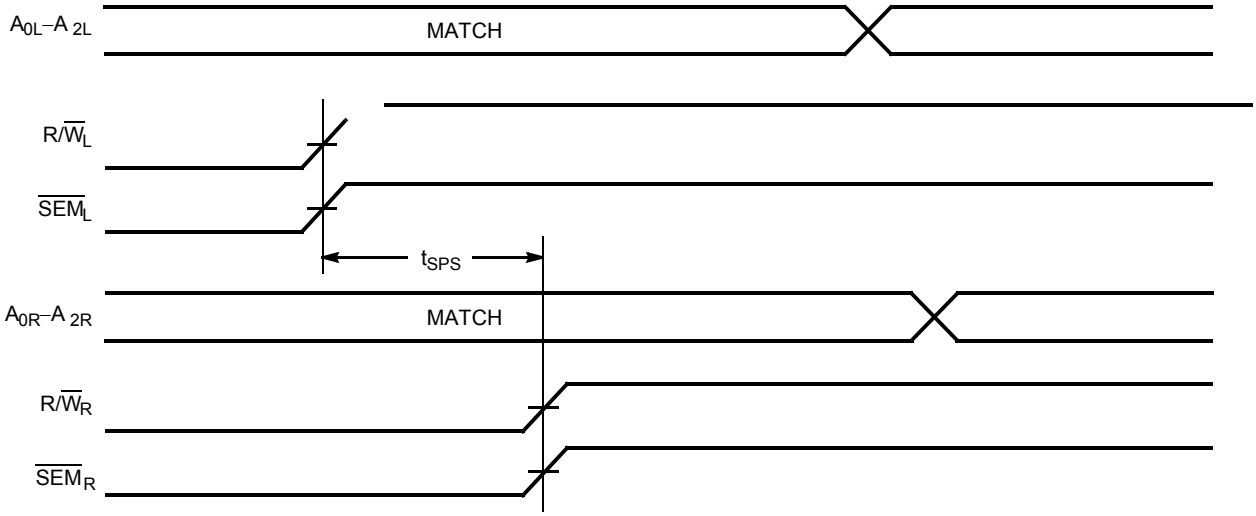


Figure 11. Semaphore Contention[25, 26, 27]



Notes
24. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
25. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
26. Semaphores are reset (available to both ports) at cycle start.
27. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Figure 12. Read with $\overline{\text{BUSY}}$ (M/S=HIGH)[19]

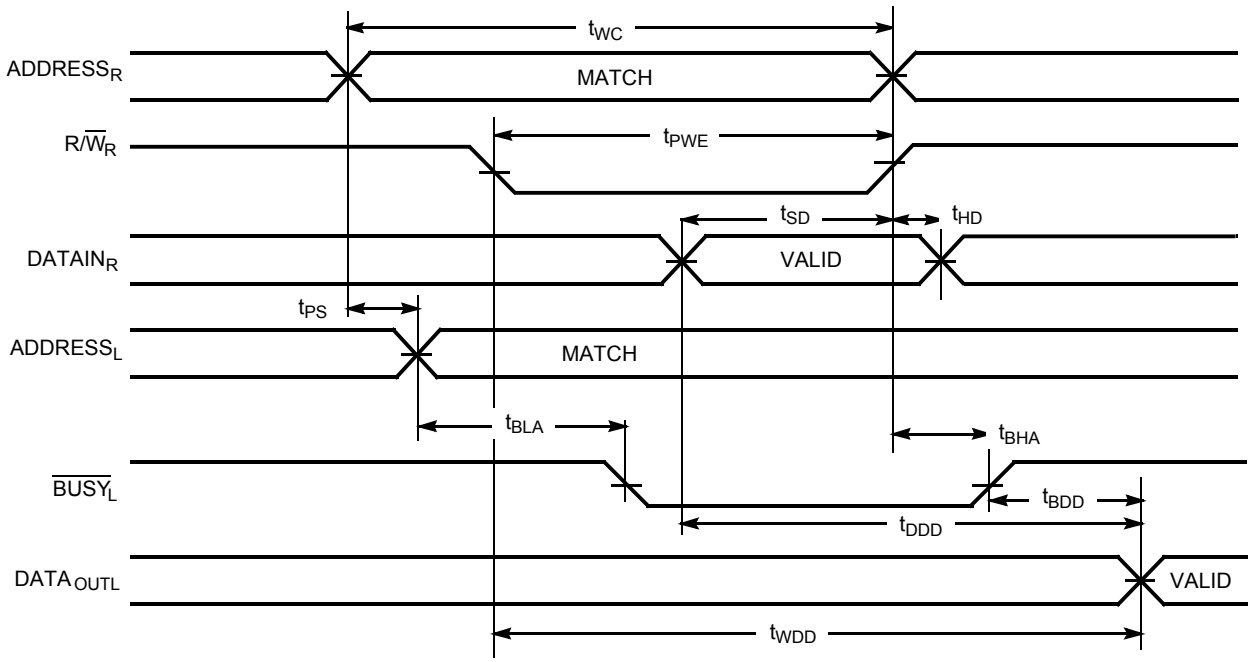
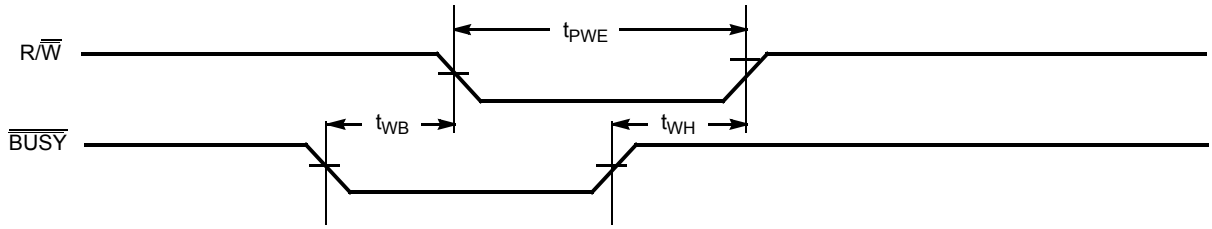


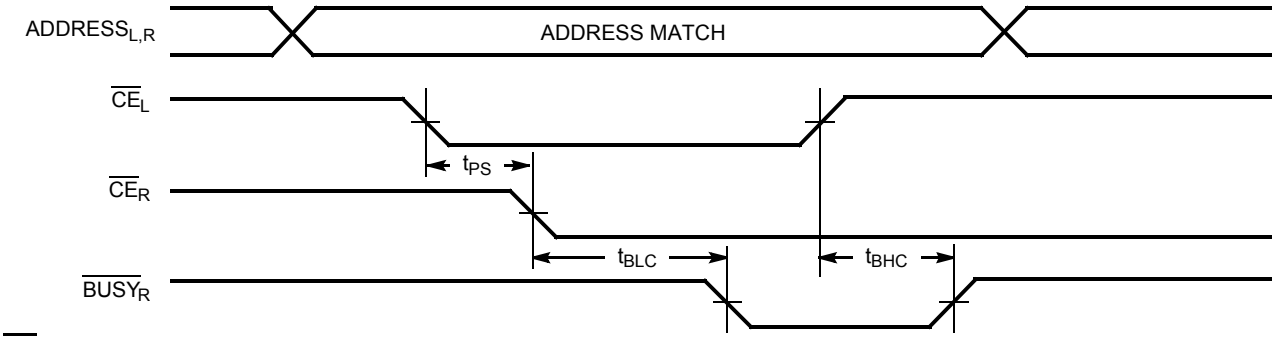
Figure 13. Write Timing with Busy Input (M/$\overline{\text{S}}$=LOW)



Switching Waveforms (continued)

Figure 14. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[28]

$\overline{CE}_L$ Valid First:



$\overline{CE}_R$ Valid First:

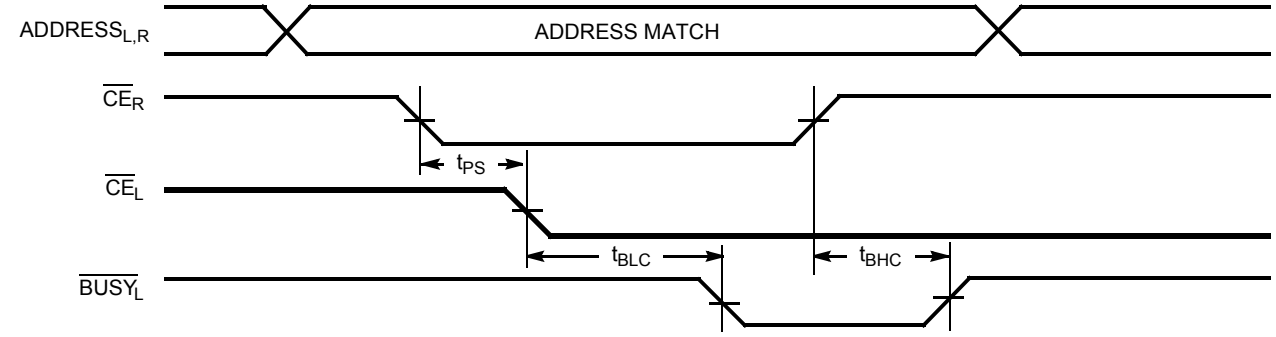
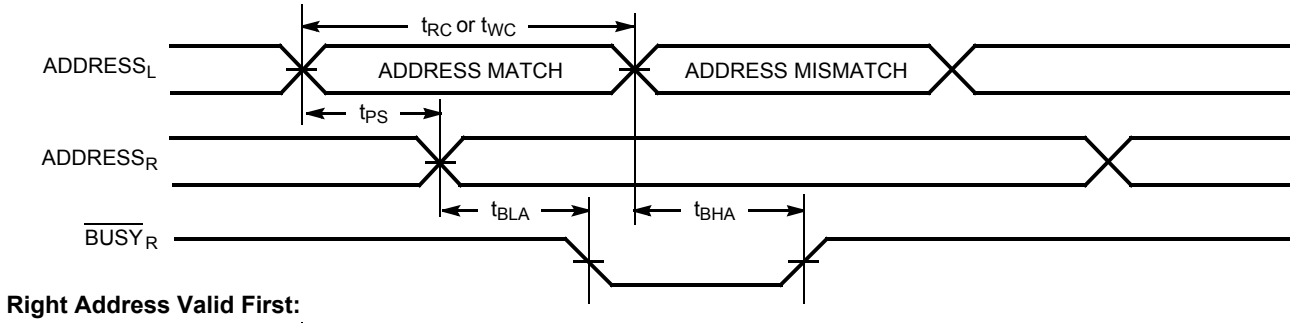
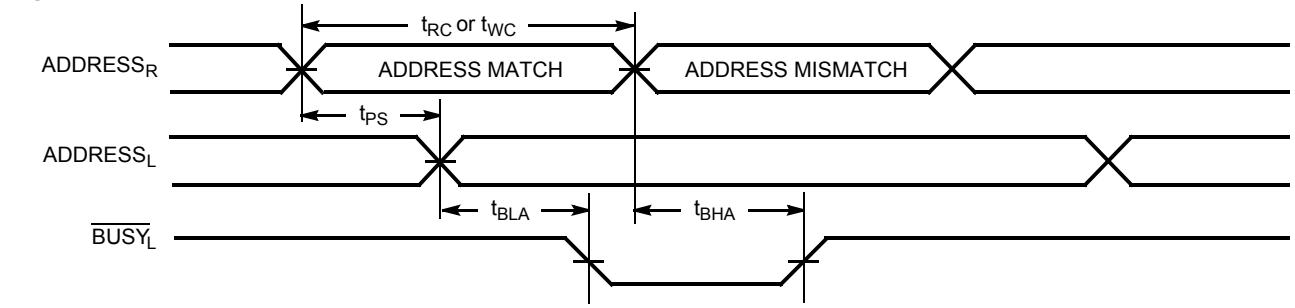


Figure 15. Busy Timing Diagram No. 2 (Address Arbitration)[28]

Left Address Valid First:



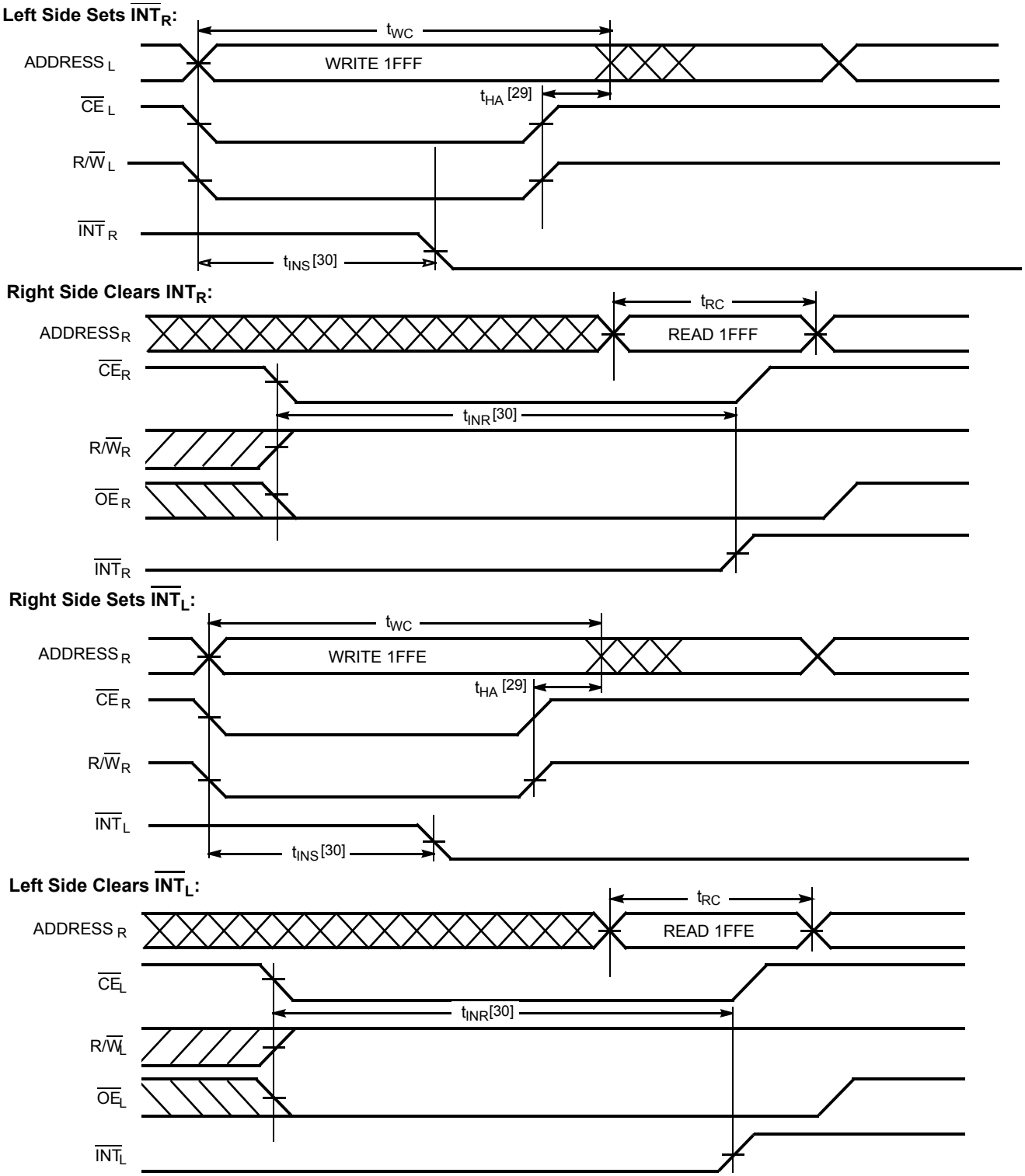
Right Address Valid First:



Note
28. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

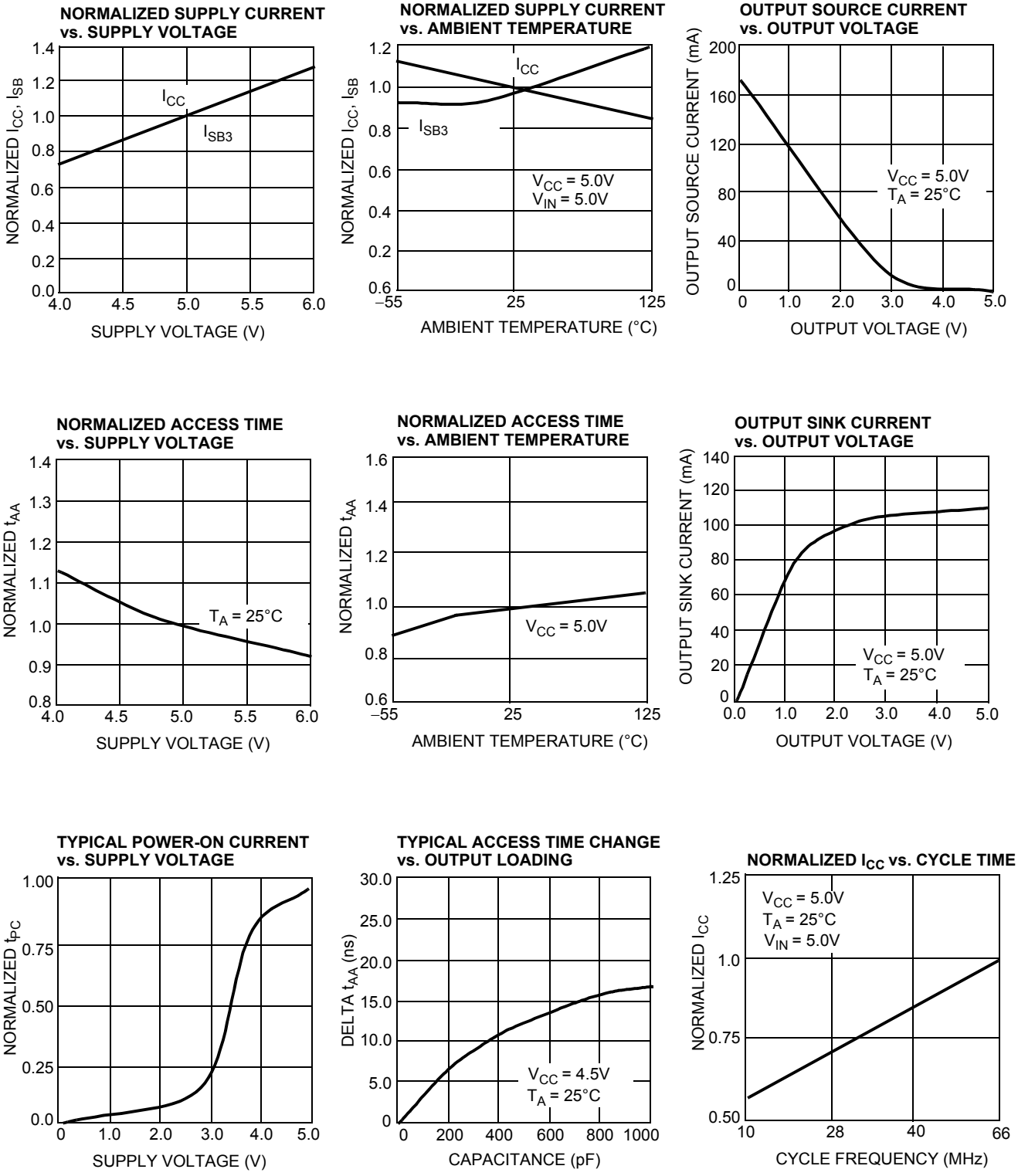
Switching Waveforms (continued)

Figure 16. Interrupt Timing Diagrams



Notes
29. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
30. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Figure 17. Typical DC and AC Characteristics

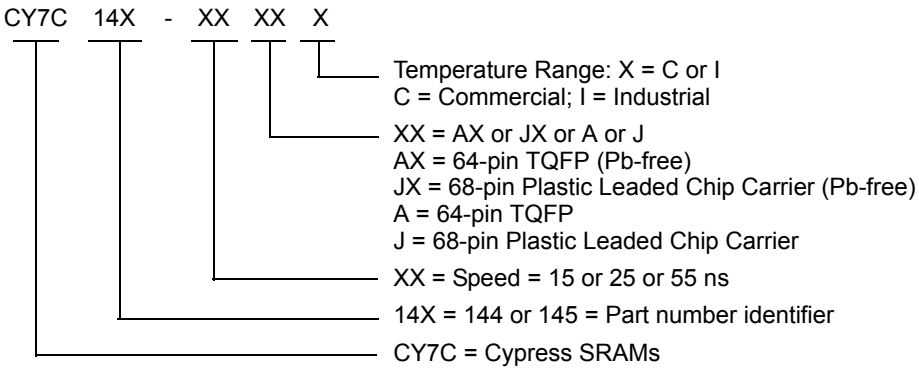


Ordering Information

8 K × 8 Dual-Port SRAM

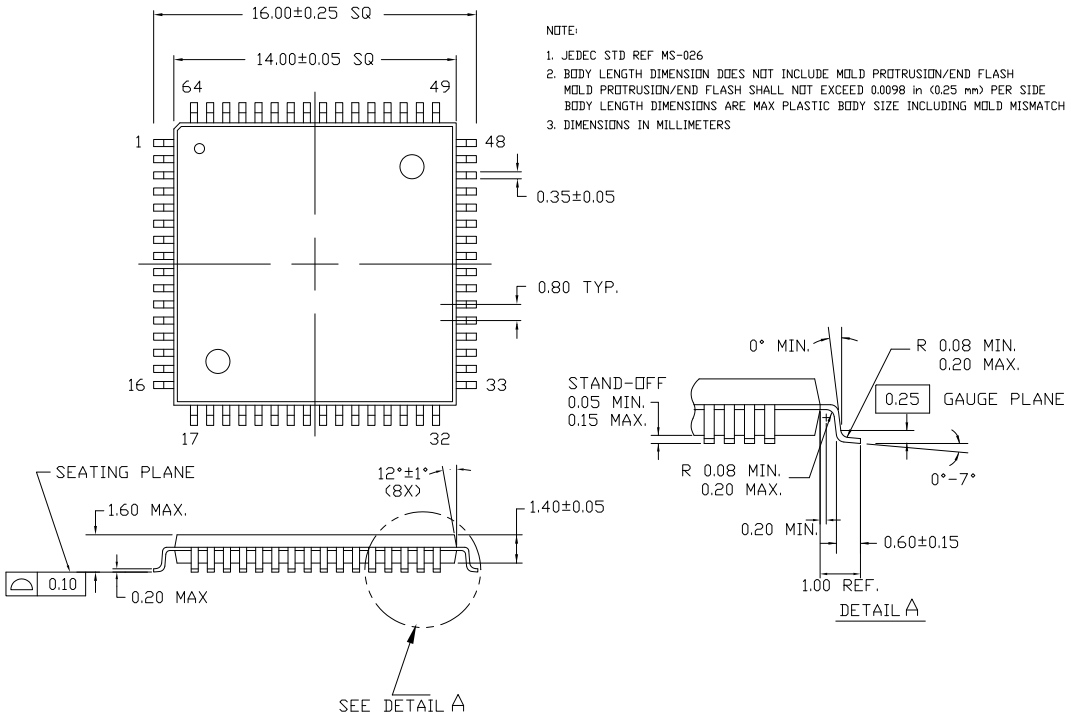
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C144-15AXC	51-85046	64-pin Thin Quad Flat Pack (Pb-free)	Commercial
	CY7C144-15JXI	51-85005	68-pin Plastic Leaded Chip Carrier (Pb-free)	Industrial
	CY7C144-15AXI	51-85046	64-pin Thin Quad Flat Pack (Pb-free)	
25	CY7C144-25AXC	51-85046	64-pin Thin Quad Flat Pack (Pb-free)	Commercial
55	CY7C144-55AC	51-85046	64-pin Thin Quad Flat Pack	Commercial
	CY7C144-55AXC	51-85046	64-pin Thin Quad Flat Pack (Pb-free)	
	CY7C144-55JC	51-85005	68-pin Plastic Leaded Chip Carrier	
	CY7C144-55JXC	51-85005	68-pin Plastic Leaded Chip Carrier (Pb-free)	
8 K × 9 Dual-Port SRAM				
15	CY7C145-15AXC	51-85065	80-pin Thin Quad Flat Pack (Pb-free)	Commercial

Ordering Code Definitions



Package Diagrams

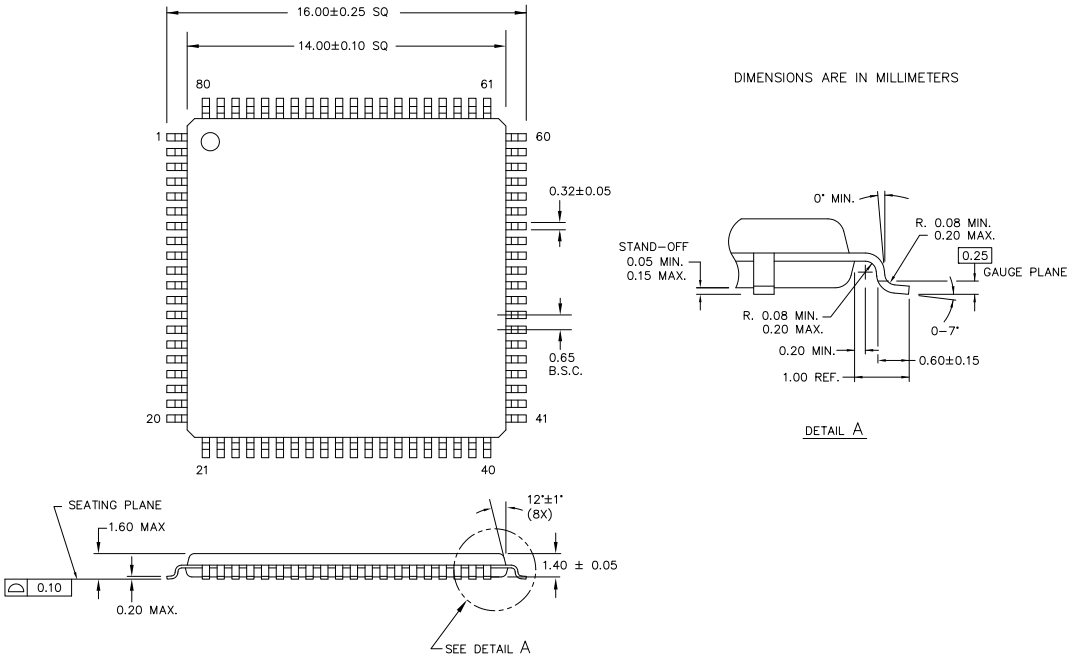
Figure 18. 64-Pin Thin Plastic Quad Flat Pack (14 x 14 x 1.4 mm), 51-85046



51-85046 *D

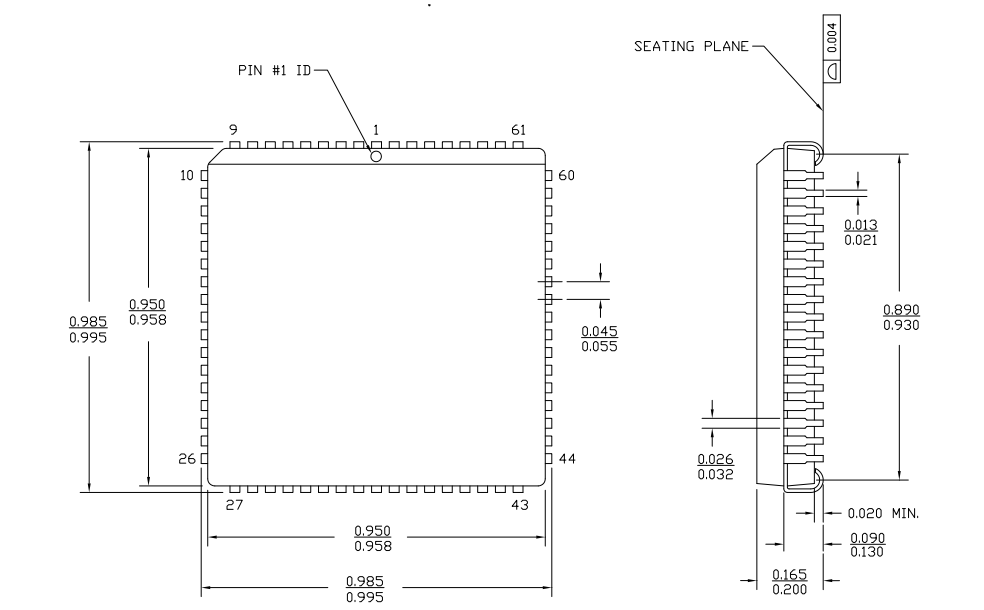
Package Diagrams (continued)

Figure 19. 80-Pin Thin Plastic Quad Flat Pack, 51-85065



51-85065 *C

Figure 20. 68-Pin Plastic Leaded Chip Carrier, 51-85005



DIMENSIONS IN INCHES MIN.
MAX.

51-85005 *B

Document History Page

Document Title: CY7C145, CY7C144 8K x 8/9 Dual-Port Static RAM with Sem, Int, Busy Document Number: 38-06034				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110175	SZV	09/29/01	Change from Spec number: 38-00163 to 38-06034
*A	122285	RBI	12/27/02	Power up requirements added to Maximum Ratings Information
*B	236752	YDT	See ECN	Removed cross information from features section, added CY7C144-15AI to ordering information section
*C	393320	YIM	See ECN	Added Pb-Free Logo Added Pb-Free parts to ordering information: CY7C144-15AXC, CY7C144-15JXC, CY7C144-15AXI, CY7C144-25AXC, CY7C144-55AXC, CY7C144-55JXC, CY7C145-15AXC, CY7C145-35JXC
*D	2623658	VKN/PYRS	12/17/2008	Added CY7C144-15JXI in the Ordering information table
*E	2699693	VKN/PYRS	04/29/2009	Corrected defective Logic Block diagram, Pinouts and Package diagrams
*F	2896210	RAME	03/22/2010	Updated Ordering Information Updated Package Diagrams
*G	3054633	ADMU	10/11/2010	Updated Ordering Information and added Ordering Code Definitions.

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