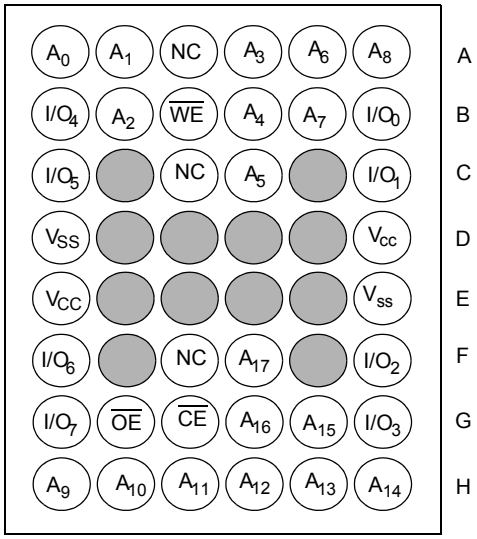
Contents

Pin Configuration

Figure 1. 36-ball FBGA pinout (Top View) [1]



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62138EV30LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... 55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to $V_{CC(MAX)}$ + 0.3 V

DC voltage applied to outputs in High Z state [3, 4] .....–0.3 V to $V_{CC(MAX)}$ + 0.3 V

DC input voltage [3, 4] .....–0.3 V to $V_{CC(MAX)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC}[5]
CY62138EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		CY62138EV30-45			Unit
				Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20 V	2.0	–	–	V
		I_{OH} = –1.0 mA	V_{CC} = 2.70 V	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20 V	–	–	0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70 V	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	V
		V_{CC}= 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} Operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels	–	15	20	mA
		f = 1 MHz		–	2	2.5	mA
I_{SB1}[7]	Automatic CE power down current – CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V, f = f_{max} (Address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = 3.60 V		–	1	7	µA
I_{SB2} [7]	Automatic CE power down current – CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 3.60 V		–	1	7	µA

Notes

3. $V_{IL(min.)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min.) and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25 °C.
7. Chip enable ($\overline{CE}$) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Capacitance

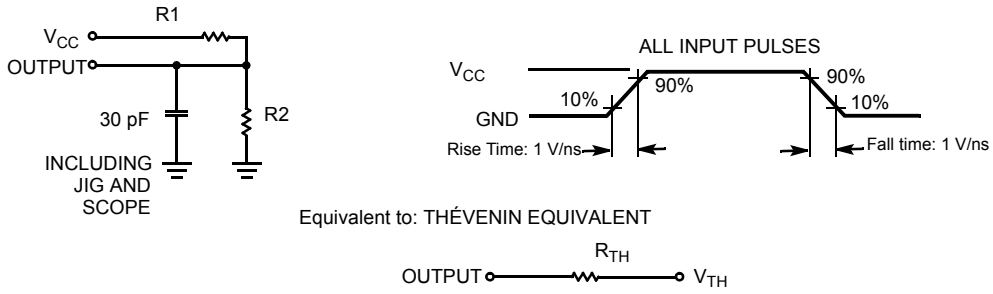
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ.)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	36-ball BGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	72	°C/W
Θ_{JC}	Thermal resistance (junction to case)		8.86	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

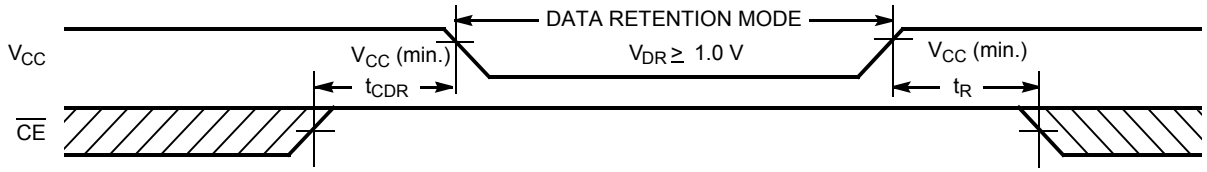
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	V
I_{CCDR} [10]	Data retention current	V_{CC} = 1 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	0.8	3	µA
t_{CDR}[11]	Chip deselect to data retention time		0	–	–	ns
t_R[12]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enable ($\overline{CE}$) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [15]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [15, 16]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [15]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [15, 16]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-up	–	45	ns
Write Cycle [17, 18]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [15, 16]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [15]	10	–	ns

Notes

13. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
14. Test conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
18. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1: Address Transition Controlled [19, 20]

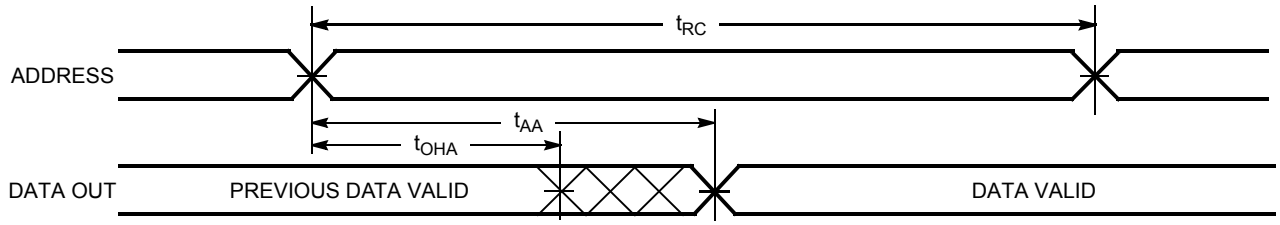
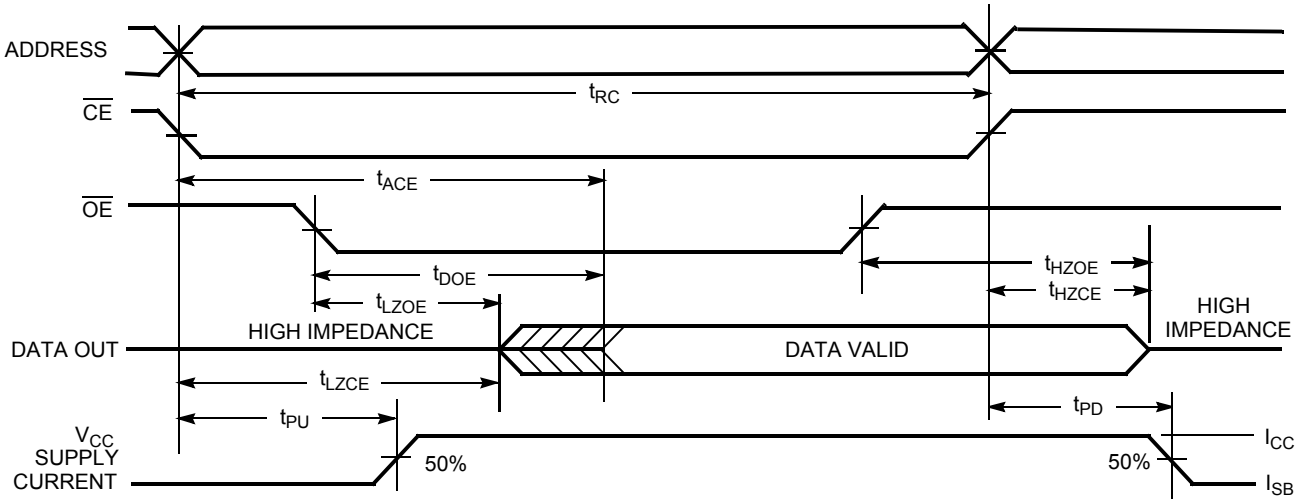


Figure 5. Read Cycle No. 2: $\overline{OE}$ Controlled [21, 22]



Notes
19. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
20. $\overline{WE}$ is HIGH for read cycle.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1: $\overline{WE}$ Controlled [23, 24]

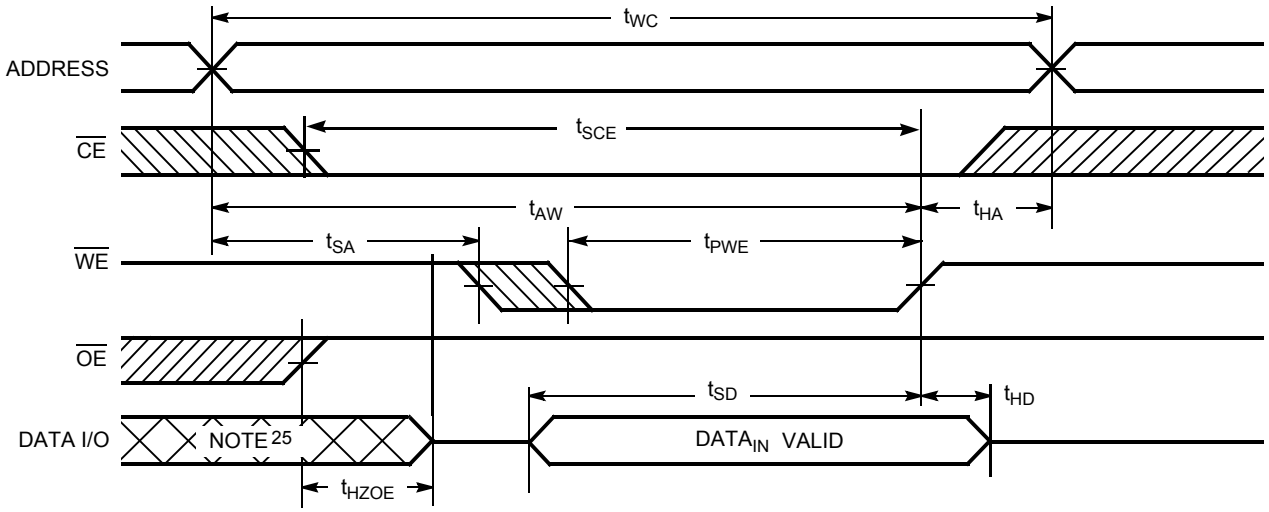
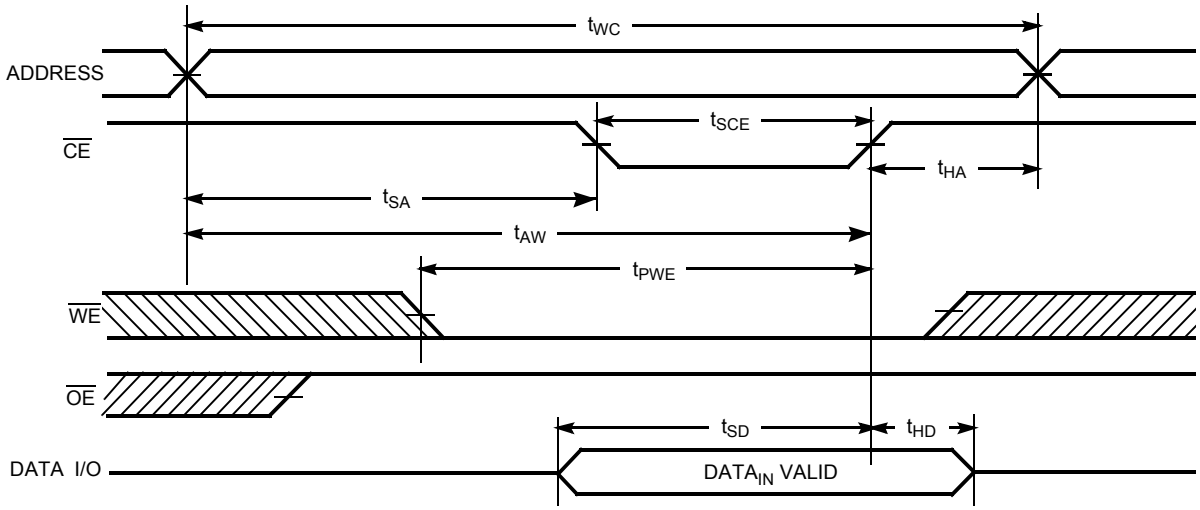


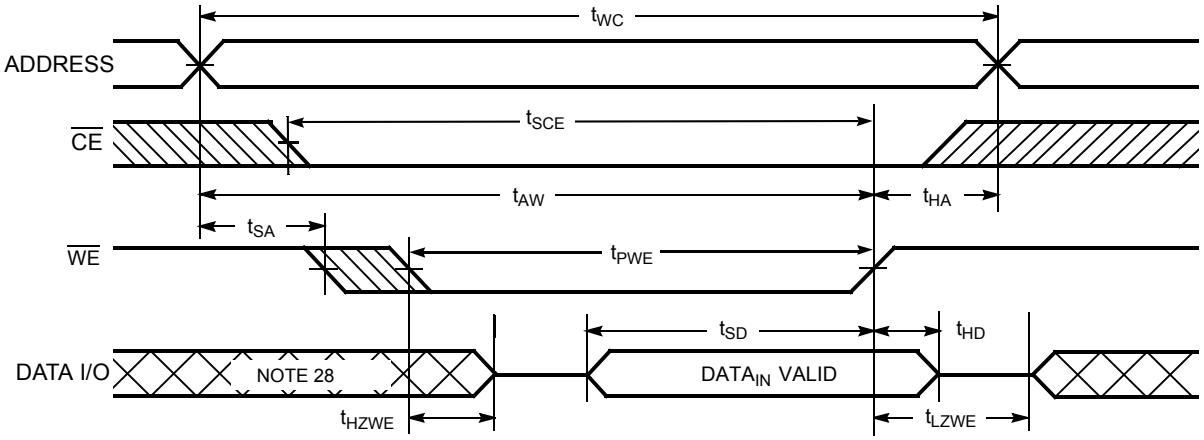
Figure 7. Write Cycle No. 2: $\overline{CE}$ Controlled [23, 24]



Notes
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3: $\overline{WE}$ Controlled, $\overline{OE}$ LOW [26, 27]



Notes
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
27. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
28. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

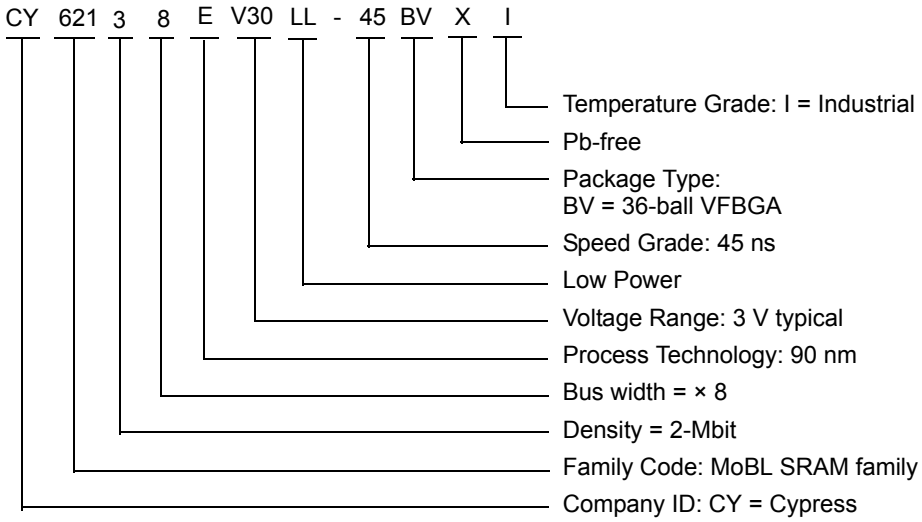
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H [29]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in (I/O_0–I/O_7)	Write	Active (I_{CC})

Note
29. Chip enable ($\overline{CE}$) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Ordering Information

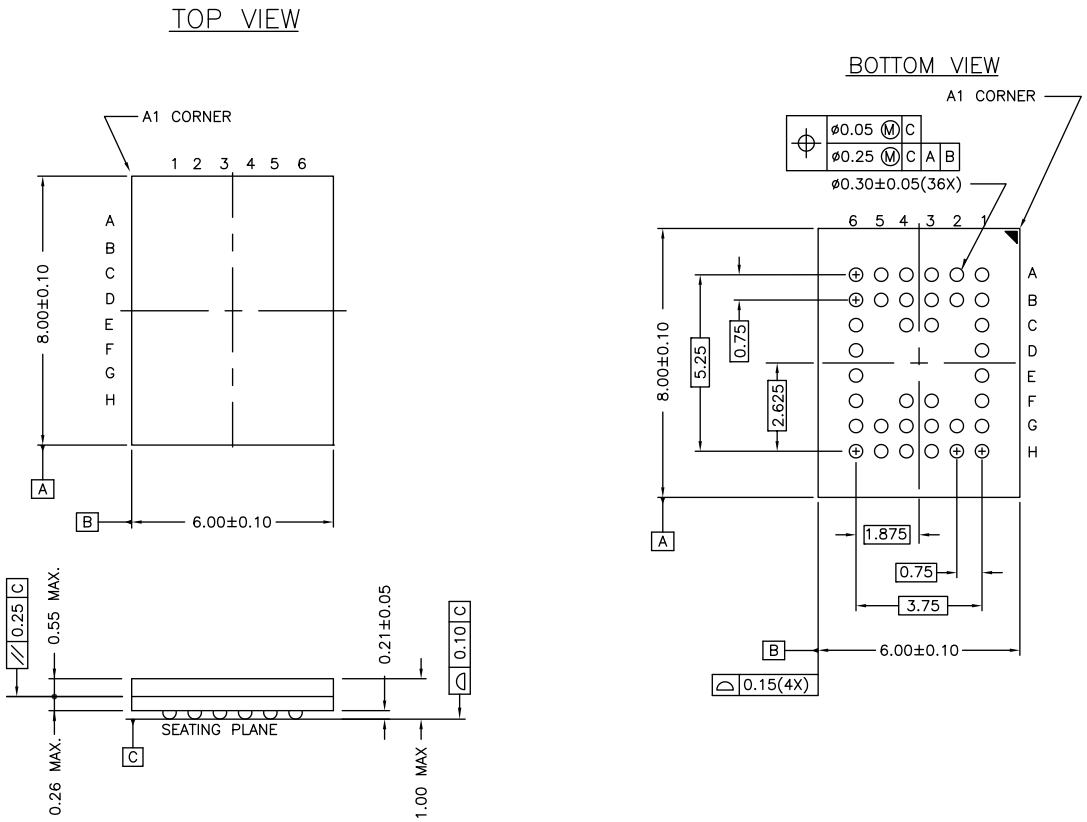
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138EV30LL-45BVXI	51-85149	36-ball VFBGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 9. 36-ball VFBGA (6 × 8 × 1.0 mm) BV36A Package Outline, 51-85149



51-85149 *F

Acronyms

Acronym	Description
BGA	ball gird array
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
FBGA	fine-pitch ball gird array
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
VFBGA	very fine ball gird array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
pF	picofarad
Ω	ohm
V	volt
W	watt

Document History Page

Document Title: CY62138EV30 MoBL®, 2-Mbit (256 K × 8) Static RAM Document Number: 38-05577				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	237432	AJU	See ECN	New data sheet.
*A	427817	NXR	See ECN	Removed 35 ns Speed Bin Removed “L” version Removed 32-pin TSOPII package from product Offering. Changed ball C3 from DNU to NC. Removed the redundant footnote on DNU. Moved Product Portfolio from Page # 3 to Page #2. Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f = 1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max}=1/t_{RC} Changed I_{SB1} and I_{SB2} Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA. Changed V_{CC} stabilization time in footnote #7 from 100 μs to 200 μs Changed the AC test load capacitance from 50pF to 30pF on Page# 4 Changed V_{DR} from 1.5V to 1V on Page# 4. Changed I_{CCDR} from 1 μA to 3 μA in the Data Retention Characteristics table on Page # 4. Corrected t_R in Data Retention Characteristics from 100 μs to t_{RC} ns Changed t_{OHA}, t_{LZCE}, t_{LZWE} from 6 ns to 10 ns Changed t_{HZOE}, t_{HZCE}, t_{HZWE} from 15 ns to 18 ns Changed t_{LZOE} from 3 ns to 5 ns Changed t_{SCE} and t_{AW} from 40 ns to 35 ns Changed t_{SD} from 20 ns to 25 ns Changed t_{PWE} from 25 ns to 35 ns Updated the Ordering Information table and replaced Package Name column with Package Diagram.
*B	2604685	VKN / PYRS	11/12/08	Updated Electrical Characteristics: Added Note 7 and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Added Note 10 and referred the same note in I_{CCDR} parameter.
*C	3143896	RAME	01/17/2011	Converted all tablenotes to Footnote. Added Ordering Code Definitions. Updated Package Diagram: spec 51-85149 – Changed revision from *C to *D. Added Acronyms and Units of Measure. Updated to new template.
*D	3284728	AJU	06/16/2011	Updated Functional Description: Removed the Note “For best practice recommendations, refer to the Cypress application note “SRAM System Design Guidelines” on http://www.cypress.com website.” and its reference. Updated to new template.
*E	3806123	TAVA	11/08/2012	Updated Data Retention Waveform (Updated Figure 3 (Changed “$V_{DR} \geq 1.5$ V” to “$V_{DR} \geq 1.0$ V”)). Updated Package Diagram (spec 51-85149 (Changed revision from *D to *E)).
*F	4099016	VINI	08/19/2013	Updated Switching Characteristics: Added Note 13 and referred the same note in “Parameter” column. Updated to new template. Completing Sunset Review.
*G	4576475	VINI	11/19/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.

Document History Page (continued)

Document Title: CY62138EV30 MoBL®, 2-Mbit (256 K × 8) Static RAM Document Number: 38-05577				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	5022355	VINI	11/20/2015	Updated Document Title to read as “CY62138EV30 MoBL®, 2-Mbit (256 K × 8) Static RAM”. Updated Switching Characteristics: Added Note 18 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 27 and referred the same note in Figure 8. Updated Package Diagram: spec 51-85149 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.

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