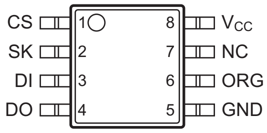
1. Pin Configurations and Pinouts

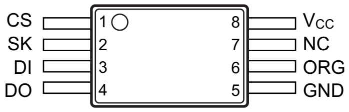
Table 1-1. Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
NC	No Connect

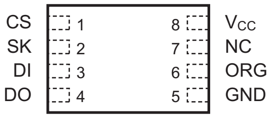
8-lead SOIC
(Top View)



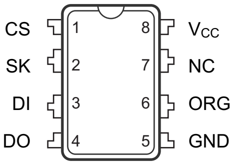
8-lead TSSOP
(Top View)



8-pad UDFN
(Top View)



8-lead PDIP
(Top View)



Note: Drawings are not to scale.

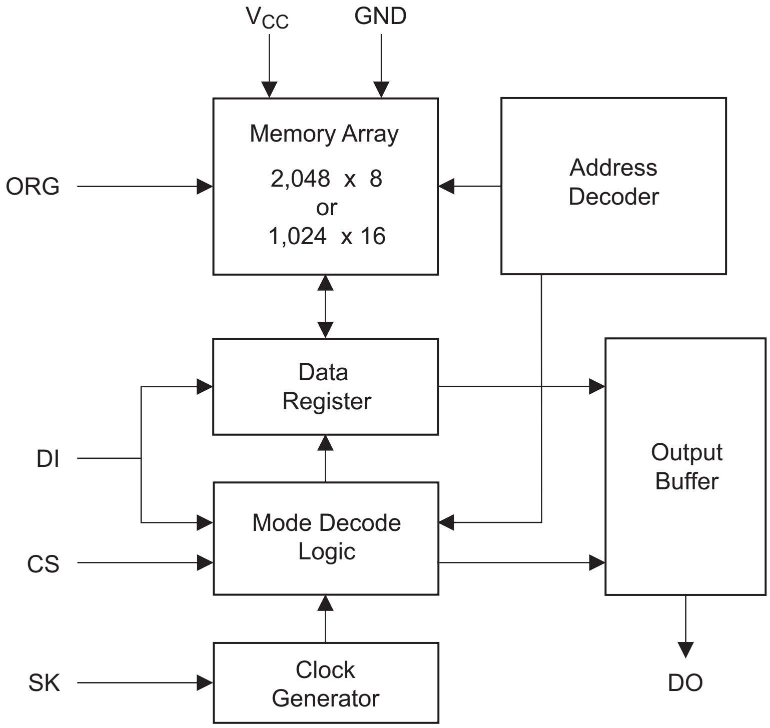
2. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.00V to +7.00V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram



Note: When the ORG pin is connected to V_{CC}, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, and the application does not load the input beyond the capability of the internal 1MΩ pull-up resistor, then the x16 organization is selected.

4. Memory Organization

4.1 Pin Capacitance

Table 4-1. Pin Capacitance(1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = 5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized, and is not 100% tested.

4.2 DC Characteristics

Table 4-2. DC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	Read at 1.0MHz		0.5	2.0	mA
			Write at 1.0MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0.4	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
V_{IL1}(1)	Input Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V		–0.6		0.8	V
V_{IH1}(1)	Input High Voltage	2.7V ≤ V_{CC} ≤ 5.5V		2.0		V_{CC} + 1	V
V_{IL2}(1)	Input Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V		–0.6		V_{CC} x 0.3	V
V_{IH2}(1)	Input High Voltage	1.8V ≤ V_{CC} ≤ 2.7V		V_{CC} x 0.7		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1mA			0.4	V
V_{OH1}	Output High Voltage	2.7V ≤ V_{CC} ≤ 5.5V	I_{OH} = –0.4mA	2.4			V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 2.5V	I_{OL} = 0.15mA			0.2	V
V_{OH2}	Output High Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OH} = –100µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only, and are not tested.

4.3 AC Characteristics

Table 4-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to + 85°C, CL = 1 TTL gate and 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$		0		2	MHz
		$2.7V \le V_{CC} \le 5.5V$		0		1	MHz
		$1.8V \le V_{CC} \le 5.5V$		0		250	kHz
t_{SKH}	SK High Time	$2.7V \le V_{CC} \le 5.5V$		250			ns
		$1.8V \le V_{CC} \le 5.5V$		1000			ns
t_{SKL}	SK Low Time	$2.7V \le V_{CC} \le 5.5V$		250			ns
		$1.8V \le V_{CC} \le 5.5V$		1000			ns
t_{CS}	Minimum CS Low Time	$2.7V \le V_{CC} \le 5.5V$		250			ns
		$1.8V \le V_{CC} \le 5.5V$		1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$2.7V \le V_{CC} \le 5.5V$	50			ns
			$1.8V \le V_{CC} \le 5.5V$	200			ns
t_{DIS}	DI Setup Time	Relative to SK	$2.7V \le V_{CC} \le 5.5V$	100			ns
			$1.8V \le V_{CC} \le 5.5V$	400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$2.7V \le V_{CC} \le 5.5V$	100			ns
			$1.8V \le V_{CC} \le 5.5V$	400			ns
t_{PD1}	Output Delay to 1	AC Test	$2.7V \le V_{CC} \le 5.5V$			250	ns
			$1.8V \le V_{CC} \le 5.5V$			1000	ns
t_{PD0}	Output Delay to 0	AC Test	$2.7V \le V_{CC} \le 5.5V$			250	ns
			$1.8V \le V_{CC} \le 5.5V$			1000	ns
t_{SV}	CS to Status Valid	AC Test	$2.7V \le V_{CC} \le 5.5V$			250	ns
			$1.8V \le V_{CC} \le 5.5V$			1000	ns
t_{DF}	CS to DO in High-impedance	AC Test	$2.7V \le V_{CC} \le 5.5V$			150	ns
		CS = V_{IL}	$1.8V \le V_{CC} \le 5.5V$			400	ns
t_{WP}	Write Cycle Time		$1.8V \le V_{CC} \le 5.5V$	0.1	3	10	ms
Endurance(1)	5.0V, 25°C			1,000,000			Write Cycles

Note: 1. This parameter is characterized, and is not 100% tested.

5. Functional Description

The AT93C86A is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by seven instructions issued by the Host processor. A valid instruction starts with a rising edge of CS and consists of a Start bit (Logic 1), followed by the appropriate opcode, and the desired memory address location.

Table 5-1. AT93C86A Instruction Set

Instruction	SB	Opcode	Address		Data		Comments
			x8(1)	x16(1)	x8	x16	
READ	1	10	$A_{10} – A_0$	$A_9 – A_0$			Reads data stored in memory at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write Enable must precede all programming modes.
ERASE	1	11	$A_{10} – A_0$	$A_9 – A_0$			Erases memory location $A_N – A_0$.
WRITE	1	01	$A_{10} – A_0$	$A_9 – A_0$	$D_7 – D_0$	$D_{15} – D_0$	Writes memory location $A_N – A_0$.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXXXX	01XXXXXX	$D_7 – D_0$	$D_{15} – D_0$	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Note: 1. The ‘X’ in the address field represent don’t care values, and must be clocked.

READ: The READ instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the Serial Output pin, DO. Output data changes are synchronized with the rising edges of the Serial Clock pin, SK. It should be noted that a dummy bit (Logic 0) precedes the 8-bit or 16-bit data output string. The AT93C86A supports sequential Read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (Logic 0) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

Erase/Write Enable (EWEN): To ensure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out.

Note: Once in the EWEN state, programming remains enabled until an EWDS instruction is executed, or V_{CC} power is removed from the part.

ERASE: The ERASE instruction programs all bits in the specified memory location to the Logic 1 state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. A Logic 1 at the DO pin indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE: The WRITE instruction contains the 8-bits or 16-bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at Serial Data Input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction, and the part is ready for further instructions. A Ready/Busy status cannot be obtained if CS is brought high after the end of the self-timed programming cycle, t_{WP}.

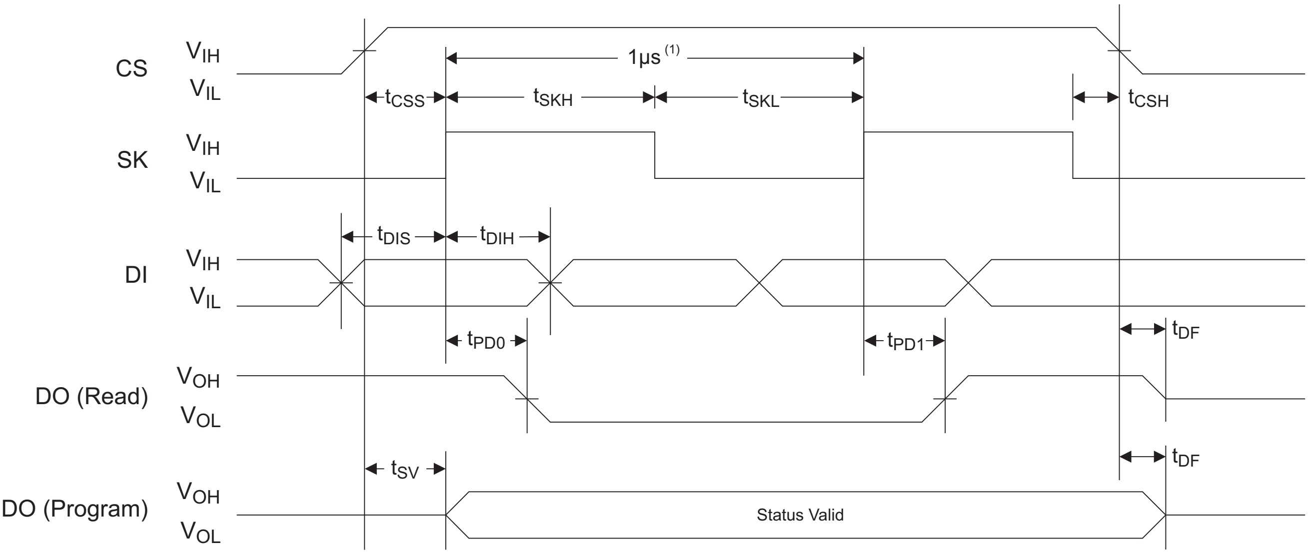
Erase All (ERAL): The Erase All (ERAL) instruction programs every bit in the Memory Array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

Write All (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

Erase/Write Disable (EWDS): To protect against accidental data disturbance, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

6. Timing Diagrams

Figure 6-1. Synchronous Data Timing



Note: 1. This is the minimum SK period.

Table 6-1. Organization Key for Timing Diagrams

I/O	AT93C86A (16K)	
	x8	x16
A_N	A_{10}	A_9
D_N	D_7	D_{15}

Figure 6-2. ERASE Timing

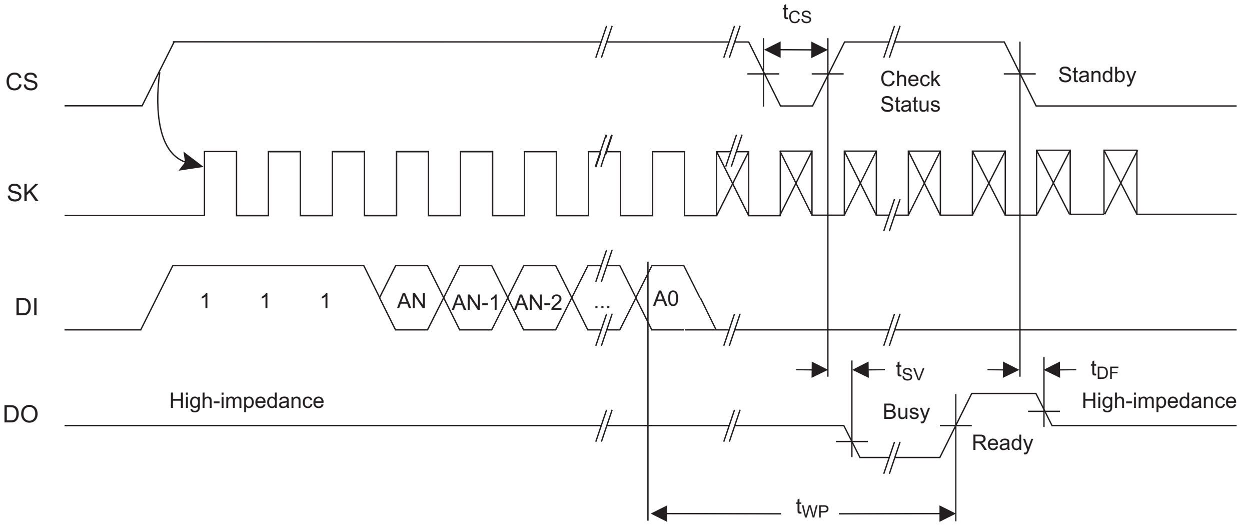


Figure 6-3. READ Timing

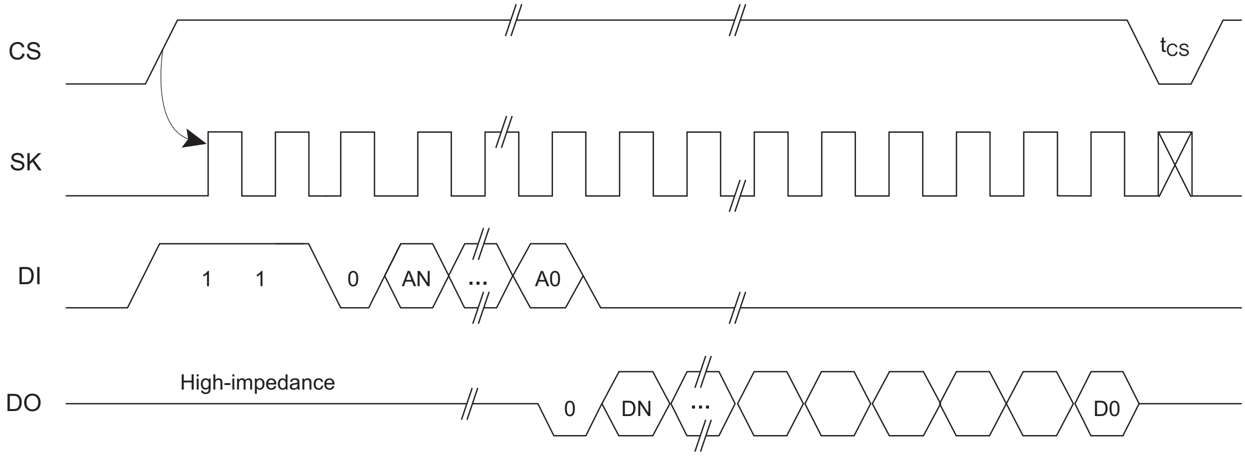


Figure 6-4. EWEN Timing

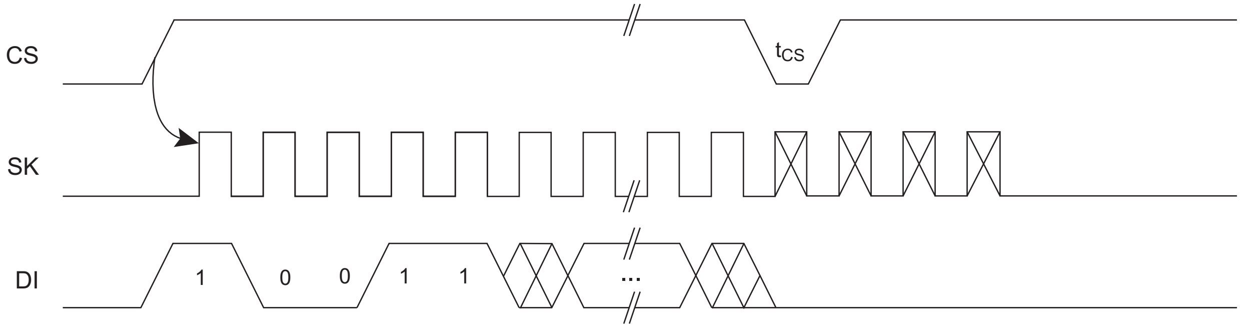


Figure 6-5. WRITE Timing

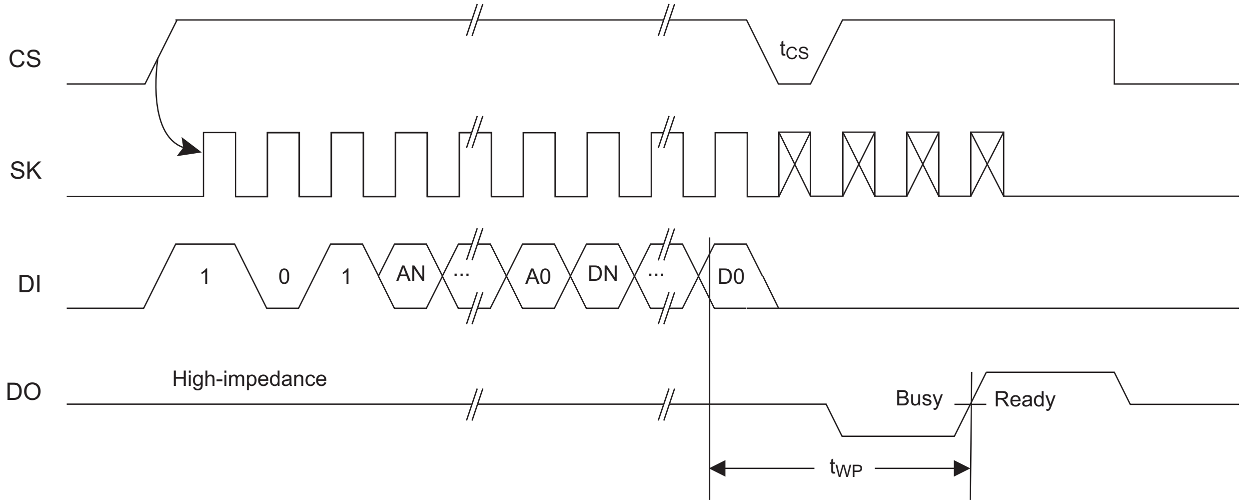
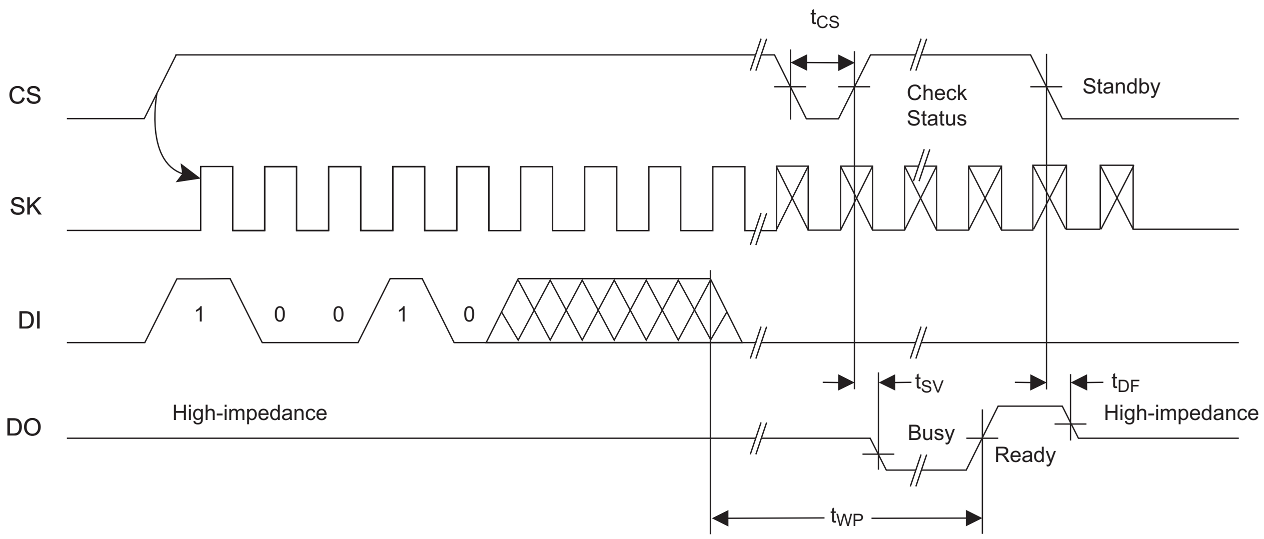
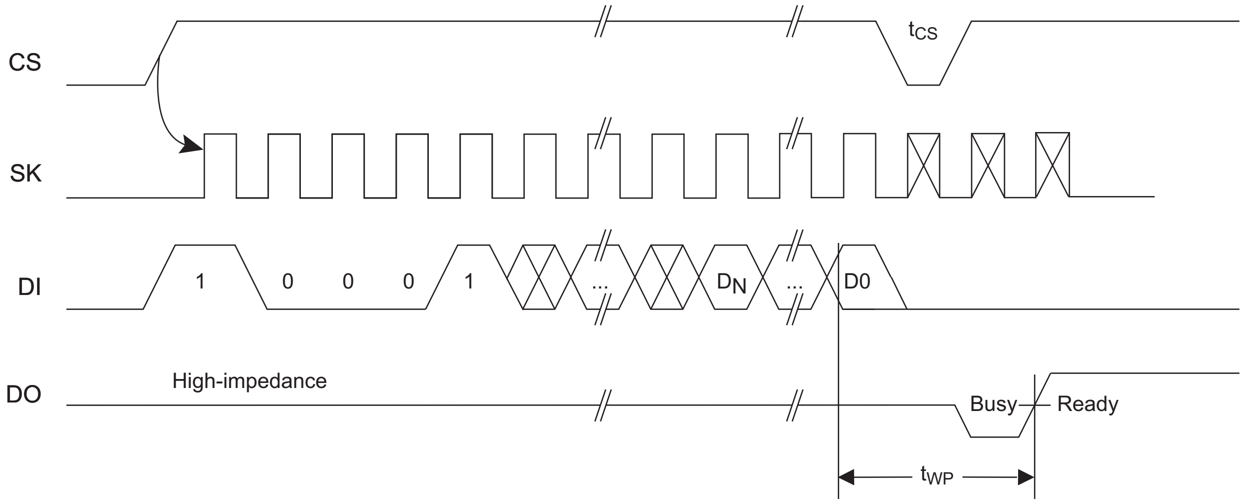


Figure 6-6. **ERAL Timing**[(1)]



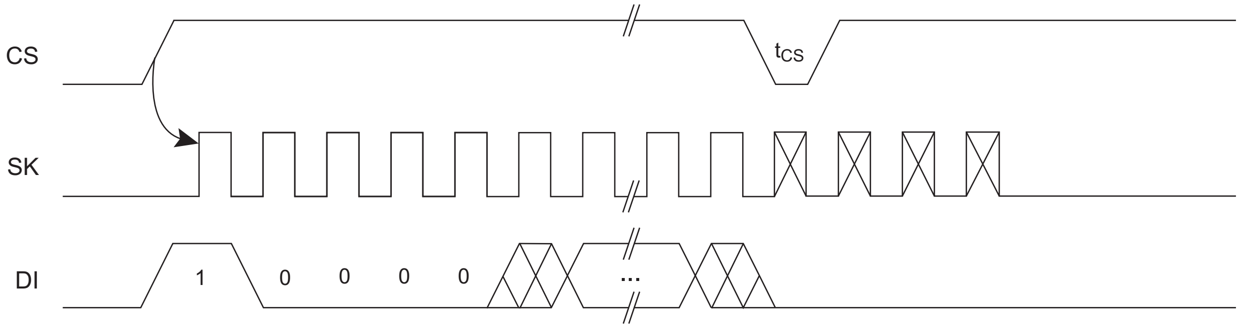
Note: 1. V_{CC} = 4.5V to 5.5V.

Figure 6-7. **WRAL Timing**[(1)]

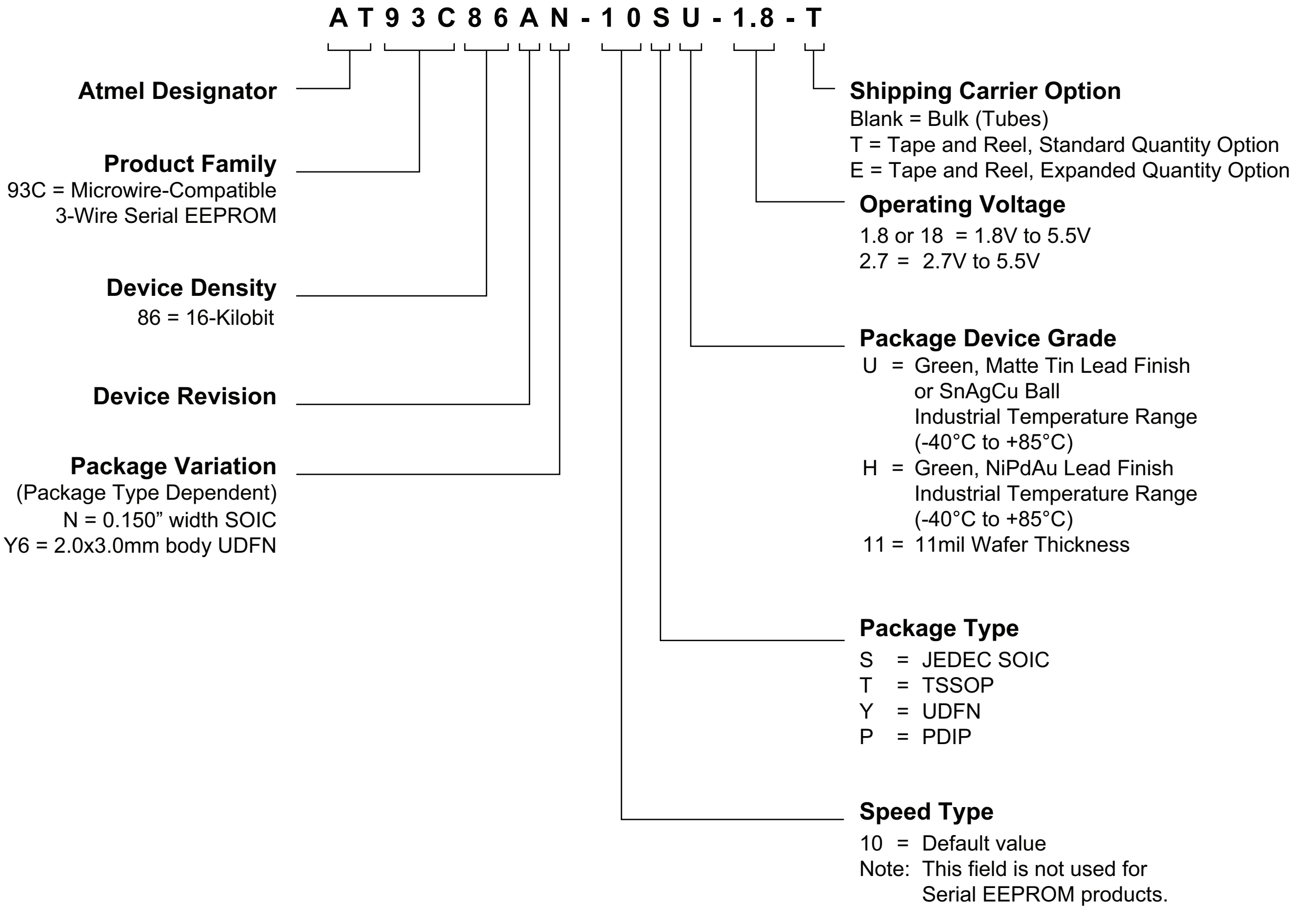


Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

Figure 6-8. **EWDS Timing**



7. Ordering Code Detail



AT93C86AN-10SU-1.8-T

Atmel Designator

Product Family
93C = Microwire-Compatible 3-Wire Serial EEPROM

Device Density
86 = 16-Kilobit

Device Revision

Package Variation
(Package Type Dependent)
N = 0.150” width SOIC
Y6 = 2.0x3.0mm body UDFN

Shipping Carrier Option
Blank = Bulk (Tubes)
T = Tape and Reel, Standard Quantity Option
E = Tape and Reel, Expanded Quantity Option

Operating Voltage
1.8 or 18 = 1.8V to 5.5V
2.7 = 2.7V to 5.5V

Package Device Grade
U = Green, Matte Tin Lead Finish or SnAgCu Ball Industrial Temperature Range (-40°C to +85°C)
H = Green, NiPdAu Lead Finish Industrial Temperature Range (-40°C to +85°C)
11 = 11mil Wafer Thickness

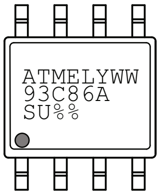
Package Type
S = JEDEC SOIC
T = TSSOP
Y = UDFN
P = PDIP

Speed Type
10 = Default value
Note: This field is not used for Serial EEPROM products.

8. Part Markings

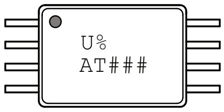
AT93C86A: Package Marking Information

8-lead SOIC



Note: Lot Number and location of assembly on the bottom side of the package.

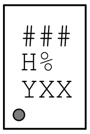
8-lead TSSOP



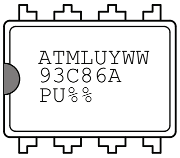
Note: Lot Number, location of assembly and YWW date code on the bottom side of the package.

8-pad UDFN

2.0 x 3.0 mm Body



8-lead PDIP



Note: Lot Number and location of assembly on the bottom side of the package.

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation	
AT93C86A	Truncation Code ###: 86A

Date Codes				**Voltages**
Y = Year		M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014	8: 2018	A: January	02: Week 2	3 or 27: 2.7V min
5: 2015	9: 2019	B: February	04: Week 4	1 or 18: 1.8V min
6: 2016	0: 2020	...	...	
7: 2017	1: 2021	L: December	52: Week 52	

Country of Assembly	**Lot Number**	**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number	H: Industrial/NiPdAu U: Industrial/Matte Tin/SnAgCu

Trace Code	**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ	AT: Atmel ATM: Atmel ATML: Atmel

6/11/14

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **93C86ASM**, AT93C86A Package Marking Information	**DRAWING NO.** 93C86ASM	**REV.** A

9. Ordering Information

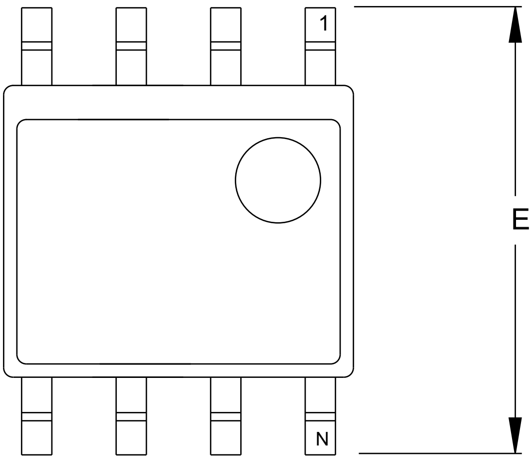
Atmel Ordering Code (1)	Lead Finish	Package	Voltage	Delivery Information		Operation Range
				Form	Quantity	
AT93C86A-10SU-1.8	Matte Tin Lead-free Halogen-free	8S1	1.8V to 5.5V	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT93C86A-10SU-1.8-T			1.8V to 5.5V	Tape and Reel	4,000 per Reel	
AT93C86A-10SU-2.7			2.7V to 5.5V(1)	Bulk (Tubes)	100 per Tube	
AT93C86A-10SU-2.7-T			2.7V to 5.5V(1)	Tape and Reel	4,000 per Reel	
AT93C86A-10TU-1.8		8X	1.8V to 5.5V	Bulk (Tubes)	100 per Tube	
AT93C86A-10TU-1.8-T			1.8V to 5.5V	Tape and Reel	5,000 per Reel	
AT93C86A-10TU-2.7			2.7V to 5.5V(1)	Bulk (Tubes)	100 per Tube	
AT93C86A-10TU-2.7-T			2.7V to 5.5V(1)	Tape and Reel	5,000 per Reel	
AT93C86A-10PU-1.8		8P3	1.8V to 5.5V	Bulk (Tubes)	50 per Tube	
AT93C86A-10PU-2.7			2.7V to 5.5V(1)	Bulk (Tubes)	50 per Tube	
AT93C86AY6-10YH-1.8-T	NiPdAu Lead-free Halogen-free	8MA2	1.8V to 5.5V	Tape and Reel	5,000 per Reel	
AT93C86AY6-10YH-18-E				Tape and Reel	15,000 per Reel	

Notes: 1. For 2.7V devices used in a 4.5V to 5.5V range, please refer to performance values in Section 4.2, "DC Characteristics" and 4.3, "AC Characteristics" on page 5.

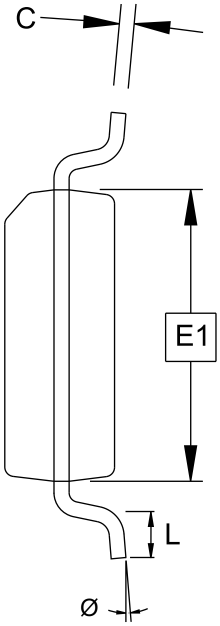
Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing, Small Outline (JEDEC SOIC)
8X	8-lead, 0.170" wide, Thin Shrink Small Outline (TSSOP)
8P3	8-lead, 0.300" wide body, Plastic Dual In-line Package (PDIP)
8MA2	8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Ultra Thin Dual No Lead (UDFN)

10. Packaging Information

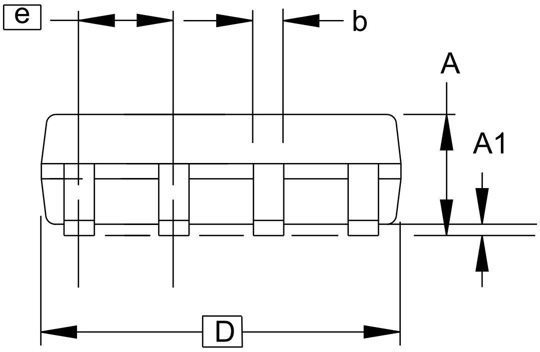
10.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

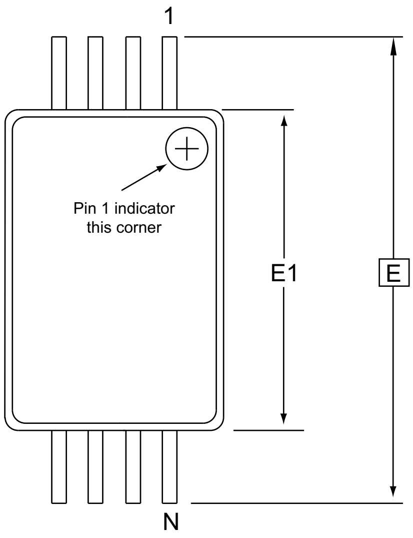
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.90 BSC			
E	6.00 BSC			
E1	3.90 BSC			
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

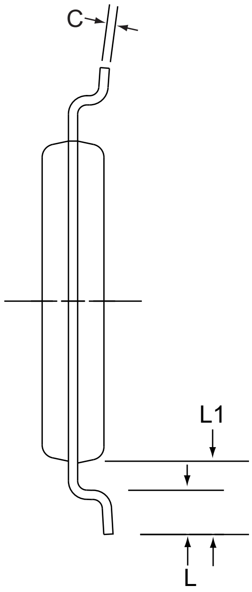
3/6/2015

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	SWB	8S1	H

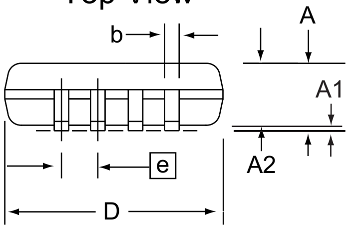
10.2 8X — 8-lead TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

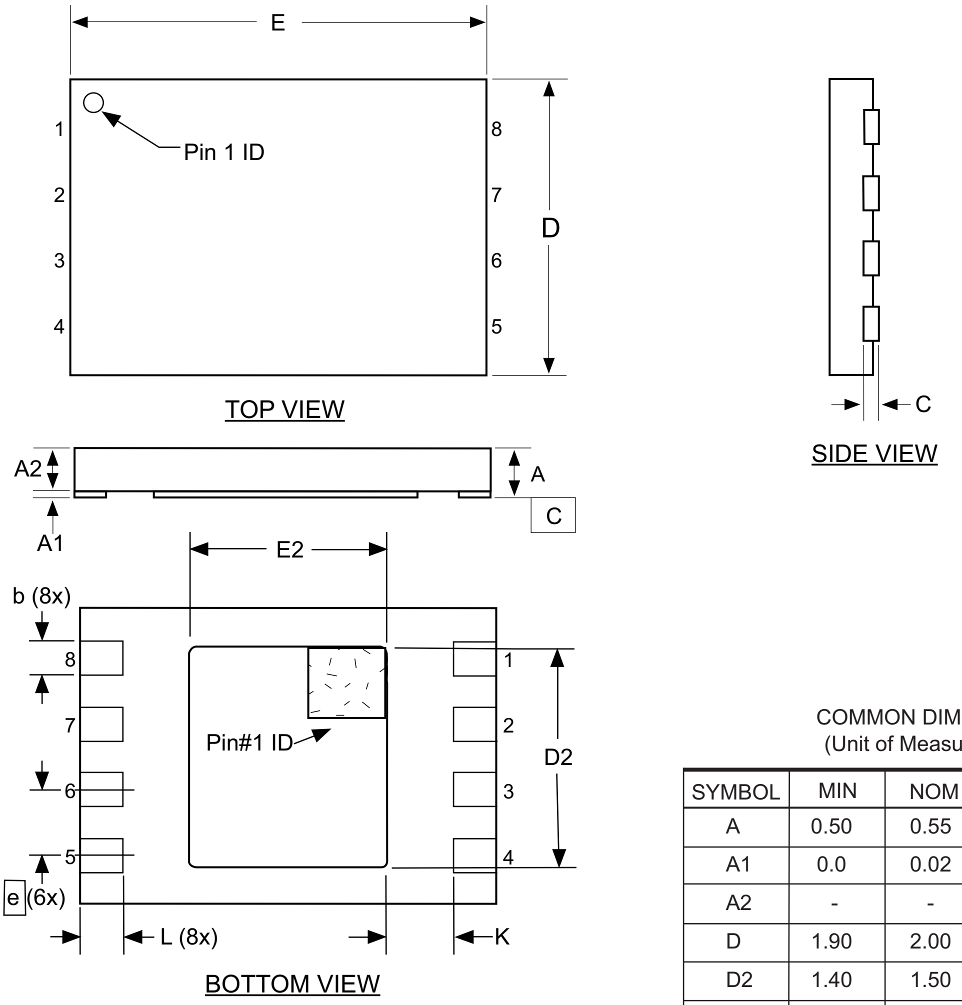
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

2/27/14

	TITLE	GPC	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	TNR	8X	E

10.3 8MA2 — 8-pad UDFN



Notes:

1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

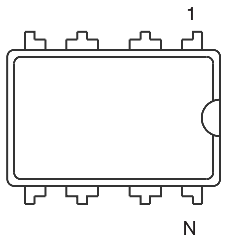
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C	0.152 REF			
L	0.35	0.40	0.45	
e	0.50 BSC			
K	0.20	-	-	

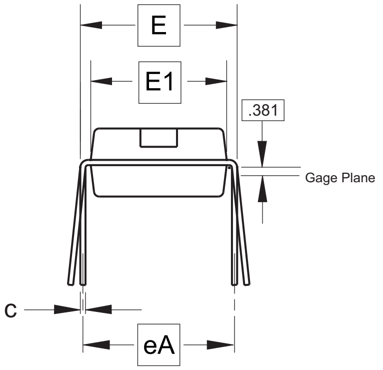
11/2/15

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** H

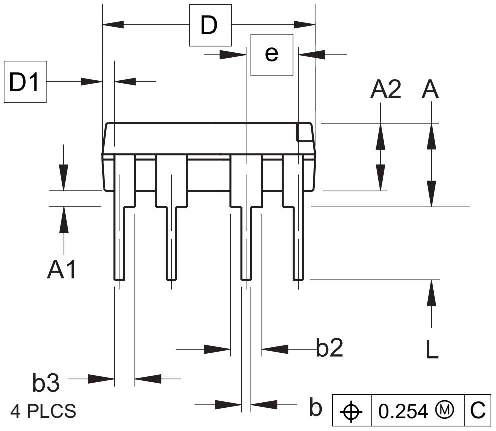
10.4 8P3 — 8-lead PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	5.334	2
A1	0.381	-	-	
A2	2.921	3.302	4.953	
b	0.356	0.457	0.559	5
b2	1.143	1.524	1.778	6
b3	0.762	0.991	1.143	6
c	0.203	0.254	0.356	
D	9.017	9.271	10.160	3
D1	0.127	0.000	0.000	3
E	7.620	7.874	8.255	4
E1	6.096	6.350	7.112	3
e	2.540 BSC			
eA	7.620 BSC			4
L	2.921	3.302	3.810	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

07/31/14

Package Drawing Contact: packagedrawings@atmel.com	TITLE 8P3, 8-lead, 0.300” Wide Body, Plastic Dual In-line Package (PDIP)	GPC PTC	DRAWING NO. 8P3	REV. E

11. Revision History

Revision No.	Date	Comments
3408L	01/2017	Added Bulk (Tube) Shipping Carrier Option Changed Standard Quantity Tape and Reel Option to “T” Updated Ordering Information Table Removed AT93C86A-W1.8-11 Part Number
3408K	12/2015	Correct Ordering Code Detail and update the 8S1 and 8MA2 package drawings.
3408J	01/2015	Add the UDFN extended quantity option and update the ordering information section. Update the 8MA2 and 8P3 package drawings.
3408I	08/2014	Update pinouts, 8MA2 package drawing, grammatical changes, document template, logos, and disclaimer page. No changes to functional specification.
3408H	01/2007	Add “Bottom View” to page 1 Ultra Thin MiniMap package drawing page 4 revise Note 1 added “ensured by characterization”.
3408G	07/2006	Revision history implemented. Delete ‘Preliminary’ status from datasheet; Add ‘Ultra Thin’ description to MLP 2x3 package; Delete ‘1.8V not available’ on Figure 1 Note; Add 1.8V range on Table 4 under Write Cycle Time.

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