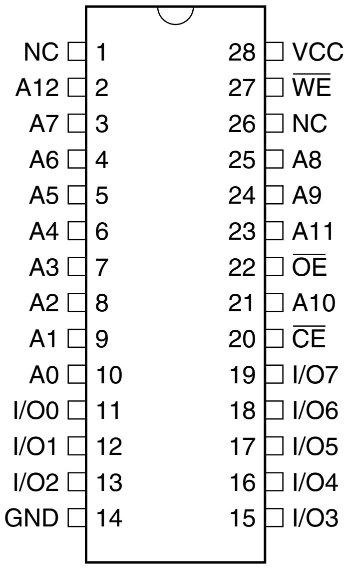
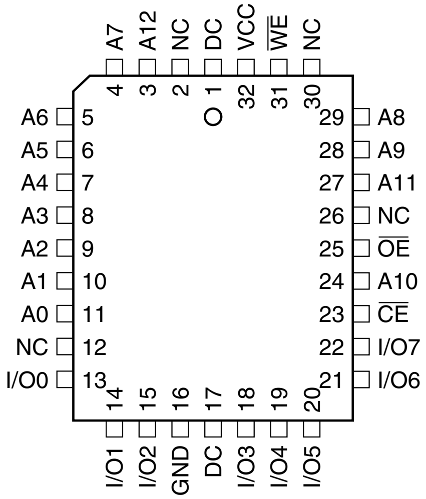
2. Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don’t Connect

2.1 28-lead PDIP/SOIC Top View

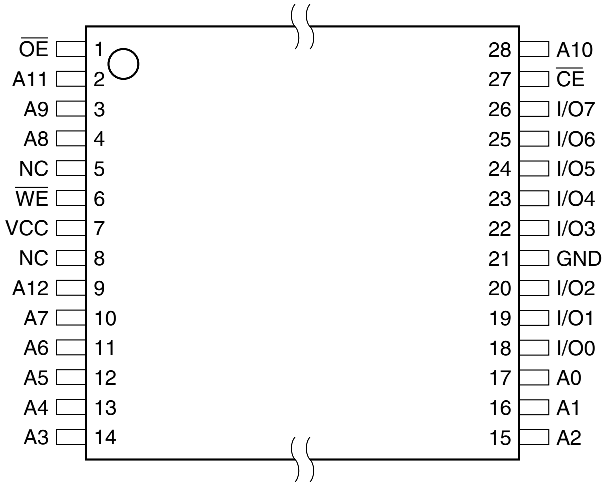


2.2 32-lead PLCC Top View

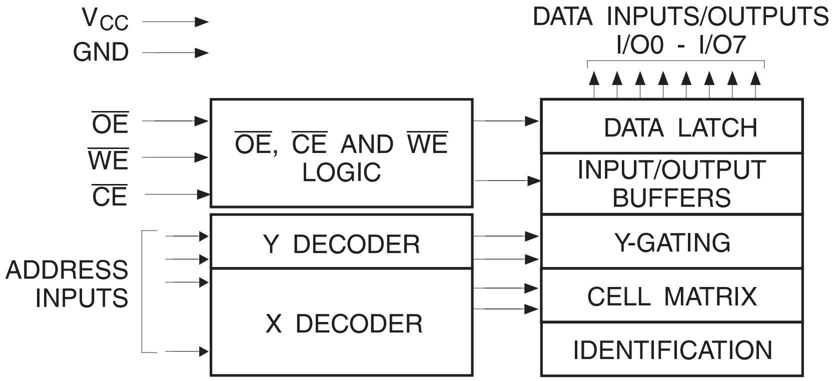


Note: PLCC package pins 1 and 17 are Don’t Connect.

2.3 28-lead TSOP Top View



3. Block Diagram



4. Device Operation

4.1 Read

The AT28BV64B is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their systems.

4.2 Byte Write

A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

4.3 Page Write

The page write operation of the AT28BV64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 100 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28BV64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

4.4 $\overline{\text{DATA}}$ Polling

The AT28BV64B features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{\text{DATA}}$ Polling may begin at anytime during the write cycle.

4.5 Toggle Bit

In addition to $\overline{\text{DATA}}$ Polling, the AT28BV64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

4.6 Data Protection

If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel® has incorporated both hardware and software features that will protect the memory against inadvertent writes.

4.6.1 Hardware Protection

Hardware features protect against inadvertent writes to the AT28BV64B in the following ways: (a) V_{CC} power-on delay – once V_{CC} has reached 1.8V (typical) the device will automatically time out 10 ms (typical) before allowing a write; (b) write inhibit – holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; and (c) noise filter – pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

4.6.2 Software Data Protection

A software-controlled data protection feature has been implemented on the AT28BV64B. Software data protection (SDP) helps prevent inadvertent writes from corrupting the data in the device. SDP can prevent inadvertent writes during power-up and power-down as well as any other potential periods of system instability.

The AT28BV64B can only be written using the software data protection feature. A series of three write commands to specific addresses with specific data must be presented to the device before writing in the byte or page mode. The same three write commands must begin each write operation. All software write commands must obey the page mode write timing specifications. The data in the 3-byte command sequence is not written to the device; the addresses in the command sequence can be utilized just like any other location in the device.

Any attempt to write to the device without the 3-byte sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

4.7 Device Identification

An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

5. DC and AC Operating Range

	AT28BV64B-20
Operating Temperature (Case)	-40° C - 85° C
V_{CC} Power Supply	2.7V to 3.6V

6. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H(3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.

2. Refer to AC Programming Waveforms.

3. $V_H = 12.0V \pm 0.5V$.

7. Absolute Maximum Ratings*

Temperature Under Bias	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

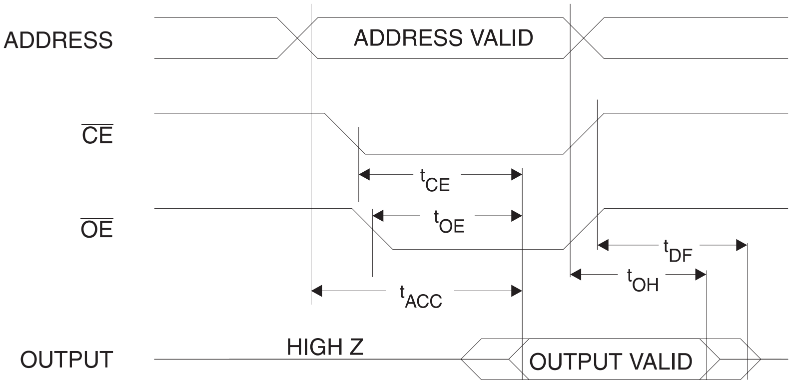
8. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		50	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		15	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.0		V

9. AC Read Characteristics

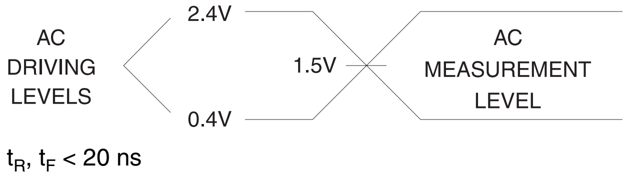
		AT28BV64B-20		
Symbol	**Parameter**	**Min**	**Max**	**Units**
t_{ACC}	Address to Output Delay		200	ns
t_{CE}(1)	$\overline{\mathrm{CE}}$ to Output Delay		200	ns
t_{OE}(2)	$\overline{\mathrm{OE}}$ to Output Delay	0	80	ns
t_{DF}(3)(4)	$\overline{\mathrm{CE}}$ or $\overline{\mathrm{OE}}$ to Output Float	0	55	ns
t_{OH}	Output Hold from $\overline{\mathrm{OE}}$, $\overline{\mathrm{CE}}$ or Address, Whichever Occurred First	0		ns

10. AC Read Waveforms(1)(2)(3)(4)

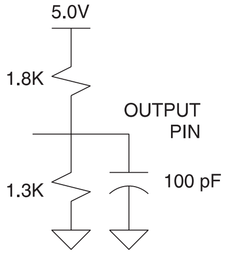


Notes:
1. $\overline{\mathrm{CE}}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{\mathrm{OE}}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{\mathrm{CE}}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{\mathrm{OE}}$ or $\overline{\mathrm{CE}}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



13. Pin Capacitance

f = 1 MHz, T = 25°C(1)

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

14. AC Write Characteristics

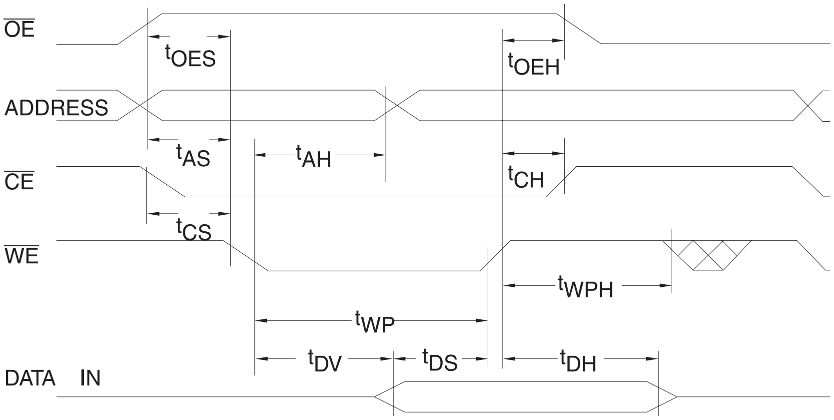
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{\text{OE}}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{\text{WE}}$ or $\overline{\text{CE}}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{\text{OE}}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR(1)		
t_{WPH}	Write Pulse Width High	100		ns

Notes: 1. NR = No Restriction

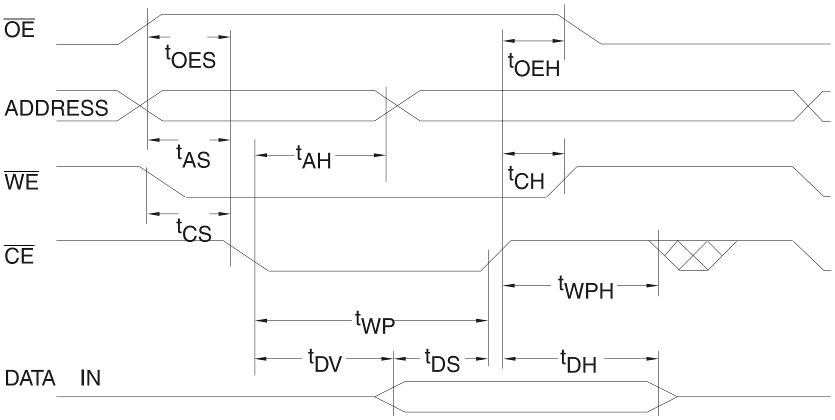
2. All byte write operations must be preceded by the SDP command sequence.

15. AC Write Waveforms

15.1 $\overline{\text{WE}}$ Controlled



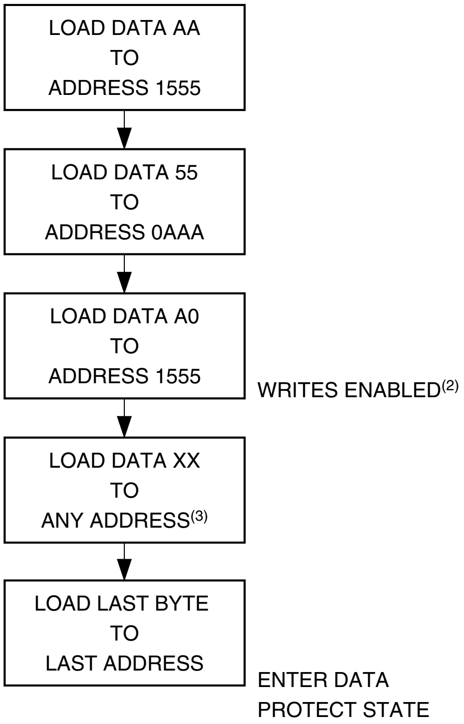
15.2 $\overline{\text{CE}}$ Controlled



16. Page Mode Characteristics

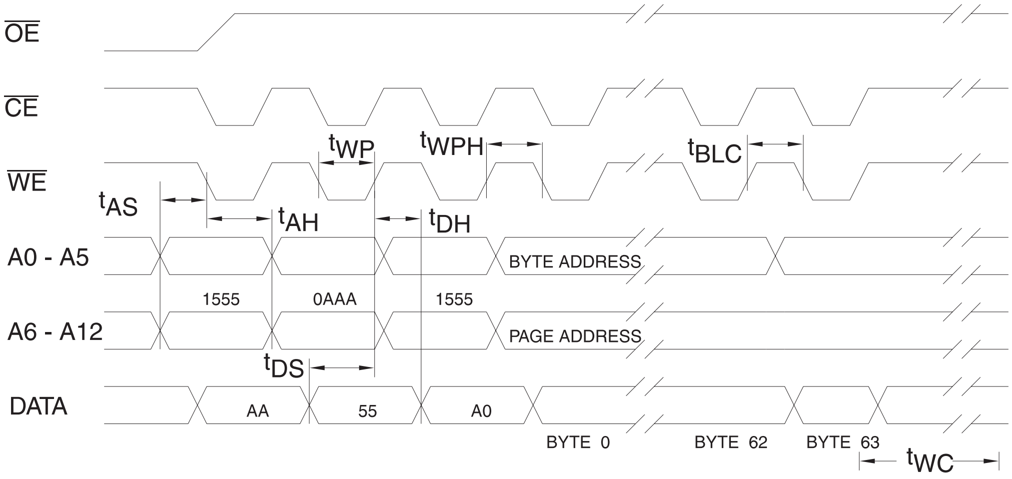
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		100	µs
t_{WPH}	Write Pulse Width High	100		ns

17. Write Algorithm(1)



Notes:
1. Data Format: I/O7 - I/O0 (Hex); Address Format: A12 - A0 (Hex).
2. Data protect state will be re-activated at the end of the write cycle.
3. 1 to 64 bytes of data are loaded.

18. Software Data Protection Write Cycle Waveforms(1)(2)(3)



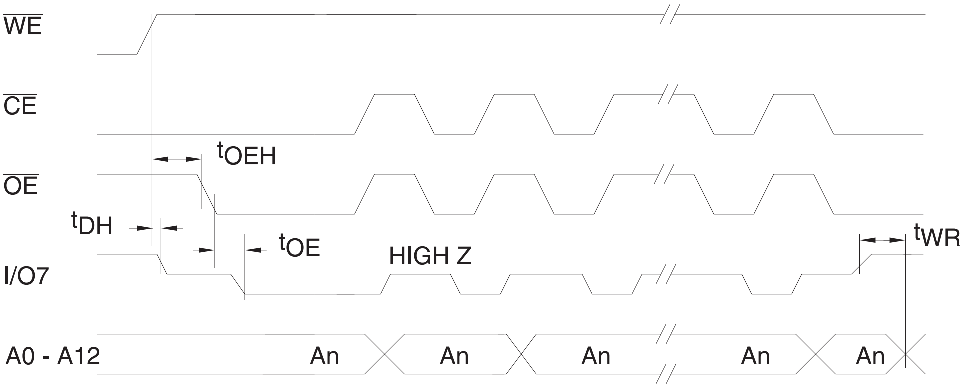
Notes:
1. A0 - A12 must conform to the addressing sequence for the first three bytes as shown above.
2. A6 through A12 must specify the same page address during each high to low transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) after the software code has been entered.
3. $\overline{\text{OE}}$ must be high only when $\overline{\text{WE}}$ and $\overline{\text{CE}}$ are both low.

19. Data Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	0			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes:
1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

20. Data Polling Waveforms

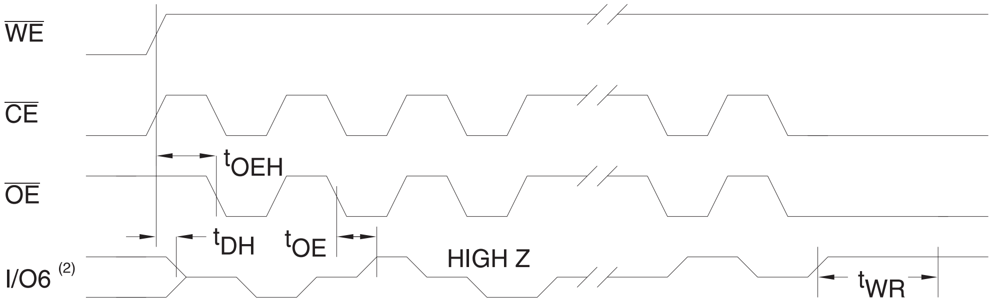


21. Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\mathrm{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\mathrm{OE}}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{\mathrm{OE}}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes:
1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

22. Toggle Bit Waveforms



Notes:
1. Toggling either $\overline{\mathrm{OE}}$ or $\overline{\mathrm{CE}}$ or both $\overline{\mathrm{OE}}$ and $\overline{\mathrm{CE}}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used, but the address should not vary.

23. Ordering Information[1]

23.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.05	AT28BV64B-20JI AT28BV64B-20PI AT28BV64B-20SI AT28BV64B-20TI	32J 28P6 28S 28T	Industrial (-40° C to 85° C)

Note: 1. See "Valid Part Numbers" below.

23.2 Green Package Option (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	15	0.05	AT28BV64B-20JU AT28BV64B-20TU AT28BV64B-20SU	32J 28T 28S	Industrial (-40° C to 85° C)

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)

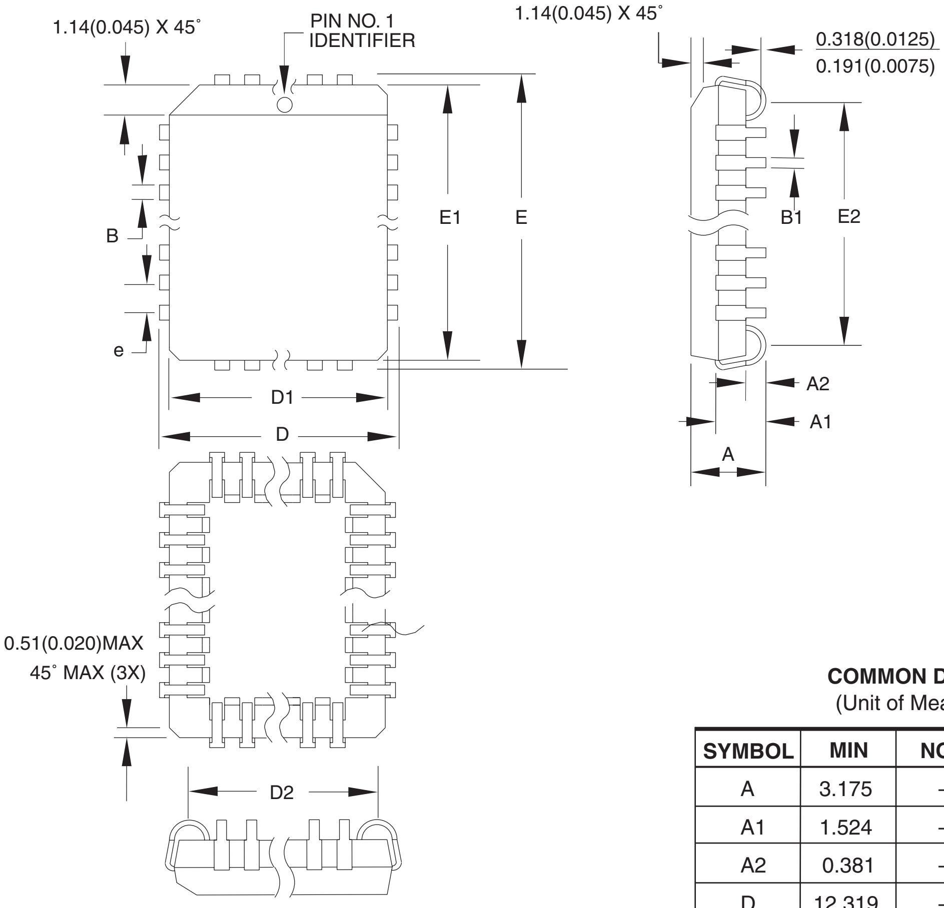
24. Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28BV64B	20	JI, JU, PI, SI, SU, TI, TU

25. Packaging Information

25.1 32J – PLCC



Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

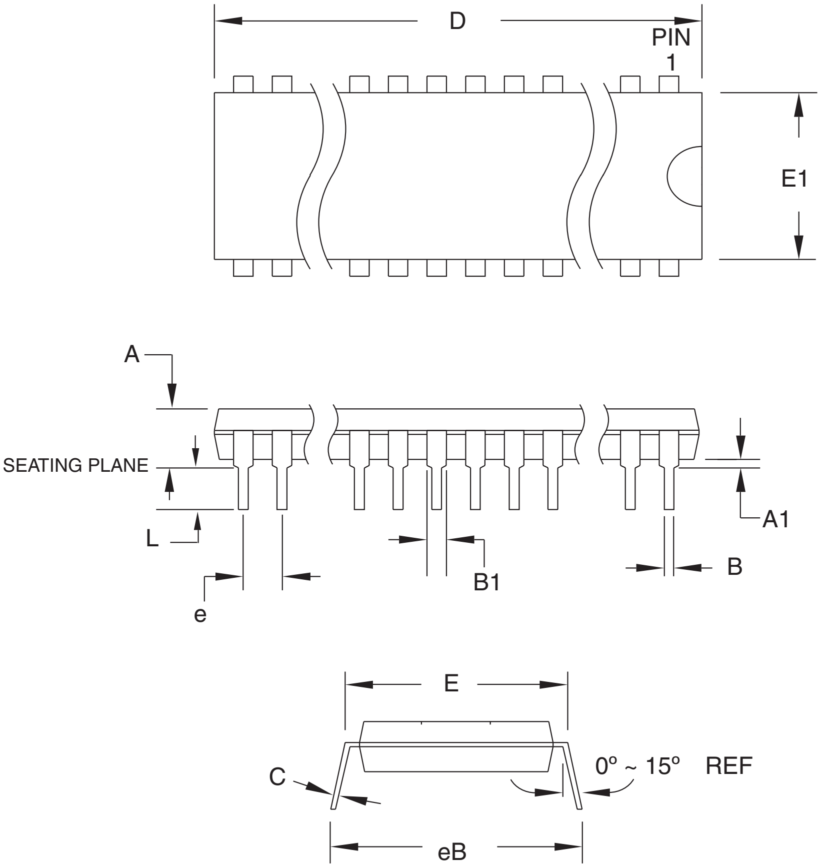
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

10/04/01

	TITLE	**DRAWING NO.**	**REV.**
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

25.2 28P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	36.703	–	37.338	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AB.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

2325 Orchard Parkway
San Jose, CA 95131

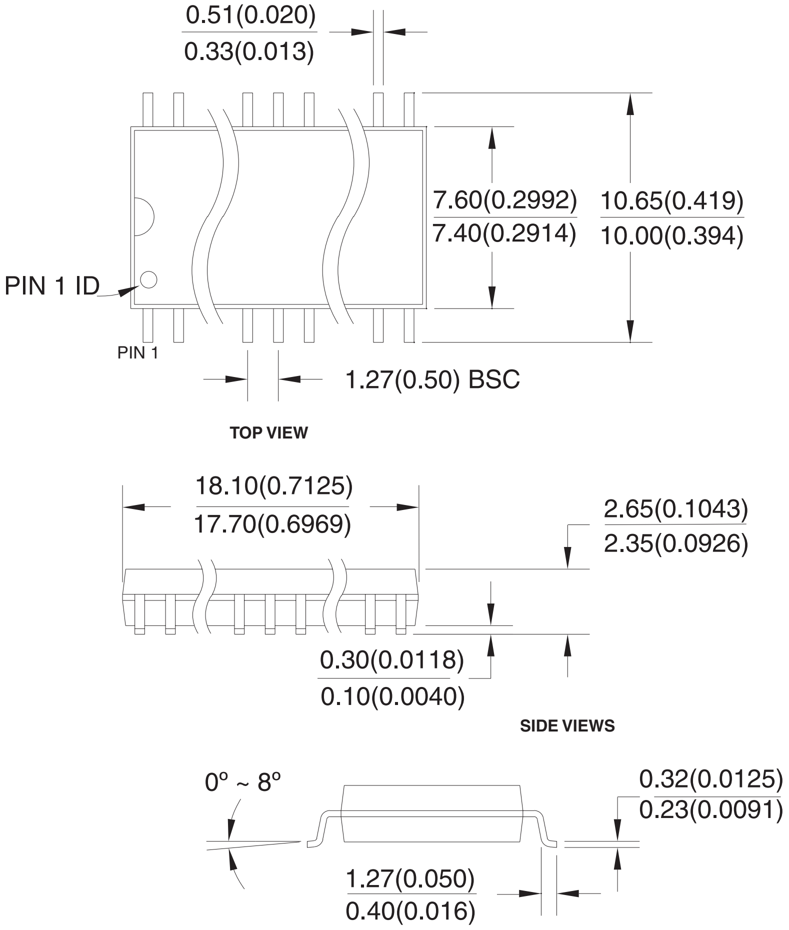
TITLE
28P6, 28-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)

DRAWING NO.
28P6

REV.
B

25.3 28S – SOIC

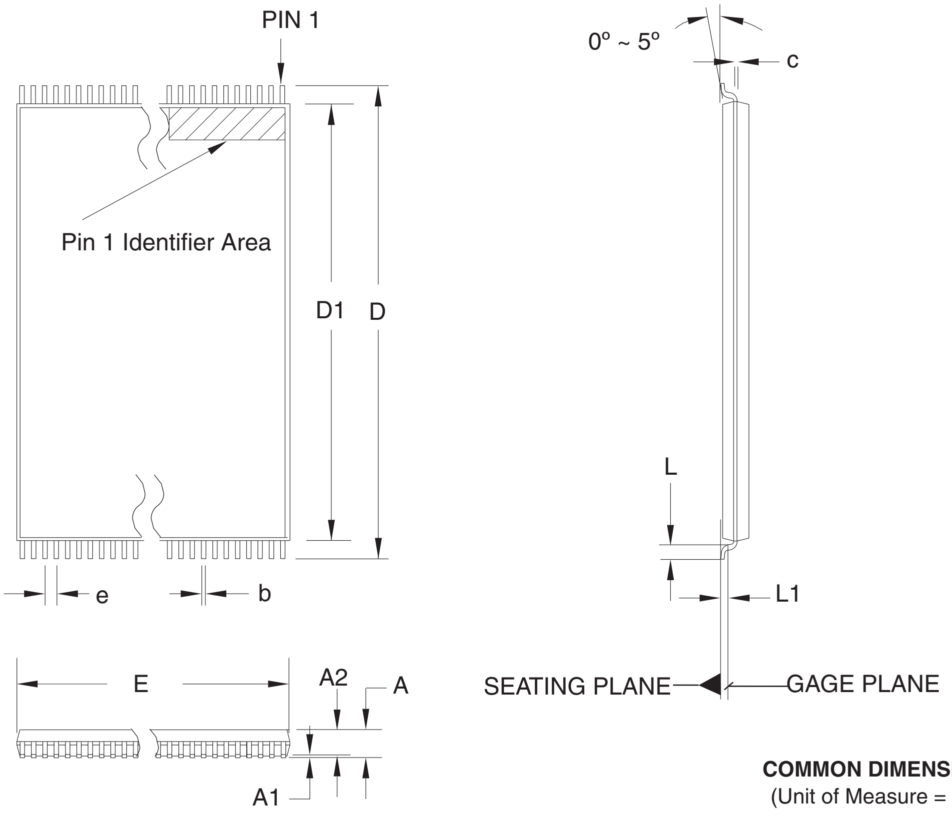
Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.



8/4/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28S**, 28-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC) JEDEC Standard MS-013	28S	B

25.4 28T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.55 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

12/06/02

2325 Orchard Parkway
San Jose, CA 95131

TITLE
28T, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)

DRAWING NO.
28T

REV.
C

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