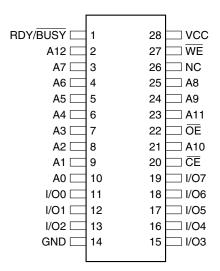
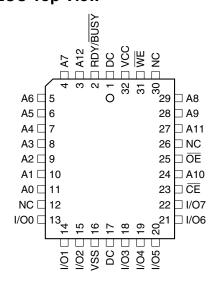
## 2. Pin Configurations

Pin Name	Function
A0 - A12	Addresses
CE	Chip Enable
ŌĒ	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/BUSY	Ready/Busy Output
NC	No Connect
DC	Don't Connect

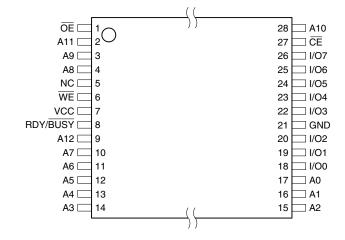
### 2.2 PDIP, SOIC Top View



### 2.1 PLCC Top View

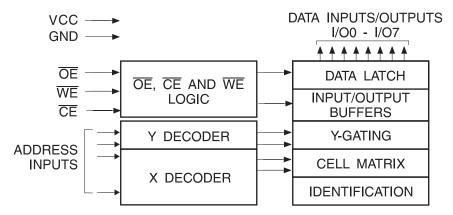


### 2.3 TSOP Top View





## 3. Block Diagram



## 4. Absolute Maximum Ratings\*

Temperature Under Bias55°C to +125°C
Storage Temperature65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground0.6V to +6.25V
All Output Voltages with Respect to Ground0.6V to V <sub>CC</sub> + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground0.6V to +13.5V

\*NOTICE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability





### 5. Device Operation

#### 5.1 Read

The AT28BV64 is accessed like a Static RAM. When  $\overline{CE}$  and  $\overline{OE}$  are low and  $\overline{WE}$  is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever  $\overline{CE}$  or  $\overline{OE}$  is high. This dual line control gives designers increased flexibility in preventing bus contention.

### 5.2 Byte Write

Writing data into the AT28BV64 is similar to writing into a Static RAM. A low pulse on the  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$  input with  $\overline{\text{OE}}$  high and  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  low (respectively) initiates a byte write. The address location is latched on the falling edge of  $\overline{\text{WE}}$  (or  $\overline{\text{CE}}$ ); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of  $t_{\text{WC}}$ , a read operation will effectively be a polling operation.

#### 5.3 READY/BUSY

Pin 1 is an open drain READY/BUSY output that can be used to detect the end of a write cycle. RDY/BUSY is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/BUSY line.

### 5.4 DATA Polling

The AT28BV64 provides  $\overline{\text{DATA}}$  Polling to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O<sub>7</sub> (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

#### 5.5 Write Protection

Inadvertent writes to the device are protected against in the following ways: (a)  $V_{CC}$  sense – if  $V_{CC}$  is below 1.8V (typical) the write function is inhibited; (b)  $V_{CC}$  power on delay – once  $V_{CC}$  has reached 2.0V the device will automatically time out 10 ms (typical) before allowing a byte write; and (c) Write Inhibit – holding any one of  $\overline{OE}$  low,  $\overline{CE}$  high or  $\overline{WE}$  high inhibits byte write cycles.

# 6. DC and AC Operating Range

	AT28BV64-30
Operating Temperature (Case)	-40°C - 85°C
V <sub>CC</sub> Power Supply	2.7V to 3.6V

# 7. Operating Modes

Mode	CE	ŌĒ	WE	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	$V_{IH}$	D <sub>OUT</sub>
Write <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Standby/Write Inhibit	V <sub>IH</sub>	X <sup>(1)</sup>	Х	High Z
Write Inhibit	Х	Х	V <sub>IH</sub>	
Write Inhibit	Х	V <sub>IL</sub>	Х	
Output Disable	Х	V <sub>IH</sub>	Х	High Z

Notes: 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.

2. Refer to AC Programming Waveforms.

## 8. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1.0V$		5	μΑ
I <sub>LO</sub>	Output Leakage Current	$V_{I/O} = 0V \text{ to } V_{CC}$		5	μΑ
$I_{SB}$	V <sub>CC</sub> Standby Current CMOS	$\overline{\text{CE}} = V_{\text{CC}} - 0.3V \text{ to } V_{\text{CC}} + 1.0V$		50	μΑ
I <sub>CC</sub>	V <sub>CC</sub> Active Current AC	$f = 5 \text{ MHz}; I_{OUT} = 0 \text{ mA}; CE = V_{IL}$		8	mA
V <sub>IL</sub>	Input Low Voltage			0.6	V
V <sub>IH</sub>	Input High Voltage		2.0		V
V	Output Low Voltage	I <sub>OL</sub> = 1 mA		0.3	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2 \text{ mA for RDY/}\overline{BUSY}$		0.3	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -100 μA	2.0		V

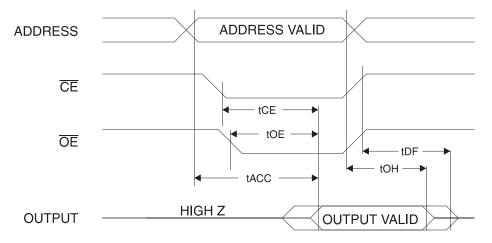




#### 9. AC Read Characteristics

		AT28B		
Symbol	Parameter	Min	Max	Units
t <sub>ACC</sub>	Address to Output Delay		300	ns
t <sub>CE</sub> <sup>(1)</sup>	CE to Output Delay		300	ns
t <sub>OE</sub> <sup>(2)</sup>	OE to Output Delay	0	150	ns
t <sub>DF</sub> <sup>(3)(4)</sup>	CE or OE High to Output Float	0	60	ns
t <sub>OH</sub>	Output Hold from OE, CE or Address, whichever occurred first	0		ns

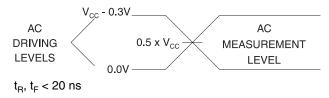
# 10. AC Read Waveforms<sup>(1)(2)(3)(4)</sup>



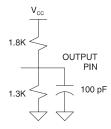
Notes: 1.  $\overline{\text{CE}}$  may be delayed up to  $t_{\text{ACC}}$  -  $t_{\text{CE}}$  after the address transition without impact on  $t_{\text{ACC}}$ .

- 2.  $\overline{\text{OE}}$  may be delayed up to  $t_{\text{CE}}$   $t_{\text{OE}}$  after the falling edge of  $\overline{\text{CE}}$  without impact on  $t_{\text{CE}}$  or by  $t_{\text{ACC}}$   $t_{\text{OE}}$  after an address change without impact on  $t_{\text{ACC}}$ .
- 3.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$  whichever occurs first (C<sub>L</sub> = 5 pF).
- 4. This parameter is characterized and is not 100% tested.

## 11. Input Test Waveforms and Measurement Level



## 12. Output Test Load



## 13. Pin Capacitance

 $f = 1 \text{ MHz}, T = 25^{\circ}C^{(1)}$ 

Symbol	Тур	Max Units		Conditions
C <sub>IN</sub>	4	6	pF	$V_{IN} = 0V$
C <sub>OUT</sub>	8	12	pF	$V_{OUT} = 0V$

Note: 1. This parameter is characterized and is not 100% tested.



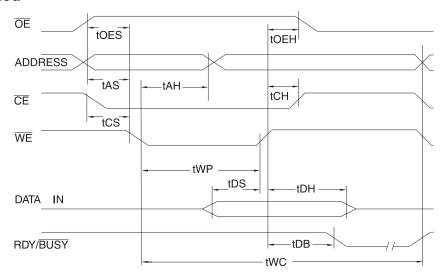


## 14. AC Write Characteristics

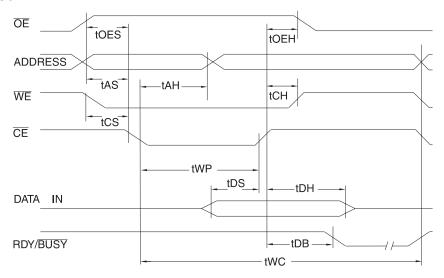
Symbol	Parameter	Min	Max	Units
t <sub>AS</sub> , t <sub>OES</sub>	Address, OE Set-up Time	10		ns
t <sub>AH</sub>	Address Hold Time	100		ns
t <sub>WP</sub>	Write Pulse Width (WE or CE)	150	1000	ns
t <sub>DS</sub>	Data Set-up Time	100		ns
t <sub>DH</sub> , t <sub>OEH</sub>	Data, OE Hold Time	10		ns
t <sub>DB</sub>	Time to Device Busy		50	ns
t <sub>WC</sub>	Write Cycle Time		3	ms

## 15. AC Write Waveforms

## 15.1 WE Controlled



### 15.2 CE Controlled



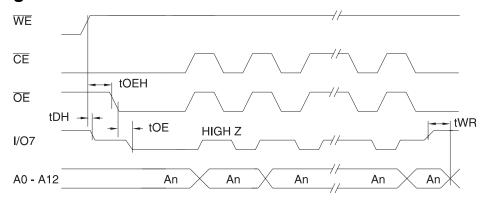
# 16. Data Polling Characteristics<sup>(1)</sup>

Symbol	Parameter	Min	Тур	Max	Units
t <sub>DH</sub>	Data Hold Time	10			ns
t <sub>OEH</sub>	OE Hold Time	10			ns
t <sub>OE</sub>	ŌĒ to Output Delay <sup>(2)</sup>				ns
t <sub>WR</sub>	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

2. See AC Characteristics.

# 17. Data Polling Waveforms







## 18. Ordering Information

## 18.1 Standard Package<sup>(1)</sup>

t <sub>ACC</sub>	I <sub>CC</sub> (mA) Operating					
(ns)	Active	Standby	Voltage	Ordering Code	Package	Operation Range
				AT28BV64-30JI	32J	
300	8	0.05	2.7V to 3.6V	AT28BV64-30PI	28P6	Industrial
300	0	0.05	2.7 V 10 3.6 V	AT28BV64-30SI	28S	(-40° C to 85° C)
				AT28BV64-30TI	28T	

Note: 1. See Valid Part Number table below.

	Package Type				
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)				
28P6	28P6 28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)				
28S	28S 28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)				
28T	28-lead, Plastic Thin Small Outline Package (TSOP)				

#### 18.2 Valid Part Number

The following table lists standard Atmel® products that can be ordered.

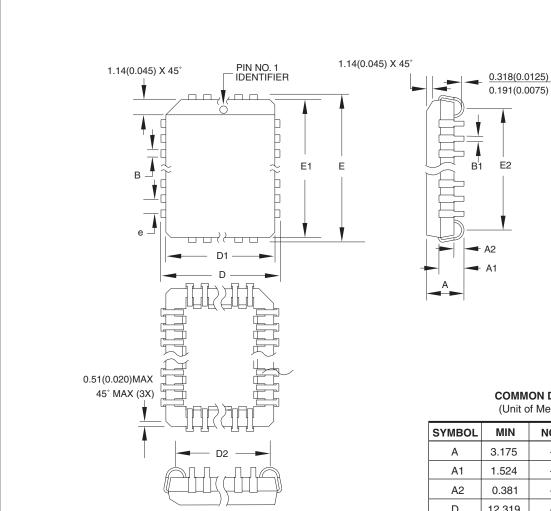
Device Numbers	Speed	Package and Temperature Combinations
AT28BV64	30	JI, PI, SI, TI

### 19. Die Products

Reference Section: Parallel EEPROM Die Products

## 20. Packaging Information

### 20.1 32J - PLCC



Notes:

- 1. This package conforms to JEDEC reference MS-016, Variation AE.
- Dimensions D1 and E1 do not include mold protrusion.
   Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
- 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

### COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
Α	3.175	_	3.556	
A1	1.524	_	2.413	
A2	0.381	_	_	
D	12.319	_	12.573	
D1	11.354	_	11.506	Note 2
D2	9.906	_	10.922	
E	14.859	_	15.113	
E1	13.894	_	14.046	Note 2
E2	12.471	_	13.487	
В	0.660	_	0.813	
B1	0.330	_	0.533	
е	1.270 TYP			

10/04/01

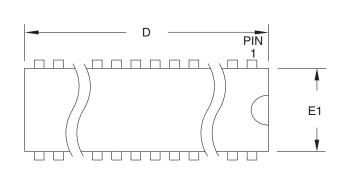
<b>32J</b> , 32-lead, Pla	stic J-leaded Chip	Carrier (PLCC)

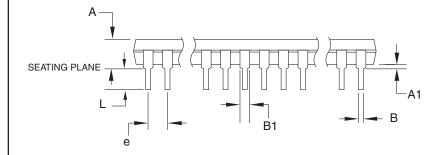
DRAWING N	O. REV.
32J	В

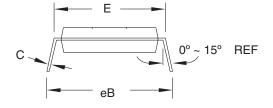




#### 20.2 28P6 - PDIP







Notes:

- 1. This package conforms to JEDEC reference MS-011, Variation AB.
- Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

#### **COMMON DIMENSIONS**

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
Α	_	_	4.826	
A1	0.381	_	ı	
D	36.703	_	37.338	Note 2
Е	15.240	_	15.875	
E1	13.462	_	13.970	Note 2
В	0.356	_	0.559	
B1	1.041	_	1.651	
L	3.048	_	3.556	
С	0.203	_	0.381	
еВ	15.494	_	17.526	
е	2.540 TYP			

09/28/01

		TITLE	DRAWING NO.	REV.
<u>am</u>	2325 Orchard Parkway San Jose, CA 95131	<b>28P6</b> , 28-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	28P6	В

AT28BV64

12

#### 20.3 28S - SOIC

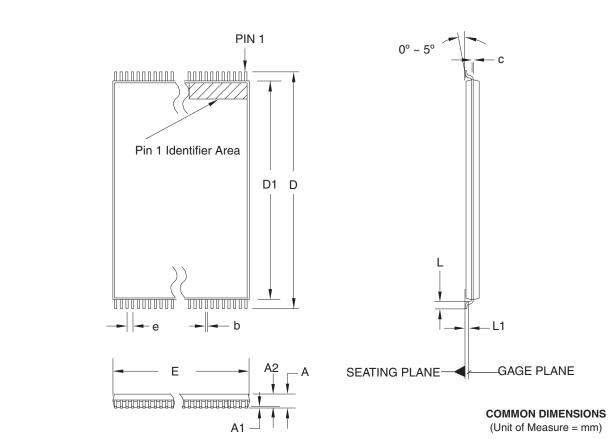
Dimensions in Millimeters and (Inches). Controlling dimension: Millimeters. 0.51(0.020) 0.33(0.013) 7.60(0.2992) 10.65(0.419) 7.40(0.2914)  $\overline{10.00(0.394)}$ PIN 1 ID 1.27(0.50) BSC TOP VIEW 18.10(0.7125) 2.65(0.1043) 17.70(0.6969) 2.35(0.0926) 0.30(0.0118) 0.10(0.0040) SIDE VIEWS 0° ~ 8° 0.32(0.0125) 0.23(0.0091) 1.27(0.050) 0.40(0.016) 8/4/03 DRAWING NO. TITLE REV. 2325 Orchard Parkway 28S, 28-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC) **28S** В San Jose, CA 95131



JEDEC Standard MS-013



#### 20.4 28T - TSOP



Notes:

- 1. This package conforms to JEDEC reference MO-183.
- 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
- 3. Lead coplanarity is 0.10 mm maximum.

(				
MIN	NOM	MAX	NOTE	
-	-	1.20		
0.05	-	0.15		
0.90	1.00	1.05		
13.20	13.40	13.60		
11.70	11.80	11.90	Note 2	
7.90	8.00	8.10	Note 2	
0.50	0.60	0.70		
0.25 BASIC				
0.17	0.22	0.27		
0.10	_	0.21		
0.55 BASIC				
	- 0.05 0.90 13.20 11.70 7.90 0.50	0.05 - 0.90 1.00 13.20 13.40 11.70 11.80 7.90 8.00 0.50 0.60 0.25 BASIC 0.17 0.22 0.10 -	-         -         1.20           0.05         -         0.15           0.90         1.00         1.05           13.20         13.40         13.60           11.70         11.80         11.90           7.90         8.00         8.10           0.50         0.60         0.70           0.25 BASIC           0.17         0.22         0.27           0.10         -         0.21	

12/06/02

TITLE		DRAWING NO.	REV.
2 C A 05121 I -	, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline kage, Type I (TSOP)	28T	С



#### Headquarters

Atmel Corporation

2325 Orchard Parkway San Jose, CA 95131 USA

Tel: 1(408) 441-0311 Fax: 1(408) 487-2600

#### International

Atmel Asia

Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimshatsui East Kowloon Hong Kong

Tel: (852) 2721-9778 Fax: (852) 2722-1369 Atmel Europe

France

Le Krebs 8, Rue Jean-Pierre Timbaud BP 309 78054 Saint-Quentin-en-Yvelines Cedex

Tel: (33) 1-30-60-70-00 Fax: (33) 1-30-60-71-11 Atmel Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan

Tel: (81) 3-3523-3551 Fax: (81) 3-3523-7581

#### **Product Contact**

Web Site

www.atmel.com

Technical Support eprom@atmel.com

Sales Contact

www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© 2007 Atmel Corporation. All rights reserved. Atmel<sup>®</sup>, logo and combinations thereof, and others are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.