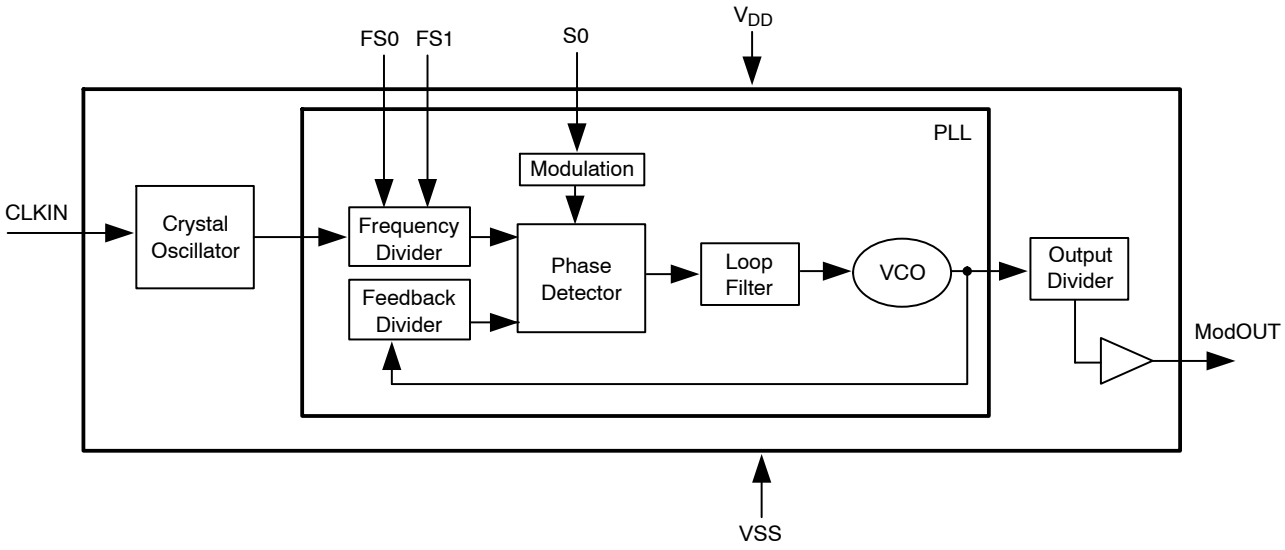


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	CLKIN	I	Connect to externally generated clock signal.
2	GND	P	Ground to entire chip.
3	S1	I	Spread range select. Digital logic input used to select frequency deviation (Refer to *Spread Deviation Table*). This pin has an internal pull−up resistor.
4	S0	I	Spread range select. Digital logic input used to select frequency deviation (Refer to *Spread Deviation Table*). This pin has an internal pull−up resistor.
5	ModOUT	O	Spread spectrum low EMI output.
6	VDD	P	Power supply for the entire chip (3.3 V).
7	FS0	I	Frequency range select. Digital logic input used to select frequency range (Refer to *Input Frequency and Modulation Rate Table*). This pin has an internal pull−up resistor.
8	FS1	I	Frequency range select. Digital logic input used to select frequency range (Refer to *Input Frequency and Modulation Rate Table*). This pin has an internal pull−up resistor.

Table 2. INPUT FREQUENCY AND MODULATION RATE TABLE

FS1 (pin 8)	FS0 (pin 7)	Frequency Range
0	0	25 MHz to 50 MHz
0	1	50 MHz to 103 MHz
1	0	75 MHz to 150 MHz
1	1	160 MHz to 210 MHz

Table 3. SPREAD DEVIATION SELECTION TABLE

		Spreading Range (±%)								
S1	S0	25 MHz	40 MHz	65 MHz	81 MHz (Note 1)	81 MHz (Note 2)	108 MHz	120 MHz	162 MHz	200 MHz
0	0	0.28	0.19	0.15	0.12	0.18	0.15	0.1	0.1	0.06
0	1	0.8	0.3	0.3	0.2	0.5	0.3	0.19	0.3	0.1
1	0	1.2	0.54	0.45	0.4	0.8	0.6	0.36	1.0	0.6
1	1	2.1	1.0	1.1	0.9	1.4	1.1	0.75	1.9	1.2

1. Frequency Range: 50 MHz to 103 MHz
2. Frequency Range: 75 MHz to 150 MHz

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage pin with respect to Ground	−0.5 to +4.6	V
V_{IN}	Input Voltage pin with respect to Ground	VSS−0.5 to VDD+0.5	V
V_{OUT}	Output Voltage pin with respect to Ground	VSS−0.5 to VDD+0.5	V
T_{STG}	Storage temperature	−55 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22−A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. RECOMMENDED OPERATING CONDITIONS

Parameter	Description	Min	Typ	Max	Unit
VDD	Operating Voltage	2.7	3.3	3.7	V
T_A	Operating Temperature (Ambient Temperature)	0		+70	°C
C_L	Load Capacitance			15	pF
C_{IN}	Input Capacitance		5		pF

Table 6. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	GND − 0.3		0.8	V
V_{IH}	Input high voltage	2.0		V_{DD} + 0.3	V
I_{IL}	Input low current			−35	μA
I_{IH}	Input high current			35	μA
V_{OL}	Output low voltage (V_{DD} = 3.3 V, I_{OL} = 20 mA)			0.4	V
V_{OH}	Output high voltage (V_{DD} = 3.3 V, I_{OH} = 20 mA)	2.5			V
I_{CC}	Dynamic supply current Normal mode (3.3 V and 10 pF loading)	8.46	12	17.78	mA
I_{DD}	Static supply current Standby mode (Note 3)		0.6		mA
V_{DD}	Operating voltage	2.7	3.3	3.7	V
t_{ON}	Power up time (first locked clock cycle after power up)		0.18		mS
Z_{OUT}	Clock out impedance		50		Ω

3. CLKIN pin is pulled low.

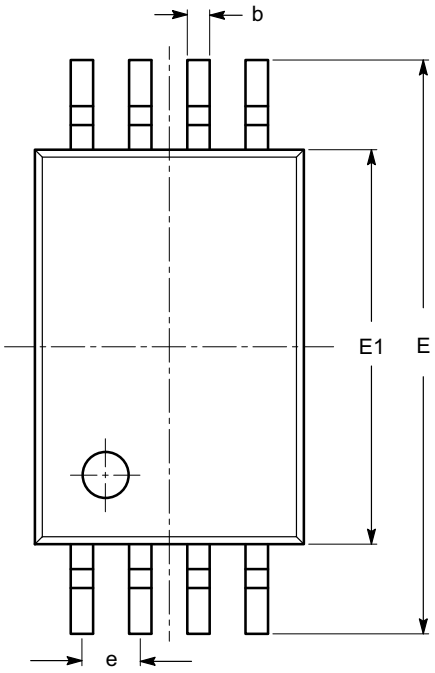
Table 7. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input frequency	25		210	MHz
ModOUT	Output frequency	25		210	MHz
t_{LH} (Note 4)	Output rise time (measured at 0.8 V to 2.0 V)	1.2	1.32	1.4	nS
t_{HL} (Note 4)	Output fall time (measured at 2.0 V to 0.8 V)	0.8	0.9	1.0	nS
t_{JC}	Jitter (cycle to cycle)			360	pS
T_D	Output duty cycle	45	50	55	%

4. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

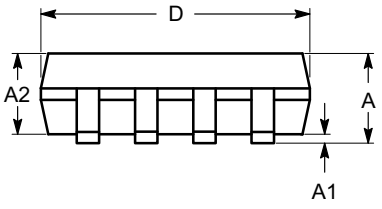
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

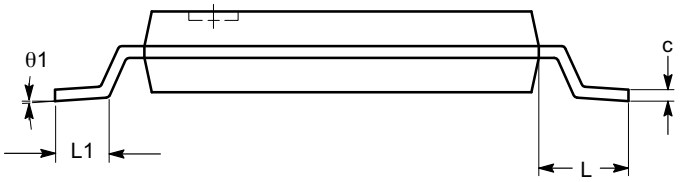


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW

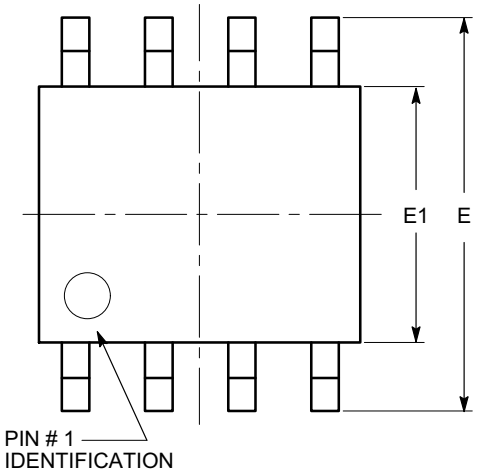


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

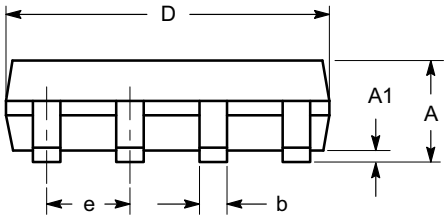
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

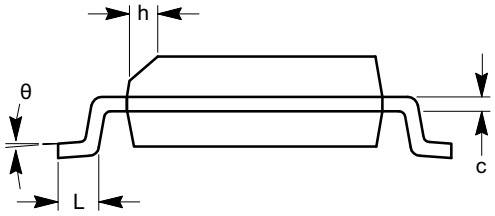


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 8. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
ASM3P2182AF−08TT	3P2182AF	8−Pin TSSOP, TUBE, Pb Free	Commercial
ASM3P2182AF−08TR	3P2182AF	8−Pin TSSOP, TAPE & REEL, Pb Free	Commercial
ASM3P2182AF−08ST	3P2182AF	8−Pin SOIC, TUBE, Pb Free	Commercial
ASM3P2182AF−08SR	3P2182AF	8−Pin SOIC, TAPE & REEL, Pb Free	Commercial
ASM3P2182A−08TT	3P2182A	8−Pin TSSOP, TUBE	Commercial
ASM3P2182A−08TR	3P2182A	8−Pin TSSOP, TAPE & REEL	Commercial
ASM3P2182A−08ST	3P2182A	8−Pin SOIC, TUBE	Commercial
ASM3P2182A−08SR	3P2182A	8−Pin SOIC, TAPE & REEL	Commercial
ASM3P2182AG−08TT	3P2182AG	8−Pin TSSOP, TUBE, Green	Commercial
ASM3P2182AG−08TR	3P2182AG	8−Pin TSSOP, TAPE & REEL, Green	Commercial
ASM3P2182AG−08ST	3P2182AG	8−Pin SOIC, TUBE, Green	Commercial
ASM3P2182AG−08SR	3P2182AG	8−Pin SOIC, TAPE & REEL, Green	Commercial

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