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6/13—Rev. 0 to Rev. A

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6/12—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.6 V, unless otherwise noted. Minimum and maximum values are guaranteed for T_J = −40°C to +125°C. Typical values specified are at T_J = 25°C. All limits at temperature extremes are guaranteed by correlation and characterization using standard statistical quality control (SQC), unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage	V_{IN}		2.5		5.5	V
Quiescent Current						
Shutdown	I_{QSHDN}	V_{EN} = 0 V, V_{SW} = GND		0.25	1.5	µA
Nonswitching State	I_Q	V_{FB} = 1.3 V, V_{SW} = GND, f_{SW} = 1.3 MHz and 650 kHz		700	1100	µA
Switching State[1]	I_{QSW}	f_{SW} = 1.3 MHz, V_{SW} = GND, no load		5.5	7	mA
		f_{SW} = 650 kHz, V_{SW} = GND, no load		3	4.5	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
Undervoltage Lockout Threshold		V_{IN} rising		2.33	2.5	V
		V_{IN} falling	2.0	2.20		V
OUTPUT						
Output Voltage[2]	V_{OUT}		V_{IN}		20	V
Load Regulation		V_{OUT} = 10 V, I_{LOAD} = 1 mA to 1 A		0.005		mV/mA
REFERENCE						
Feedback Voltage	V_{FB}		1.2250	1.2445	1.2650	V
Line Regulation		V_{IN} = 2.5 V to 5.5 V		0.02	0.2	%/V
ERROR AMPLIFIER						
Transconductance	G_{MEA}	ΔI = 4 µA		150		µA/V
Voltage Gain	A_V			80		dB
FB Pin Bias Current		V_{FB} = 1.245 V		1	50	nA
SWITCH (SW)						
On Resistance	R_{DSON}	I_{SW} = 1.0 A		50	100	mΩ
Adjustable Peak Current Limit[3]		R_{CL} = 154 kΩ, duty cycle = 70%	0.95	1.30	1.65	A
Maximum Adjustable Peak Current Limit[2]		R_{CL} = 61.9 kΩ, V_{IN} = 3.6 V, V_{OUT} = 15 V		4		A
Fixed Peak Current Limit[3]		ADP1614ACPZ-R7 only, duty cycle = 70%	2.50	3.10	3.60	A
SW Pin Leakage Current		V_{SW} = 20 V		0.1	10	µA
CLRES VOLTAGE[4]		ADP1614ACPZ-650-R7 and ADP1614ACPZ-1.3-R7				
		I_{CLRES} = 5 µA	1.225	1.27	1.315	V
		I_{CLRES} = 20 µA	1.18	1.22	1.25	V
OSCILLATOR						
Oscillator Frequency	f_{SW}	ADP1614ACPZ-1.3-R7 and ADP1614ACPZ-R7, V_{FREQ} ≥ 1.6 V	1.1	1.3	1.4	MHz
		ADP1614ACPZ-650-R7 and ADP1614ACPZ-R7, V_{FREQ} ≤ 0.3 V	500	650	720	kHz
Maximum Duty Cycle	D_{MAX}	COMP = open, V_{FB} = 1 V, f_{SW} = 1.3 MHz and 650 kHz	88	92		%
EN/FREQ LOGIC THRESHOLD		FREQ pin is ADP1614ACPZ-R7 only				
Input Voltage Low	V_{IL}	V_{IN} = 2.5 V to 5.5 V			0.3	V
Input Voltage High	V_{IH}	V_{IN} = 2.5 V to 5.5 V	1.6			V
EN Pin Leakage Current	I_{EN}	V_{EN} = 3.6 V		3.4	7	µA
FREQ Pin Leakage Current		V_{FREQ} = 3.6 V, V_{FB} = 1.3 V		0.005	1	µA
SOFT START (SS)						
Charging Current	I_{SS}	V_{SS} = 0 V	3.4	5.5	7	µA
SS Pin Voltage	V_{SS}	V_{FB} = 1.3 V	1.17	1.23	1.29	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
THERMAL SHUTDOWN						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis				20		°C

[1] This parameter specifies the average current when the device switches internally with the SW pins (Pin 6 and Pin 7) grounded.
[2] Guaranteed by design.
[3] Current limit is a function of duty cycle. For the adjustable current limit versions, it is also a function of the resistor on the CLRES pin. See Figure 10 through Figure 13.
[4] The CLRES pin cannot be controlled with a current source. An equivalent resistance should be used.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN, FB, FREQ to GND	−0.3 V to +6 V
CLRES to GND	−0.3 V to VIN
COMP to GND	1.0 V to 1.6 V
SS to GND	−0.3 V to +1.3 V
SW to GND	21 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination.

THERMAL RESISTANCE

The junction-to-ambient thermal resistance (θ_{JA}) of the package is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, attention to thermal board design is required. The value of θ_{JA} may vary, depending on the printed circuit board (PCB) material, layout, and environmental conditions.

The boundary conditions for the thermal resistance of the ADP1614 are modeled under natural convection cooling at 25°C ambient temperature, JESD 51-9, and 1 W power input on a 4-layer board.

Table 3. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead LFCSP	47	7.22	°C/W

[1] Thermal numbers per JEDEC standard JESD 51-9.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

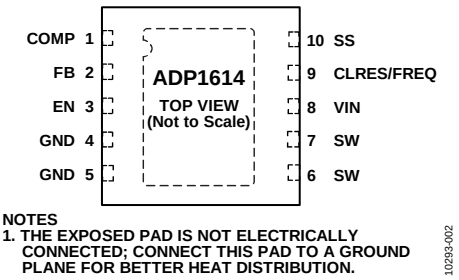


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMP	Compensation Input. Connect a series resistor-capacitor network from COMP to GND to compensate the regulator.
2	FB	Output Voltage Feedback Input. Connect a resistive voltage divider from the output voltage to FB to set the regulator output voltage.
3	EN	Enable Input. Drive EN low to shut down the regulator; drive EN high to turn on the regulator.
4, 5	GND	Ground.
6, 7	SW	Switching Output. Connect the power inductor from the input voltage to SW and connect the external rectifier from SW to the output voltage to complete the step-up converter.
8	VIN	Main Power Supply Input. VIN powers the ADP1614 internal circuitry. Connect VIN to the input source voltage. Bypass VIN to GND with a 10 µF or greater capacitor as close to the ADP1614 as possible.
9	CLRES/FREQ	Current-Limit Resistor (CLRES). Connect a resistor to GND to set the peak inductor current. Frequency Setting Input (FREQ). Connect FREQ to GND to program the oscillator to 650 kHz, or connect FREQ to VIN to program it to 1.3 MHz. Do not leave this pin floating.
10	SS	Soft Start. A capacitor connected from SS to GND brings up the output slowly at power-up and reduces inrush current.
11	EP	Exposed Die Attach Pad. The exposed pad is not electrically connected; connect this pad to a ground plane for better heat distribution.

TYPICAL PERFORMANCE CHARACTERISTICS

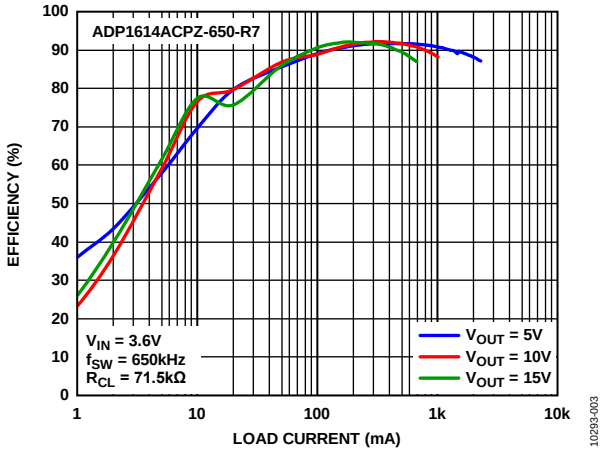


Figure 4. Efficiency vs. Load Current, V_{IN} = 3.6 V, f_{SW} = 650 kHz

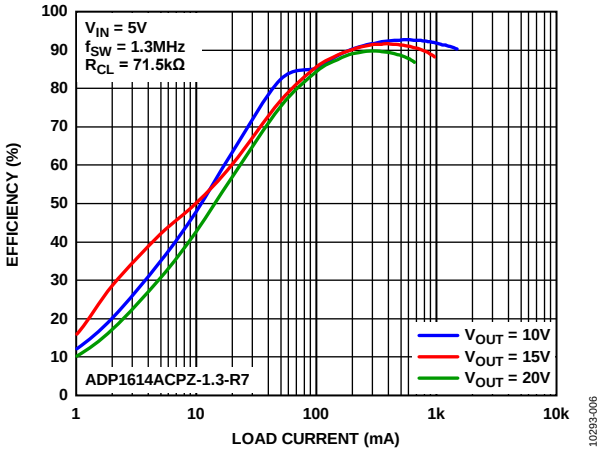


Figure 7. Efficiency vs. Load Current, V_{IN} = 5 V, f_{SW} = 1.3 MHz

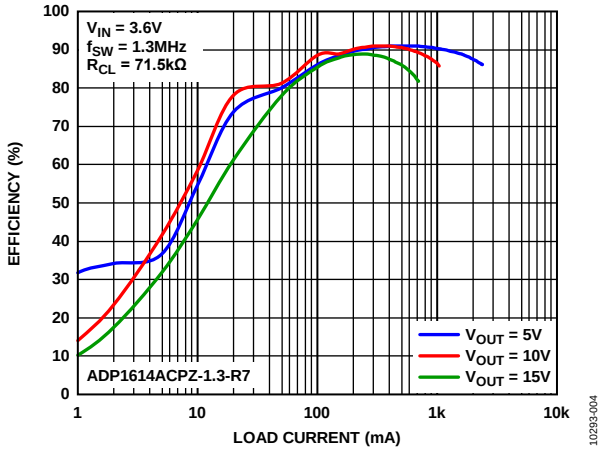


Figure 5. Efficiency vs. Load Current, V_{IN} = 3.6 V, f_{SW} = 1.3 MHz

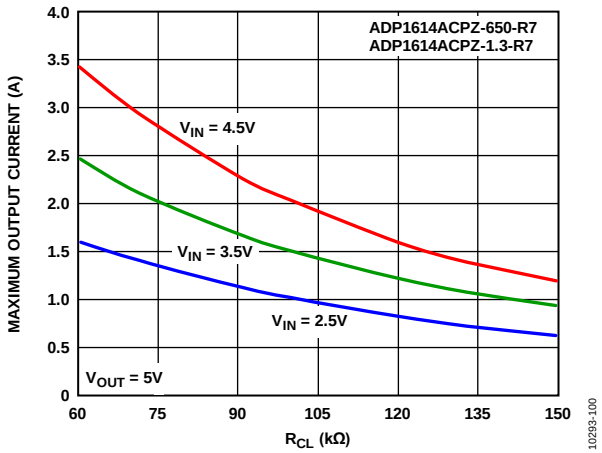


Figure 8. Typical Maximum Continuous Output Current vs. R_{CL}, V_{OUT} = 5 V

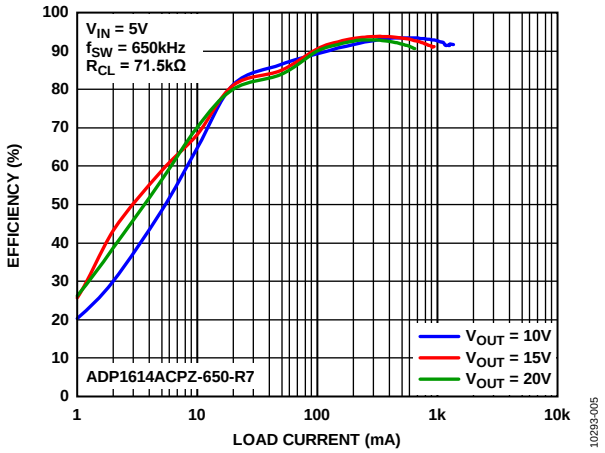


Figure 6. Efficiency vs. Load Current, V_{IN} = 5 V, f_{SW} = 650 kHz

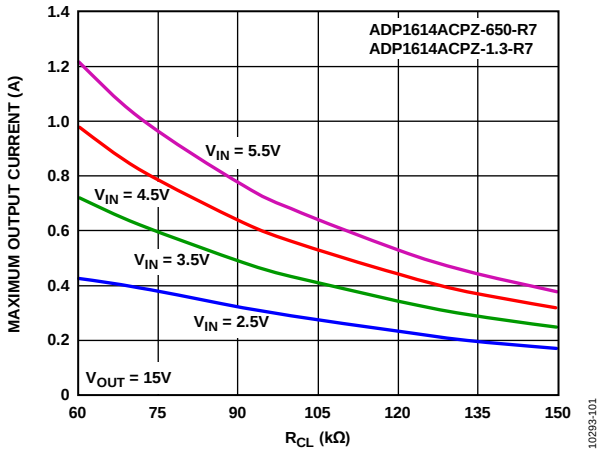


Figure 9. Typical Maximum Continuous Output Current vs. R_{CL}, V_{OUT} = 15 V

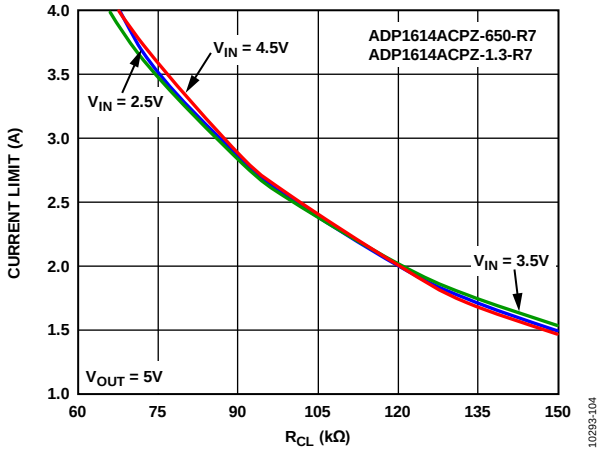


Figure 10. Peak Current Limit of Switch vs. R_{CL}, V_{OUT} = 5 V

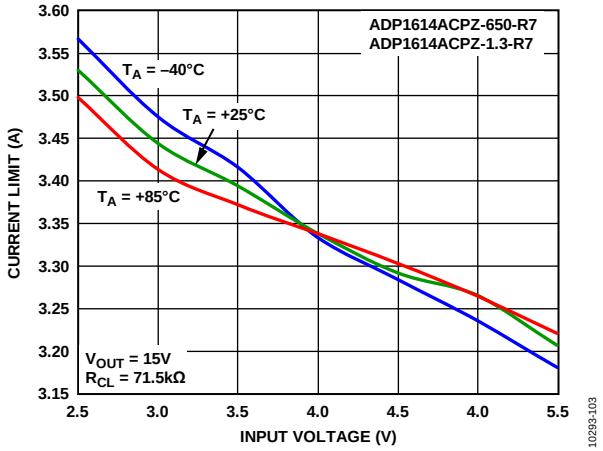


Figure 13. Peak Current Limit of Switch vs. V_{IN} over Temperature, V_{OUT} = 15 V

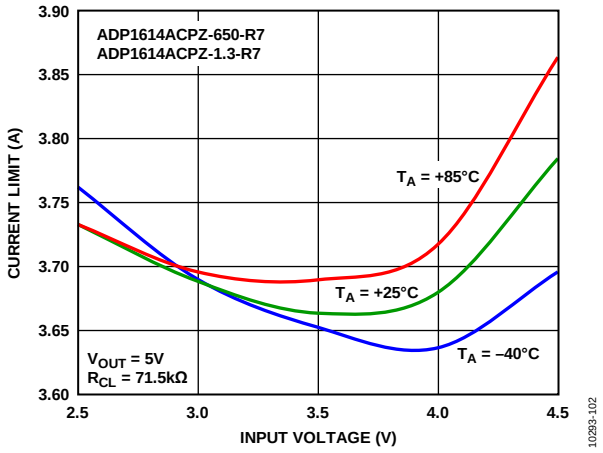


Figure 11. Peak Current Limit of Switch vs. V_{IN} over Temperature, V_{OUT} = 5 V

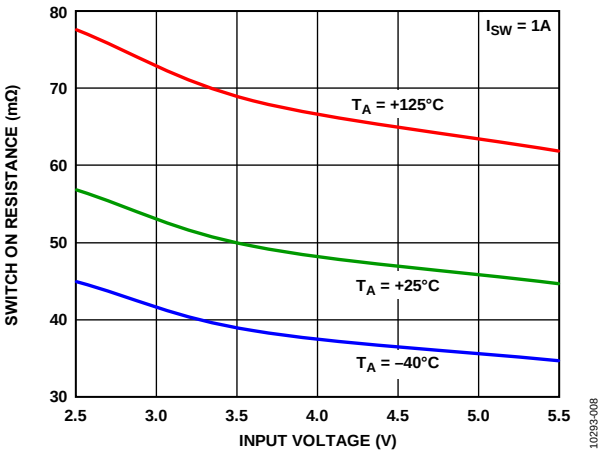


Figure 14. Switch On Resistance vs. Input Voltage

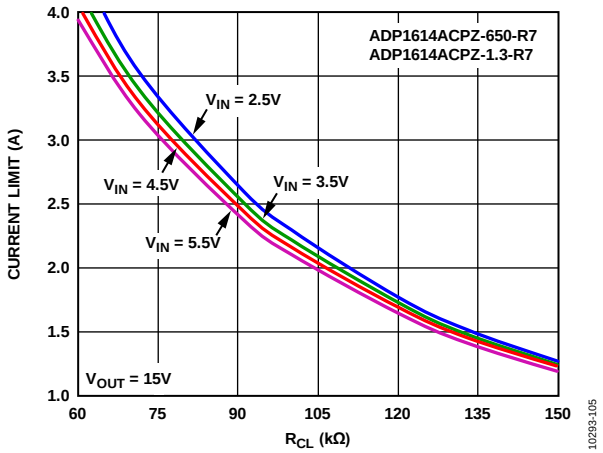


Figure 12. Peak Current Limit of Switch vs. R_{CL}, V_{OUT} = 15 V

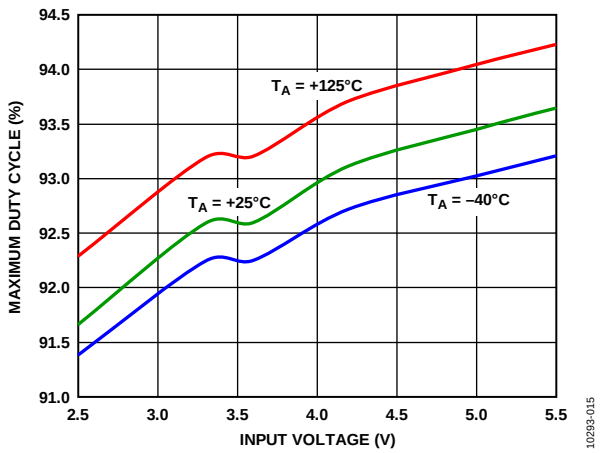


Figure 15. Maximum Duty Cycle vs. Input Voltage

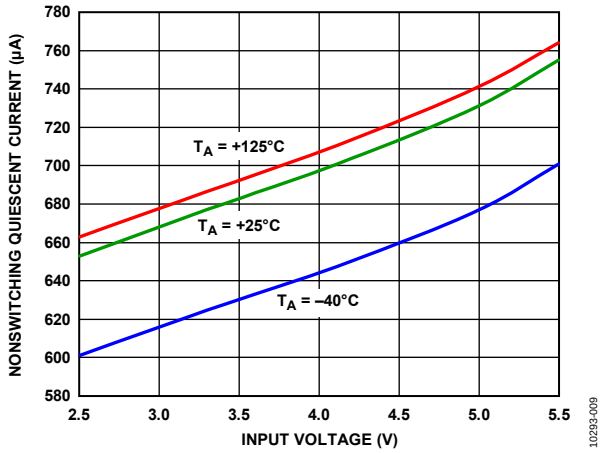


Figure 16. Nonswitching Quiescent Current vs. Input Voltage

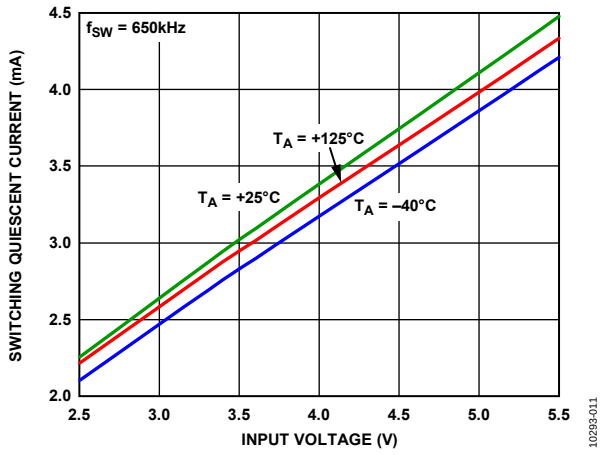


Figure 17. Switching Quiescent Current vs. Input Voltage, f_{SW} = 650 kHz

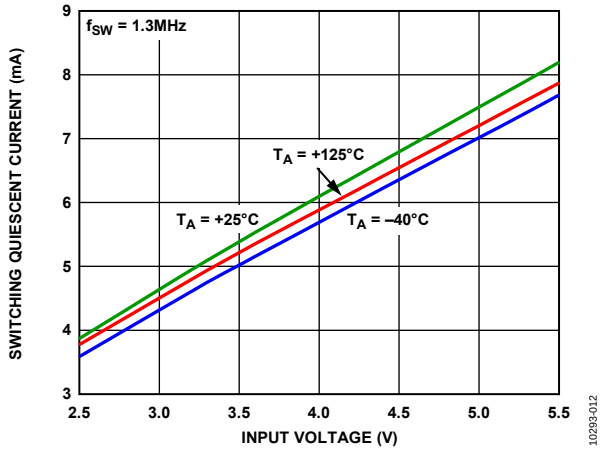


Figure 18. Switching Quiescent Current vs. Input Voltage, f_{SW} = 1.3 MHz

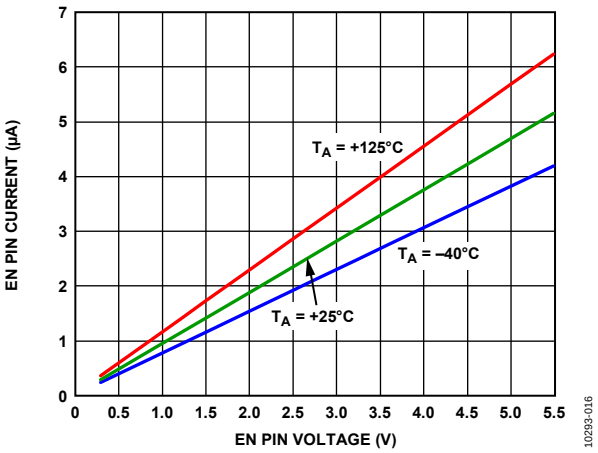


Figure 19. EN Pin Current vs. EN Pin Voltage

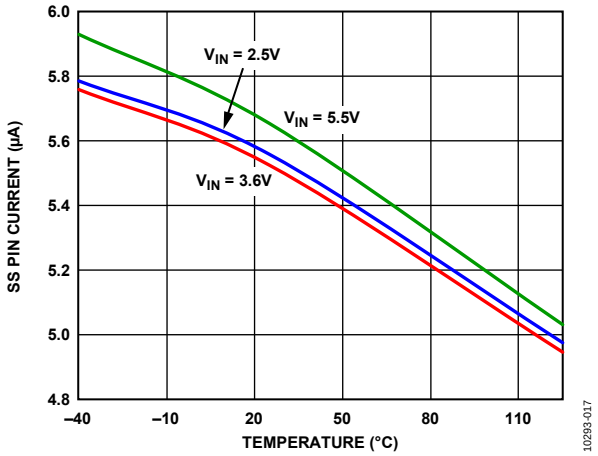


Figure 20. SS Pin Current vs. Temperature

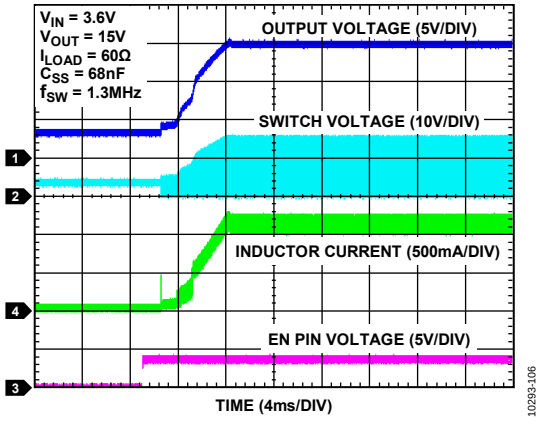


Figure 21. Startup, C_{SS} = 68 nF

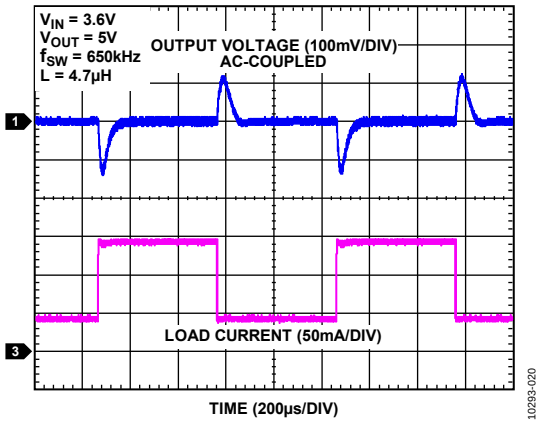


Figure 22. 50 mA to 150 mA Load Transient, V_{IN} = 3.6 V, V_{OUT} = 5 V, f_{SW} = 650 kHz

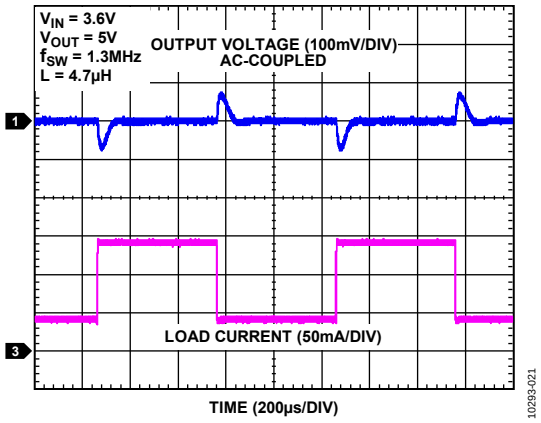


Figure 23. 50 mA to 150 mA Load Transient, V_{IN} = 3.6 V, V_{OUT} = 5 V, f_{SW} = 1.3 MHz

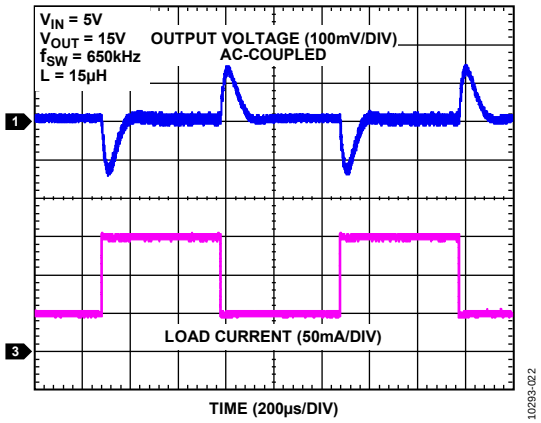


Figure 24. 50 mA to 150 mA Load Transient, V_{IN} = 5 V, V_{OUT} = 15 V, f_{SW} = 650 kHz

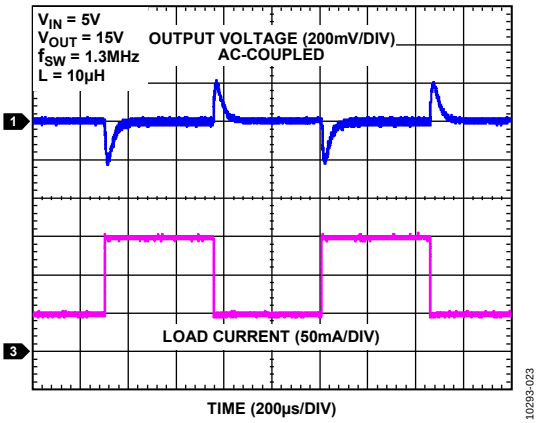


Figure 25. 50 mA to 150 mA Load Transient, V_{IN} = 5 V, V_{OUT} = 15 V, f_{SW} = 1.3 MHz

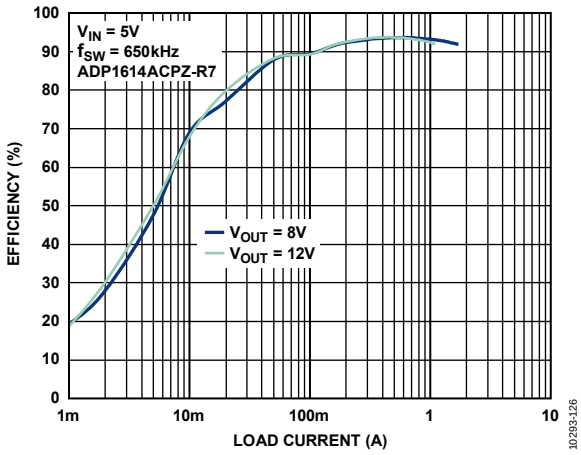


Figure 26. Efficiency vs. Load Current, V_{IN} = 5 V, f_{SW} = 650 kHz

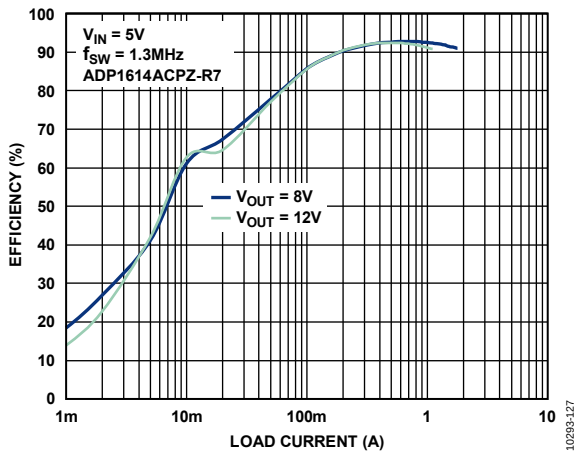


Figure 27. Efficiency vs. Load Current, V_{IN} = 5 V, f_{SW} = 1.3 MHz

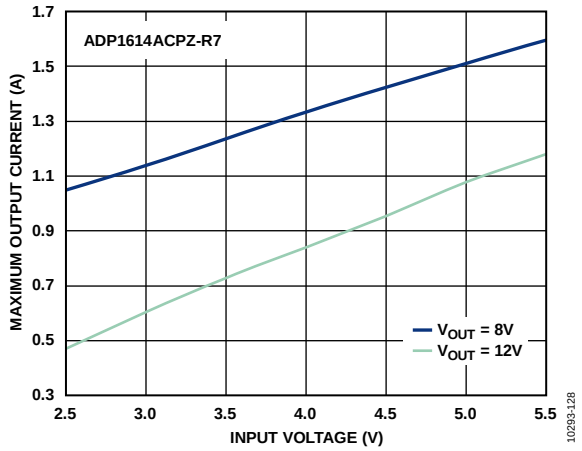


Figure 28. Typical Maximum Continuous Output Current vs. V_{IN}

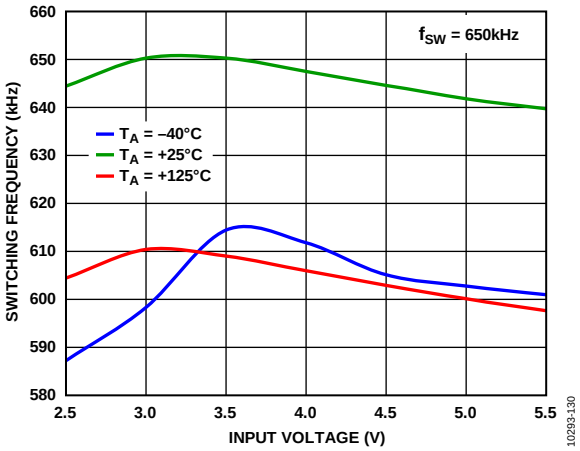


Figure 30. Frequency vs. Input Voltage, f_{SW} = 650 kHz

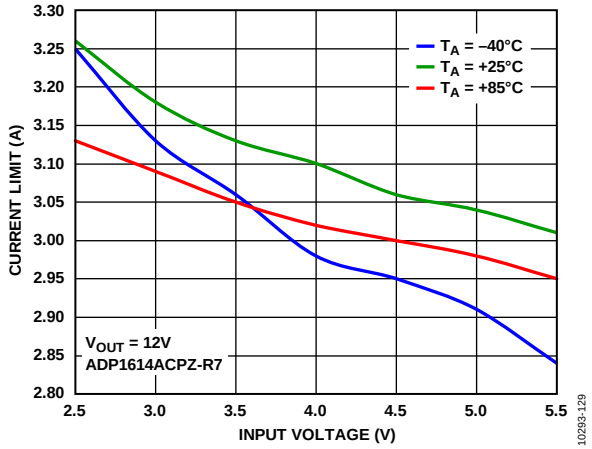


Figure 29. Peak Current Limit of Switch vs. V_{IN} over Temperature, V_{OUT} = 12 V

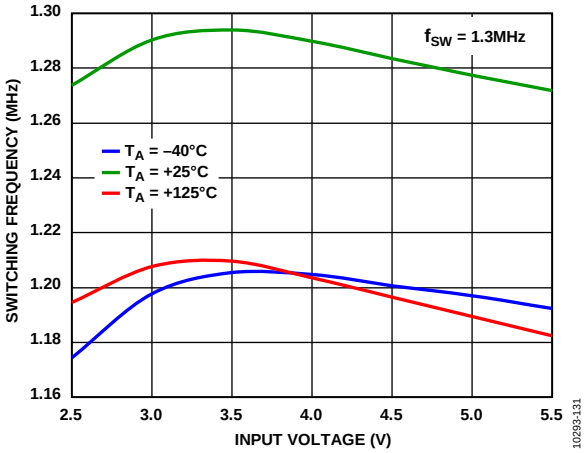
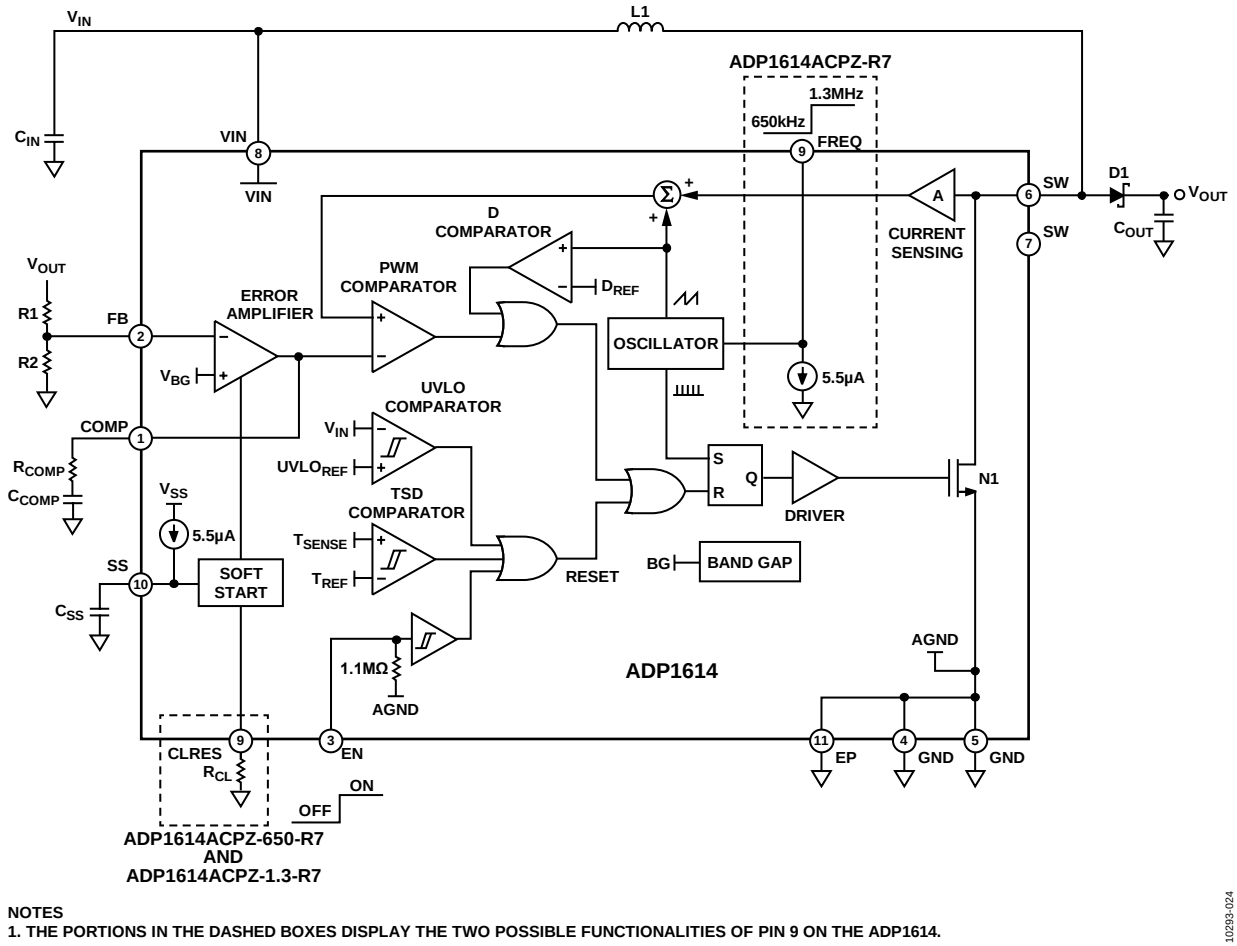


Figure 31. Frequency vs. Input Voltage, f_{SW} = 1.3 MHz

THEORY OF OPERATION

The ADP1614 current-mode, step-up switching converter boosts a 2.5 V to 5.5 V input voltage to an output voltage as high as 20 V. The internal switch allows a high output current, and the 650 kHz/1.3 MHz switching frequency allows the use of tiny external components. The switch current is monitored on a pulse-by-pulse basis to limit the current to the value set by the R_{CL} resistor on the CLRES pin on the adjustable current-limit version or to 3 A typical on the fixed current-limit version.



NOTES
1. THE PORTIONS IN THE DASHED BOXES DISPLAY THE TWO POSSIBLE FUNCTIONALITIES OF PIN 9 ON THE ADP1614.

Figure 32. Block Diagram with Step-Up Regulator Application Circuit

CURRENT-MODE PWM OPERATION

The ADP1614 utilizes a current-mode PWM control scheme to regulate the output voltage over all load conditions. The output voltage is monitored at FB through a resistive voltage divider. The voltage at FB is compared with the internal 1.245 V reference by the internal transconductance error amplifier to create an error voltage at COMP. The current of the switch is internally measured and added to the stabilizing ramp. The resulting sum is compared with the error voltage at COMP to control the PWM modulator. This current-mode regulation system allows fast transient response while maintaining a stable output voltage. By selecting the proper resistor-capacitor network from COMP to GND, the regulator response is optimized for a wide range of input voltages, output voltages, and load conditions.

ADJUSTABLE CURRENT LIMIT

A key feature of the ADP1614ACPZ-650-R7 and ADP1614ACPZ-1.3-R7 is a pin-adjustable peak current limit of up to 4 A (see Figure 10 to Figure 13 and Figure 33). This adjustable current limit allows the other external components to be selected specifically for the application. The current limit is set via an external resistor connected from Pin 9 (CLRES) to ground. For the ADP1614ACPZ-R7, the current limit is fixed at 3 A.

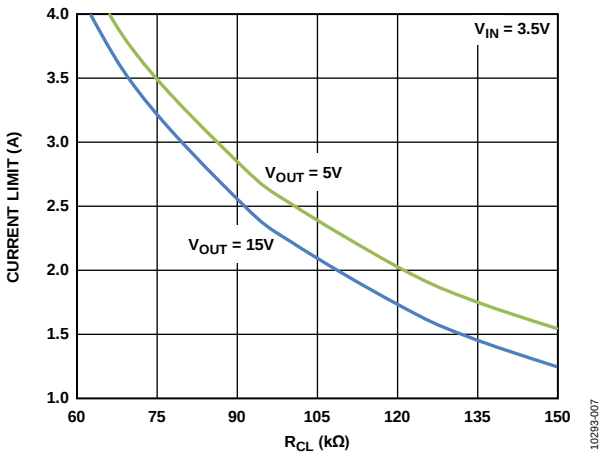


Figure 33. Peak Current Limit of Switch vs. R_{CL}

FREQUENCY SELECTION

The adjustable current-limit versions of the ADP1614 are internally programmed to operate at either 650 kHz or 1.3 MHz. Operation of the ADP1614 at 650 kHz (ADP1614ACPZ-650-R7) optimizes the efficiency of the device, whereas operation of the ADP1614 at 1.3 MHz (ADP1614ACPZ-1.3-R7) enables the device to be used with smaller external components. For the fixed current-limit version (ADP1614ACP-R7), the frequency is pin selectable via the FREQ Pin (Pin 9). Connect FREQ to GND for 650 kHz operation or connect FREQ to VIN for 1.3 MHz operation. Do not leave the FREQ pin floating.

SOFT START

To prevent input inrush current to the converter when the part is enabled, connect a capacitor from SS to GND to set the soft start period. After the ADP1614 is turned on, SS sources 5 µA (typical) to the soft start capacitor (C_{SS}) until it reaches 1.23 V at startup. As the soft start capacitor charges, it limits the peak current allowed by the part. By slowly charging the soft start capacitor, the input current ramps slowly to prevent it from overshooting excessively at startup. When the ADP1614 is disabled, the SS pin is internally shorted to GND to discharge the soft start capacitor.

THERMAL SHUTDOWN (TSD)

The ADP1614 includes TSD protection. If the die temperature exceeds 150°C (typical), TSD turns off the NMOS power device, significantly reducing power dissipation in the device and preventing output voltage regulation. The NMOS power device remains off until the die temperature is reduced to 130°C (typical). The soft start capacitor is discharged during TSD to ensure low output voltage overshoot and inrush currents when regulation resumes.

UNDERVOLTAGE LOCKOUT (UVLO)

If the input voltage is below the UVLO threshold, the ADP1614 automatically turns off the power switch and places the part into a low power consumption mode. This prevents potentially erratic operation at low input voltages and prevents the power device from turning on when the control circuitry cannot operate it. The UVLO levels have ~100 mV of hysteresis to ensure glitch-free startup.

SHUTDOWN MODE

The EN pin turns the ADP1614 regulator on or off. Drive EN low to shut down the regulator and reduce the input current to 0.25 µA (typical). Drive EN high to turn on the regulator.

When the converter is in shutdown mode (EN ≤ 0.3 V), there is a dc path from the input to the output through the inductor and output rectifier. This causes the output voltage to remain slightly below the input voltage by the forward voltage of the rectifier, preventing the output voltage from dropping to ground when the regulator is shut down.

Regardless of the state of the EN pin, when a voltage is applied to the VIN pin, a large current spike occurs due to the nonisolated path through the inductor and diode between V_{IN} and V_{OUT}. The high current is a result of the output capacitor charging. The peak value is dependent on the inductor, output capacitor, and any load active on the output of the regulator.

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADP1614 is supported by the ADIsimPower™ design toolset. ADIsimPower is a collection of tools that produce complete power designs that are optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and to calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and the external components. For more information about the ADIsimPower design tools, visit www.analog.com/ADIsimPower. The toolset is available from this website, and users can request an unpopulated board.

SETTING THE OUTPUT VOLTAGE

The ADP1614 features an adjustable output voltage range of V_{IN} to 20 V. The output voltage is set by the resistor voltage divider, R1 and R2 (see Figure 32), from the output voltage (V_{OUT}) to the 1.245 V feedback input at FB. Use the following equation to determine the output voltage:

$$V_{OUT} = 1.245 \times (1 + R1/R2) \quad (1)$$

Choose R1 based on the following equation:

$$R1 = R2 \times \left(\frac{V_{OUT} - 1.245}{1.245} \right) \quad (2)$$

INDUCTOR SELECTION

The inductor is an essential part of the step-up switching converter. It stores energy during the on time of the power switch and transfers that energy to the output through the output rectifier during the off time. To balance the trade-offs between small inductor current ripple and efficiency, inductance values in the range of 4.7 µH to 22 µH are recommended. In general, lower inductance values have higher saturation current and lower series resistance for a given physical size. However, lower inductance values result in higher peak current, which can lead to reduced efficiency and greater input and/or output ripple and noise. A peak-to-peak inductor ripple current close to 30% of the maximum dc input current typically yields an optimal compromise.

For determining the inductor ripple current in continuous operation, the input (V_{IN}) and output (V_{OUT}) voltages determine the switch duty cycle (D) as follows:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (3)$$

The duty cycle and switching frequency (f_{SW}) can be used to determine the on time:

$$t_{ON} = \frac{D}{f_{SW}} \quad (4)$$

The inductor ripple current (ΔI_L) in steady state is calculated by

$$\Delta I_L = \frac{V_{IN} \times t_{ON}}{L} \quad (5)$$

Solve for the inductance value (L) as follows:

$$L = \frac{V_{IN} \times t_{ON}}{\Delta I_L} \quad (6)$$

Ensure that the peak inductor current (the maximum input current plus half the inductor ripple current) is below the rated saturation current of the inductor. Likewise, make sure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

For continuous current-mode (CCM) duty cycles greater than 50% that occur with input voltages less than one-half the output voltage, slope compensation is required to maintain stability of the current-mode regulator. For stable current-mode operation, ensure that the selected inductance is equal to or greater than the minimum calculated inductance, L_{MIN}, for the application parameters in the following equation:

$$L > L_{MIN} = \frac{(V_{OUT} - 2 \times V_{IN})}{8 \times f_{SW}} \quad (7)$$

Inductors smaller than the 4.7 µH to 22 µH recommended range can be used as long as Equation 7 is satisfied for the given application. For input/output combinations that approach the 90% maximum duty cycle, doubling the inductor is recommended to ensure stable operation. Table 5 suggests a series of inductors for use with the ADP1614.

Table 5. Suggested Inductors

Manufacturer	Part Series
Coilcraft	XAL40xx, XAL50xx, XAL6060, DO3316P
TOKO Inc.	FDV06xx, DG6045C, FDSD0630, DEM8045C, FDVE1040
Würth Elektronik	WE-HCI, WE-TPC, WE-PD, WE-PD2, WE -PDF
Vishay Dale	IHLP-2020, IHLP-2525, IHLP-3232, IHLP-4040
TDK Components	SPM6530, VLP8040, VLF10040, VLF10045
Taiyo Yuden	NRS8030, NRS8040

CHOOSING THE INPUT AND OUTPUT CAPACITORS

The ADP1614 requires input and output bypass capacitors to supply transient currents while maintaining constant input and output voltages. Use low equivalent series resistance (ESR) capacitors of 10 µF or greater to prevent noise at the ADP1614 input. Place the capacitor between VIN and GND, as close as possible to the ADP1614. Ceramic capacitors are preferable because of their low ESR characteristics. Alternatively, use a high value, medium ESR capacitor in parallel with a 0.1 µF low ESR capacitor, placed as close as possible to the ADP1614.

The output capacitor maintains the output voltage and supplies current to the load while the ADP1614 switch is on. The value and characteristics of the output capacitor greatly affect the output voltage ripple and stability of the regulator. A low ESR ceramic dielectric capacitor is preferable. The output voltage ripple (ΔV_{OUT}) is calculated as follows:

$$\Delta V_{OUT} = \frac{Q_C}{C_{OUT}} = \frac{I_{OUT} \times t_{ON}}{C_{OUT}} \quad (8)$$

where:
Q_C is the charge removed from the capacitor.
C_{OUT} is the output capacitance.
I_{OUT} is the output load current.
t_{ON} is the on time of the switch.

The on time of the switch is determined as follows:

$$t_{ON} = \frac{D}{f_{SW}} \quad (9)$$

The input (V_{IN}) and output (V_{OUT}) voltages determine the switch duty cycle (D) as follows:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (10)$$

Choose the output capacitor based on the following equation:

$$C_{OUT} \geq \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times \Delta V_{OUT}} \quad (11)$$

Multilayer ceramic capacitors are recommended for this application.

DIODE SELECTION

The output rectifier conducts the inductor current to the output capacitor and load while the switch is off. For high efficiency, minimize the forward voltage drop of the diode. For this reason, using Schottky rectifiers is recommended. However, for high voltage, high temperature applications, where the Schottky rectifier reverse leakage current becomes significant and can degrade efficiency, use an ultrafast junction diode.

Many diode manufacturers derate the current capability of the diode as a function of the duty cycle. Verify that the output diode is rated to handle the average output load current with the minimum duty cycle. The minimum duty cycle in CCM of the ADP1614 is

$$D_{MIN} = \frac{V_{OUT} - V_{IN(MAX)}}{V_{OUT}} \quad (12)$$

where $V_{IN(MAX)}$ is the maximum input voltage.

The following are suggested Schottky diode manufacturers:

- ON Semiconductor
- Diodes, Inc.
- Toshiba
- ROHM Semiconductor

LOOP COMPENSATION

The ADP1614 uses external components to compensate the regulator loop, allowing optimization of the loop dynamics for a given application.

The step-up converter produces an undesirable right-half plane zero in the regulation feedback loop. This requires compensating the regulator such that the crossover frequency occurs well below the frequency of the right-half plane zero. The right-half plane zero is determined by the following equation:

$$F_Z(RHP) = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{R_{LOAD}}{2\pi \times L} \quad (13)$$

where:
$F_Z(RHP)$ is the right-half plane zero.
R_{LOAD} is the equivalent load resistance or the output voltage divided by the load current.

To stabilize the regulator, ensure that the regulator crossover frequency is less than or equal to one-fifth of the right-half plane zero.

The regulator loop gain is

$$A_{VL} = \frac{V_{FB}}{V_{OUT}} \times \frac{V_{IN}}{V_{OUT}} \times G_{MEA} \times \left|R_{OUT} \| Z_{COMP}\right| \times G_{CS} \times \left|Z_{OUT}\right| \quad (14)$$

where:
A_{VL} is the loop gain.
V_{FB} is the feedback regulation voltage, 1.245 V.
V_{OUT} is the regulated output voltage.
V_{IN} is the input voltage.
G_{MEA} is the error amplifier transconductance gain.
R_{OUT} = 67 MΩ.
Z_{COMP} is the impedance of the series RC network from COMP to GND.
G_{CS} is the current sense transconductance gain (the inductor current divided by the voltage at COMP), which is internally set by the ADP1614.
Z_{OUT} is the impedance of the load in parallel with the output capacitor.

To determine the crossover frequency, it is important to note that at the crossover frequency the compensation impedance (Z_{COMP}) is dominated by a resistor, and the output impedance (Z_{OUT}) is dominated by the impedance of an output capacitor. Therefore, when solving for the crossover frequency, the equation (by definition of the crossover frequency) is simplified to

$$\left|A_{VL}\right| = \frac{V_{FB}}{V_{OUT}} \times \frac{V_{IN}}{V_{OUT}} \times G_{MEA} \times R_{COMP} \times G_{CS} \times \frac{1}{2\pi \times f_C \times C_{OUT}} = 1 \quad (15)$$

where:
R_{COMP} is the compensation resistor.
f_C is the crossover frequency.

Solve for R_{COMP} as follows:

$$R_{COMP} = \frac{2\pi \times f_C \times C_{OUT} \times (V_{OUT})^2}{V_{FB} \times V_{IN} \times G_{MEA} \times G_{CS}} \quad (16)$$

where:
V_{FB} = 1.245 V.
G_{MEA} = 150 µA/V.
G_{CS} = 7 A/V.

Therefore,

$$R_{COMP} = \frac{4806 \times f_C \times C_{OUT} \times (V_{OUT})^2}{V_{IN}} \quad (17)$$

After the compensation resistor is known, set the zero formed by the compensation capacitor and resistor to one-fourth of the crossover frequency, or

$$C_{COMP} = \frac{2}{\pi \times f_C \times R_{COMP}} \quad (18)$$

where C_{COMP} is the compensation capacitor.

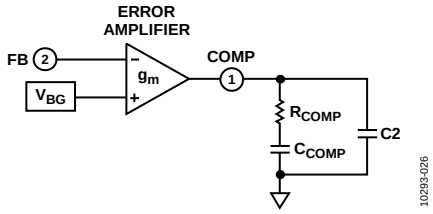


Figure 34. Compensation Components

Capacitor C2 is chosen to cancel the zero introduced by the ESR of the output capacitor.

Solve for C2 as follows:

$$C2 = \frac{ESR \times C_{OUT}}{R_{COMP}} \quad (19)$$

If a low ESR, ceramic output capacitor is used for C_{OUT}, C2 is optional. For optimal transient performance, R_{COMP} and C_{COMP} might need to be adjusted by observing the load transient response of the ADP1614. For most applications, the compensation resistor should be within the range of 1 kΩ to 100 kΩ, and the compensation capacitor should be within the range of 100 pF to 10 nF.

SOFT START CAPACITOR

Upon startup (EN ≥ 1.6 V) or fault recovery, the voltage at SS ramps up slowly by charging the soft start capacitor (C_{SS}) with an internal 5.5 µA current source (I_{SS}). As the soft start capacitor charges, it limits the peak current allowed by the part to prevent excessive overshoot at startup. Use the following equation to determine the necessary value of the soft start capacitor (C_{SS}) for a specific overshoot and start-up time when the part is at the current limit with maximum load:

$$C_{SS} = I_{SS} \frac{\Delta t}{V_{SS}} \quad (20)$$

where:
I_{SS} = 5.5 µA (typical).
Δt is the start-up time at the current limit.
V_{SS} = 1.23 V (typical).

If the applied load does not place the part at the current limit, the value of C_{SS} can be reduced. A 68 nF soft start capacitor results in negligible input current overshoot at startup and, therefore, is suitable for most applications. If an unusually large output capacitor is used, a longer soft start period is required to prevent input inrush current.

However, if fast startup is required, the soft start capacitor can be reduced or removed, which allows the ADP1614 to start quickly but with greater peak switch current.

PCB LAYOUT GUIDELINES

For high efficiency, good regulation, and stability, a well designed PCB layout is required.

Use the following guidelines when designing PCBs (see Figure 32 for a block diagram and Figure 3 for a pin configuration).

- Keep the low ESR input capacitor (C_{IN}), which is labeled as C4 in Figure 35, close to VIN and GND. This minimizes noise injected into the part from board parasitic inductance.
- Keep the high current path from C_{IN} through the L1 inductor to SW and GND as short as possible.
- Keep the high current path from VIN through the inductor (L1), the rectifier (D1), and the output capacitor (C_{OUT}), which is labeled as C7 in Figure 35, as short as possible.
- Keep high current traces as short and as wide as possible.
- Place the feedback resistors as close to FB as possible to prevent noise pickup. Connect the ground of the feedback network directly to an AGND plane that makes a Kelvin connection to the GND pin.
- Place the compensation components as close as possible to COMP. Connect the ground of the compensation network directly to an AGND plane that makes a Kelvin connection to the GND pin.
- Connect the soft start capacitor (C_{SS}), which is labeled as C1 in Figure 35, as close as possible to the device. Connect the ground of the soft start capacitor to an AGND plane that makes a Kelvin connection to the GND pin.
- Connect the current-limit set resistor (R_{CL}), which is labeled as R4 in Figure 35, as close as possible to the device. Connect the ground of the CL resistor to an AGND plane that makes a Kelvin connection to the GND pin.
- The PCB must be properly designed to conduct the heat away from the package. This is achieved by adding thermal vias to the PCB, which provide a thermal path to the inner or bottom layers. Thermal vias should be placed on the PCB underneath the exposed pad of the LFCSP and in the GND plane around the ADP1614 package to improve thermal performance of the package.

Avoid routing high impedance traces from the compensation and feedback resistors near any node connected to SW or near the inductor to prevent radiated noise injection.

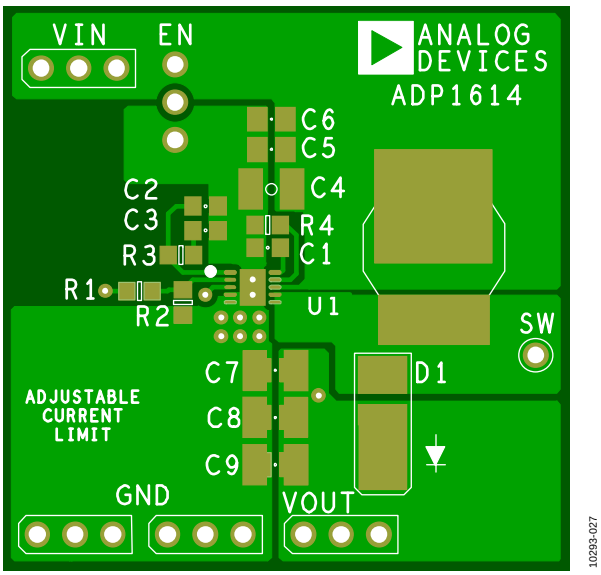


Figure 35. ADP1614 Recommended Top Layer Layout for the Adjustable Current-Limit Boost Application

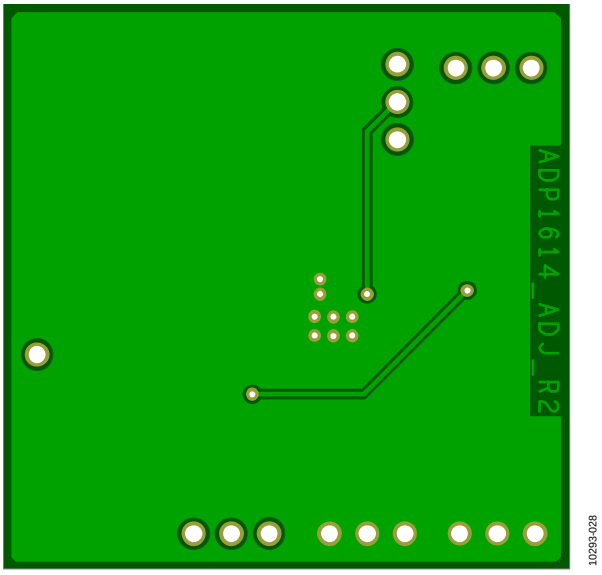


Figure 36. ADP1614 Recommended Bottom Layer Layout for the Adjustable Current-Limit Boost Application

OUTLINE DIMENSIONS

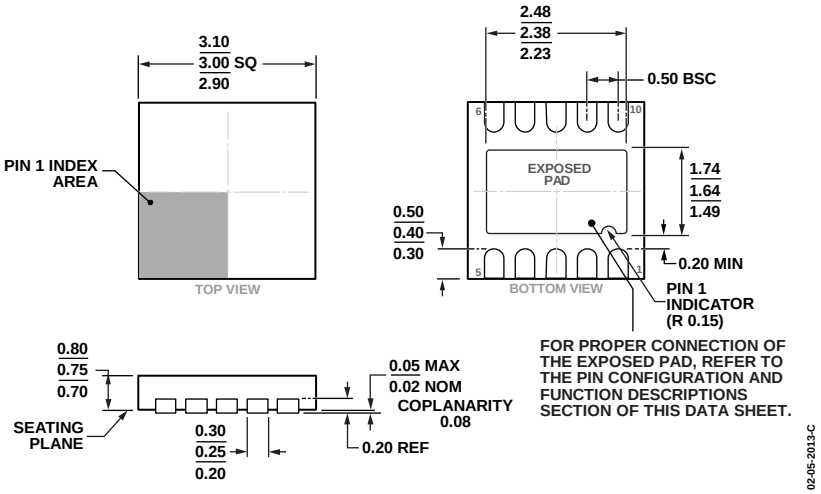


Figure 37. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Switching Frequency	Current Limit	Package Description	Package Option	Branding
ADP1614ACPZ-1.3-R7	−40°C to +125°C	1.3 MHz	Adjustable up to 4 A	10-Lead LFCSP_WD	CP-10-9	LM4
ADP1614ACPZ-650-R7	−40°C to +125°C	650 kHz	Adjustable up to 4 A	10-Lead LFCSP_WD	CP-10-9	LM5
ADP1614ACPZ-R7	−40°C to +125°C	Pin selectable	Fixed 3 A	10-Lead LFCSP_WD	CP-10-9	LNG
ADP1614-1.3-EVALZ		1.3 MHz	Adjustable up to 4 A	Evaluation Board, 15 V Output Voltage Configuration		
ADP1614-650-EVALZ		650 kHz	Adjustable up to 4 A	Evaluation Board, 5 V Output Voltage Configuration		

[1] Z = RoHS Compliant Part.

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