

# ADM3101E\* Product Page Quick Links

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## Documentation

### Data Sheet

- ADM3101E: 15 kV ESD Protected, 3.3 V Single-Channel RS-232 Line Driver/Receiver Data Sheet

## Software and Systems Requirements

- ADI RS-485/RS-422 Cross Reference Guide
- RS-232 Transceivers Cross Reference Guide

## Reference Materials

### Solutions Bulletins & Brochures

- RS-232 Transceivers Applications Bulletin (Summer 2008)

## Design Resources

- ADM3101E Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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## REVISION HISTORY

### 5/15—Rev. C to Rev. D

Change to $\theta_{JA}$ , Thermal Impedance (LFCSP) Parameter, Table 2 .....	4
Changes to Figure 2 and Table 3 .....	5
Changes to Ordering Guide .....	9
Updated Outline Dimensions .....	9

### 7/08—Rev. B to Rev. C

Changes to General Description Section .....	1
Reformatted Table 1 .....	4
Change to $T_{IN}$ Rating, Table 2 .....	4
Changes to Figure 2 .....	5
Moved High Baud Rate Section .....	8
Added Exposed Pad Notation to Outline Dimensions .....	9

### 12/07—Rev. A to Rev. B

Added 16-Lead QSOP Package (Universal) .....	1
Updated Outline Dimensions .....	10
Changes to Ordering Guide .....	10

### 10/07—Rev. 0 to Rev. A

Changes to Figure 1 .....	1
Changes to Table 1, RS-232 Receiver Section .....	3
Changes to Table 3 .....	5
Changes to Figure 11 .....	8

### 5/07—Revision 0: Initial Version

## SPECIFICATIONS

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $C1$  to  $C4 = 0.1 \mu\text{F}$ ,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC CHARACTERISTICS					
Operating Voltage Range	No load R <sub>L</sub> = 3 kΩ to GND	3.0	3.3	5.5	V
Power Supply Current, V <sub>CC</sub>			1.5	2.6	mA
			5	7	mA
LOGIC					
Input Logic Threshold Low, V <sub>INL</sub>	T <sub>IN</sub>			0.6	V
Input Logic Threshold High, V <sub>INH</sub>	T <sub>IN</sub>	1.4			V
Input Logic Threshold Low, V <sub>INL</sub>	T <sub>IN</sub> , V <sub>CC</sub> = 5.0 V ± 0.5 V			0.8	V
Input Logic Threshold High, V <sub>INH</sub>	T <sub>IN</sub> , V <sub>CC</sub> = 5.0 V ± 0.5 V	2.0			V
CMOS Output Voltage Low, V <sub>OL</sub>	I <sub>OUT</sub> = 1.6 mA			0.4	V
CMOS Output Voltage High, V <sub>OH</sub>	I <sub>OUT</sub> = −1 mA	V <sub>CC</sub> − 0.6			V
Logic Pull-Up Current	T <sub>IN</sub> = GND to V <sub>CC</sub>		5	12	μA
RS-232 RECEIVER					
EIA/TIA-232E Input Voltage Range <sup>1</sup>	V <sub>CC</sub> = 3.0 V to 5.5 V	−30		+30	V
EIA/TIA-232E Input Threshold Low		0.6	1.3		V
EIA/TIA-232E Input Threshold High			1.6	2.4	V
EIA/TIA-232E Input Hysteresis			0.4		V
EIA/TIA-232E Input Resistance		3	5	7	kΩ
TRANSMITTER					
Output Voltage Swing	V <sub>CC</sub> = 3.3 V to 5.5 V; transmitter output loaded with 3 kΩ to ground V <sub>CC</sub> = 3.0 V V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = ±2 V <sup>1</sup>	±5.0	±5.7		V
RS-232					
RS-562		±4.5			V
Transmitter Output Resistance		300			Ω
RS-232 Output Short-Circuit Current			±15		mA
TIMING CHARACTERISTICS					
Maximum Data Rate	V <sub>CC</sub> = 3.3 V, R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 50 pF to 1000 pF	460			kbps
Receiver Propagation Delay					
t <sub>PHL</sub>			0.4		μs
t <sub>PLH</sub>	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 1000 pF		0.4		μs
Transmitter Propagation Delay			600		ns
Transmitter Skew			80		ns
Receiver Skew			70		ns
Transition Region Slew Rate		+3 V to −3 V or −3 V to +3 V, V <sub>CC</sub> = +3.3 V, R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 1000 pF, T <sub>A</sub> = 25°C <sup>1</sup>	5.5	10	30
ESD PROTECTION					
RS-232 and CMOS I/O Pins	Human body model air discharge		±15		kV
	Human body model contact discharge		±8		kV

<sup>1</sup> Guaranteed by design.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Rating
$V_{CC}$	−0.3 V to +6 V
$V_+$	$(V_{CC} - 0.3 \text{ V})$ to +13 V
$V_-$	+0.3 V to −13 V
Input Voltages	
$T_{IN}$	−0.3 V to $(V_{CC} + 0.3 \text{ V})$
$R_{IN}$	±30 V
Output Voltages	
$T_{OUT}$	±15 V
$R_{OUT}$	−0.3 V to $(V_{CC} + 0.3 \text{ V})$
Short-Circuit Duration	
$T_{OUT}$	Continuous
Package Information	
$\theta_{JA}$ , Thermal Impedance (LFCSP)	80°C/W
$\theta_{JA}$ , Thermal Impedance (QSOP)	149.97°C/W
Operating Temperature Range	
Industrial (A Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature (Soldering, 10 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

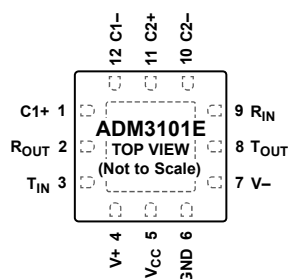
### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



## NOTES

1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO GND. THIS CONNECTION IS NOT REQUIRED TO MEET ELECTRICAL PERFORMANCE.

Figure 2. LFCSP Pin Configuration

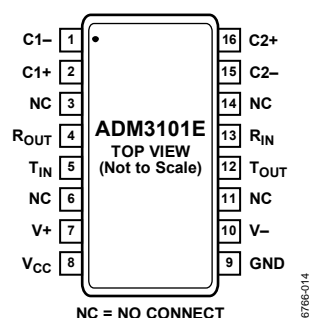


Figure 3. QSOP Pin Configuration

Table 3. Pin Function Descriptions

Pin No. <sup>1</sup>		Mnemonic	Description
LFCSP	QSOP		
1, 12	2, 1	C1+, C1-	Positive and Negative Connections for Charge Pump Capacitor. External Capacitor C1 is connected between these pins; a 0.1 $\mu$ F capacitor is recommended, but larger capacitors up to 10 $\mu$ F can be used.
2	4	R_OUT	Receiver Output. This pin outputs CMOS output logic levels.
3	5	T_IN	Transmitter (Driver) Input. This input accepts TTL/CMOS levels.
4	7	V+	Internally Generated Positive Supply (+6 V Nominal).
5	8	VCC	Power Supply Input, 3.0 V to 5.5 V.
6	9	GND	Ground. Must be connected to 0 V.
7	10	V-	Internally Generated Negative Supply (-6 V Nominal).
8	12	T_OUT	Transmitter (Driver) Output. This pin outputs RS-232 signal levels (typically $\pm 6$ V).
9	13	R_IN	Receiver Input. This input accepts RS-232 signal levels. An internal 5 k $\Omega$ pull-down resistor to GND is connected on the input.
10, 11	15, 16	C2-, C2+	Positive and Negative Connections for Charge Pump Capacitor. External Capacitor C2 is connected between these pins; a 0.1 $\mu$ F capacitor is recommended, but larger capacitors up to 10 $\mu$ F can be used.
N/A	3, 6, 11, 14	NC	No Connect. These pins should always remain unconnected.
EPAD	N/A	EPAD	Exposed Pad. The exposed pad must be connected to GND. This connection is not required to meet electrical performance.

<sup>1</sup> N/A means not applicable.

## TYPICAL PERFORMANCE CHARACTERISTICS

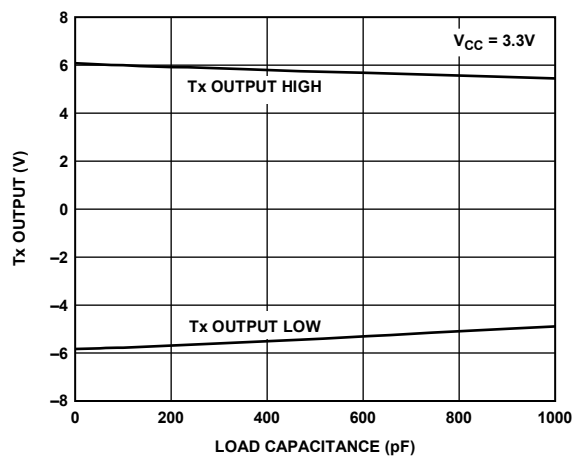


Figure 4. Transmitter Output Voltage High/Low vs. Load Capacitance @ 460 kbps

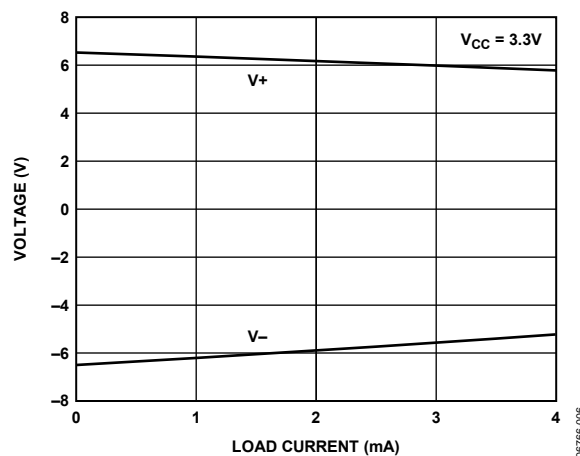


Figure 7. Charge Pump  $V+$ ,  $V-$  vs. Load Current

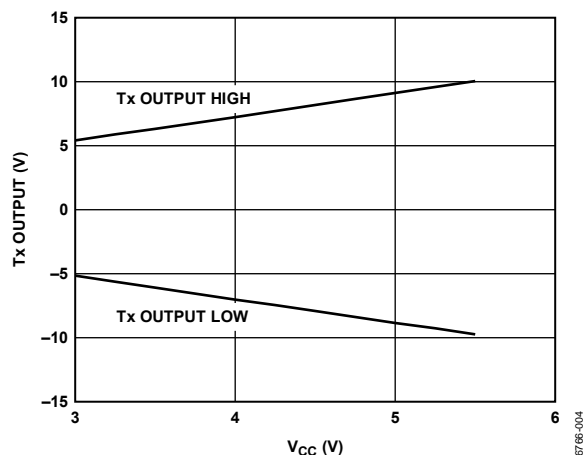


Figure 5. Transmitter Output Voltage High/Low vs.  $V_{CC}$ ,  $R_L = 3 k\Omega$

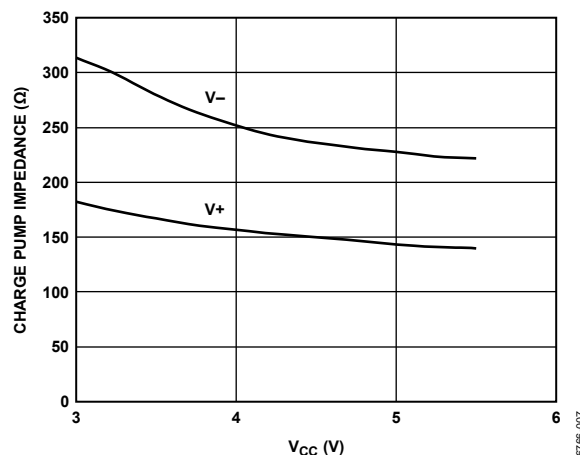


Figure 8. Charge Pump Impedance vs.  $V_{CC}$

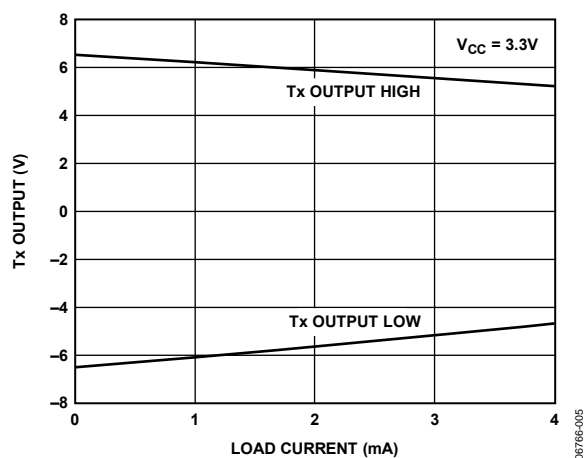


Figure 6. Transmitter Output Voltage High/Low vs. Load Current

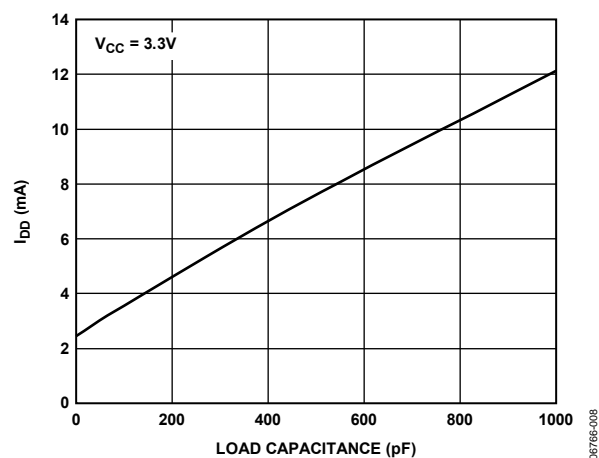


Figure 9. Power Supply Current vs. Load Capacitance

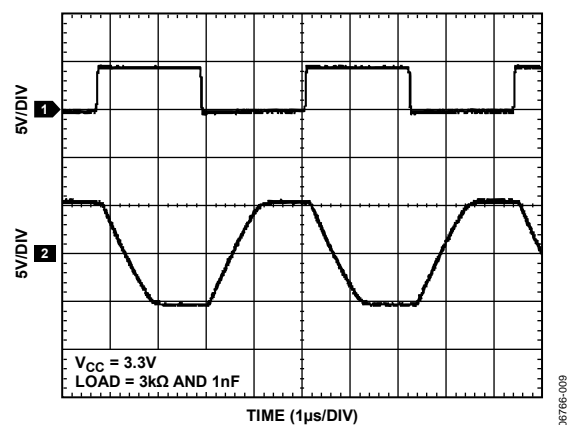
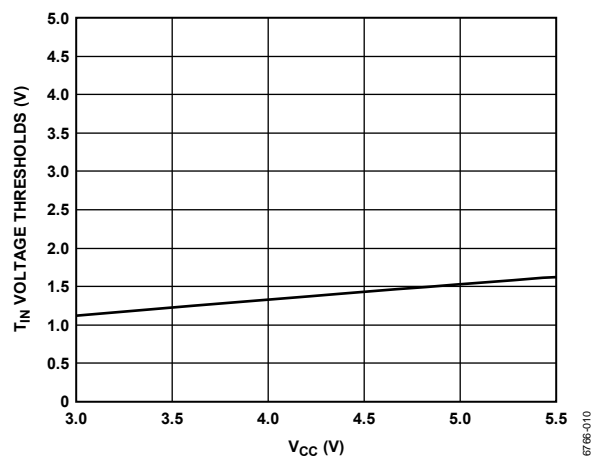


Figure 10. 460 kbps Data Transmission

Figure 11.  $T_{IN}$  Voltage Threshold vs.  $V_{CC}$

## THEORY OF OPERATION

The **ADM3101E** is a single-channel RS-232 line driver/receiver. Step-up voltage converters, coupled with level shifting transmitters and receivers, allow RS-232 levels to be developed while operating from a single 3.3 V supply.

CMOS technology is used to keep the power dissipation to an absolute minimum, allowing maximum battery life in portable applications.

## CIRCUIT DESCRIPTION

The internal circuitry consists of the following main sections:

- A charge pump voltage converter
- A 3.3 V logic to an EIA/TIA-232E transmitter
- An EIA/TIA-232E to a 3.3 V logic receiver

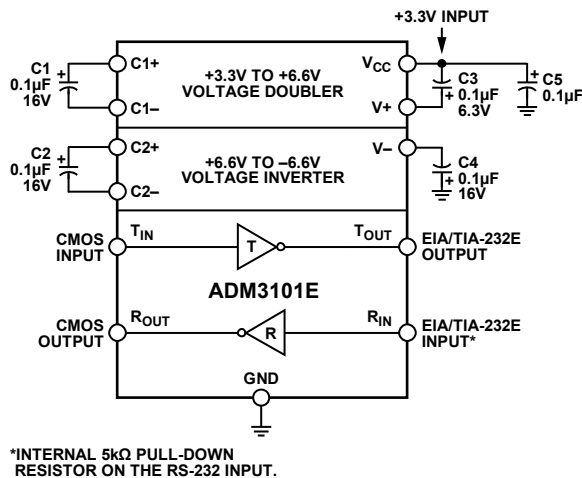


Figure 12. Typical Operating Circuit

### Charge Pump Voltage Converter

The charge pump voltage converter consists of a 200 kHz oscillator and a switching matrix. The converter generates a  $\pm 6.6$  V supply (when unloaded) from the 3.3 V input level. This is achieved in two stages by using a switched capacitor technique, as illustrated in Figure 13 and Figure 14. First, the 3.3 V input supply is doubled to +6.6 V by using C1 as the charge storage element. The +6.6 V level is then inverted to generate -6.6 V using C2 as the storage element. C3 is shown connected between V+ and V<sub>CC</sub> but is equally effective if connected between V+ and GND.

The C3 and C4 capacitors are used to reduce the output ripple. The values are not critical and can be increased, if desired. Larger capacitors (up to 10  $\mu$ F) can also be used in place of the C1, C2, C3, and C4 capacitors.

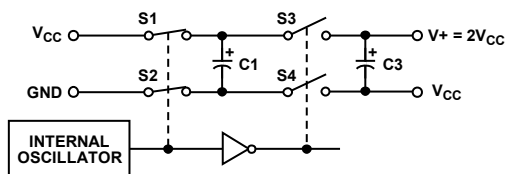


Figure 13. Charge Pump Voltage Doubler

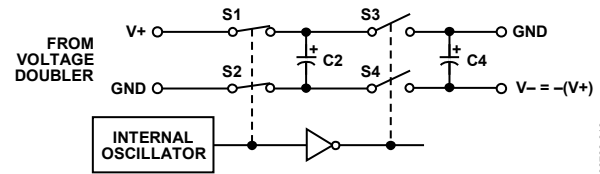


Figure 14. Charge Pump Voltage Inverter

### 3.3 V Logic to EIA/TIA-232E Transmitter

The transmitter driver converts the 3.3 V logic input levels into RS-232 output levels. When driving an RS-232 load with V<sub>CC</sub> = 3.3 V, the output voltage swing is typically  $\pm 6$  V. Internally, the T<sub>IN</sub> pin has a weak pull-up that allows it to be driven by an open-drain output, but the maximum operating data rate is reduced when the T<sub>IN</sub> pin is driven by an open-drain pin.

### EIA/TIA-232E to 3.3 V Logic Receiver

The receiver is an inverting level shifter that accepts the RS-232 input level and translates it into a 3.3 V logic output level. The input has an internal 5 k $\Omega$  pull-down resistor to ground and is protected against overvoltages of up to  $\pm 30$  V. An unconnected input is pulled to 0 V by the internal 5 k $\Omega$  pull-down resistor, which, therefore, results in a Logic 1 output level for an unconnected input or for an input connected to GND.

The receiver has a Schmitt trigger input with a hysteresis level of 0.4 V, which ensures error-free reception for both a noisy input and for an input with slow transition times.

### CMOS Input Voltage Thresholds

The CMOS input and output pins (T<sub>IN</sub> and R<sub>OUT</sub>) of the **ADM3101E** are designed to interface with 1.8 V logic thresholds when V<sub>CC</sub> = 3.3 V.

The CMOS input and output pins (T<sub>IN</sub> and R<sub>OUT</sub>) of the **ADM3101E** are also designed to interface with TTL/CMOS logic thresholds when V<sub>CC</sub> = 5 V.

### ESD Protection on RS-232 and CMOS I/O Pins

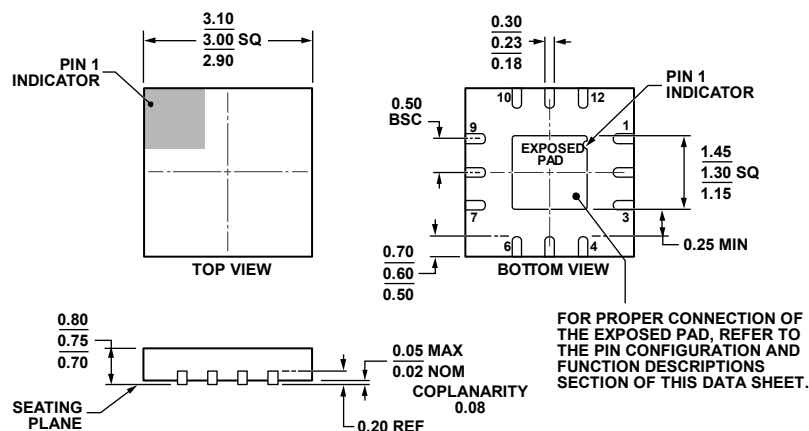
All RS-232 (T<sub>OUT</sub> and R<sub>IN</sub>) and CMOS (T<sub>IN</sub> and R<sub>OUT</sub>) inputs and outputs are protected against electrostatic discharges (up to  $\pm 15$  kV).

### HIGH BAUD RATE

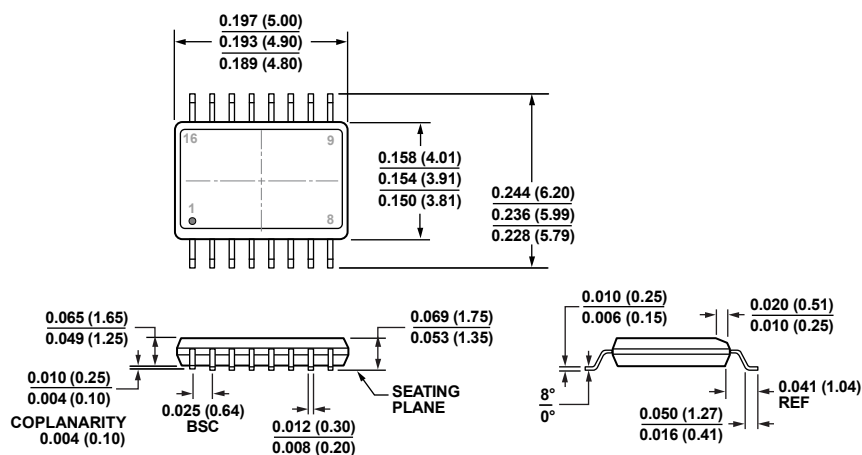
The **ADM3101E** features high slew rates, permitting data transmission at rates well in excess of the EIA/RS-232 specifications. The RS-232 voltage levels are maintained at data rates of up to 460 kbps, even under worst-case loading conditions, when T<sub>IN</sub> is driven by a push-pull output. The slew rate is internally controlled to less than 30 V/ $\mu$ s to minimize EMI interference.



## OUTLINE DIMENSIONS



111808-A



08-12-2014-A

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
ADM3101EACPZ-REEL	-40°C to +85°C	12-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-12-4	MA6
ADM3101EACPZ-250R7	-40°C to +85°C	12-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-12-4	MA6
ADM3101EARQZ	-40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16	
ADM3101EARQZ-REEL	-40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

## NOTES

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