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REVISION HISTORY

8/2016—Rev. A to Rev. B

Updated Format	Universal
Deleted ADM203	Universal
Changes to Typical Application Circuit Section Heading	1
Deleted ADM203 Functional Block Diagram Figure;	
Renumbered Sequentially	1
Changes to Features Section and General Description Section .	1
Deleted ADM203 Pin Configuration Figure and Figure 1	3
Changed T_{IN} to T_{xIN}	Throughout

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Changes to TTL/CMOS to RS-232 Transmitters (Drivers)	
Section and RS-232 to TLL/CMOS Receivers Section	8
Updated Outline Dimensions	9
Changes to Ordering Guide	10

1/2001—Rev. 0 to Rev. A

SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 10\%$, ($C1$ to $C4 = 0.1\text{ }\mu\text{F}$). All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE SWING	± 5	± 9		V	$V_{CC} = 5\text{ V} \pm 5\%$; $T1_{OUT}$ and $T2_{OUT}$ loaded with $3\text{ k}\Omega$ to GND
	± 5	± 9		V	$V_{CC} = 5\text{ V} \pm 10\%$; $T_A = 25^\circ\text{C}$; $T1_{OUT}$ and $T2_{OUT}$ loaded with $3\text{ k}\Omega$ to GND
V_{CC} POWER SUPPLY CURRENT (I_{CC})		2.5	6.0	mA	No load; $T1_{IN}$ and $T2_{IN} = V_{CC}$, or $T1_{IN}$ and $T2_{IN} = \text{GND}$
INPUT LOGIC THRESHOLD					
Low, V_{INL}			0.8	V	Tx_{IN}
High, V_{INH}	2.4			V	Tx_{IN}
LOGIC PULL-UP CURRENT		12	25	μA	$Tx_{IN} = 0\text{ V}$
RS-232 INPUT					
Voltage Range	-30		+30	V	
Threshold					
Low	0.8	1.2		V	
High		1.6	2.4	V	
Hysteresis	0.2	0.4	1.0	V	
Resistance	3	5	7	$\text{k}\Omega$	$T_A = 0^\circ\text{C}$ to 85°C
TTL/CMOS Output Voltage					
Low, V_{OL}			0.4	V	$I_{OUT} = 1.6\text{ mA}$
High, V_{OH}	3.5			V	$I_{OUT} = -1.0\text{ mA}$
PROPAGATION DELAY		0.3	5	μs	RS-232 to TTL
TRANSITION REGION SLEW RATE		8		V/ μs	$R_L = 3\text{ k}\Omega$, $C_L = 1000\text{ pF}$, measured from $+3\text{ V}$ to -3 V or -3 V to $+3\text{ V}$
BAUD RATE	120			kB	$R_L = 3\text{ k}\Omega$, $C_L = 1\text{ nF}$
OUTPUT					
Output Resistance	300			Ω	$V_{CC} = V+ = V- = 0\text{ V}$, $V_{OUT} = \pm 2\text{ V}$
RS-232 Output Short-Circuit Current		± 10	± 60	mA	

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	6 V
V_+	$(V_{CC} - 0.3 \text{ V})$ to $+14 \text{ V}$
V_-	$+0.3 \text{ V}$ to -14 V
Input Voltages	
$T1_{IN}, T2_{IN}$	-0.3 V to $(V_{CC} + 0.3 \text{ V})$
$R1_{IN}, R2_{IN}$	$\pm 30 \text{ V}$
Output Voltages	
$T1_{OUT}, T2_{OUT}$	$((V_+) + 0.3 \text{ V})$ to $((V_-) - 0.3 \text{ V})$
$R1_{OUT}, R2_{OUT}$	-0.3 V to $(V_{CC} + 0.3 \text{ V})$
Short-Circuit Duration	
$T1_{OUT}, T2_{OUT}$	Continuous
Power Dissipation	
16-Lead PDIP (N-16)	470 mW
16-Lead SOIC (R-16)	600 mW
16-Lead SOIC (RW-16)	500 mW
Thermal Impedance, θ_{JA}	
16-Lead PDIP (N-16)	135°C/W
16-Lead SOIC (R-16)	105°C/W
16-Lead SOIC (RW-16)	105°C/W
Operating Temperature Range	
Commercial (J Version)	0°C to 70°C
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Rating	$>2000 \text{ V}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

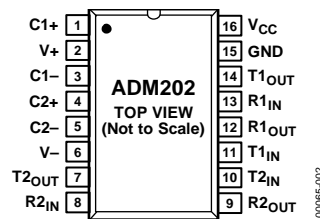


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	C1+	External Positive Capacitor 1 Connection. The positive terminal is connected to this pin.
2	V+	Internally Generated Positive Supply (+10 V nominal).
3	C1-	External Negative Capacitor 1 Connection. The negative terminal is connected to this pin.
4	C2+	External Positive Capacitor 2 Connection. The positive terminal is connected to this pin.
5	C2-	External Negative Capacitor 1 Connection. The negative terminal is connected to this pin.
6	V-	Internally Generated Negative Supply (-10 V Nominal).
7, 14	T2OUT, T1OUT	Transmitter (Driver) Outputs. These outputs are RS-232 levels (typically ± 10 V).
8, 13	R2IN, R1IN	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 k Ω pull-down resistor to GND is connected on each of these inputs.
9, 12	R2OUT, R1OUT	Receiver Outputs. These outputs are TTL/CMOS levels.
10, 11	T2IN, T1IN	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 k Ω pull-up resistor to V _{CC} is connected on each input.
15	GND	Ground. This pin must be connected to 0 V.
16	V _{CC}	Power Supply Input, 5 V \pm 10%.

TYPICAL PERFORMANCE CHARACTERISTICS

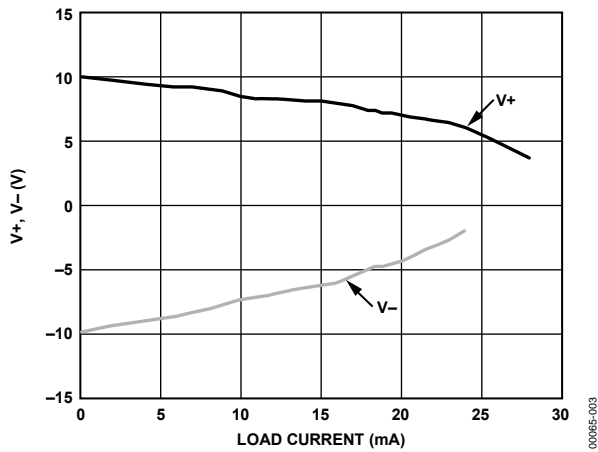
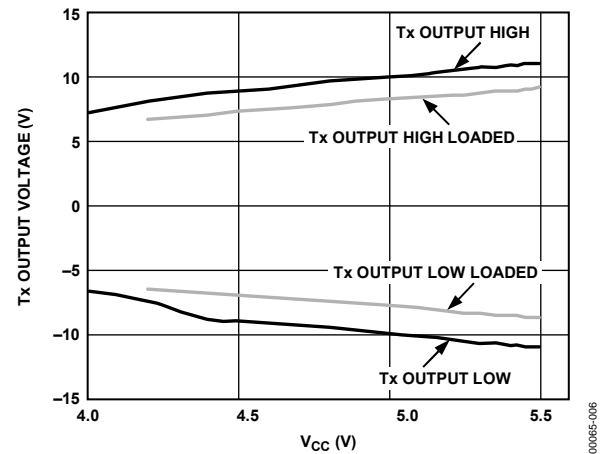
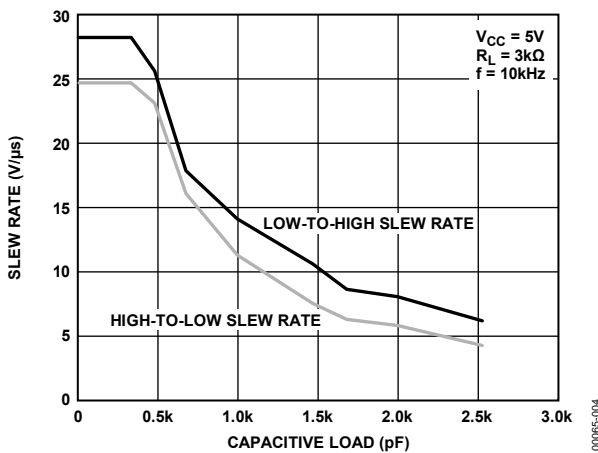
Figure 3. Charge Pump V_+ , V_- vs. Load CurrentFigure 6. Transmitter (Tx) Output Voltage vs. V_{CC} 

Figure 4. Transmitter Slew Rate vs. Capacitive Load

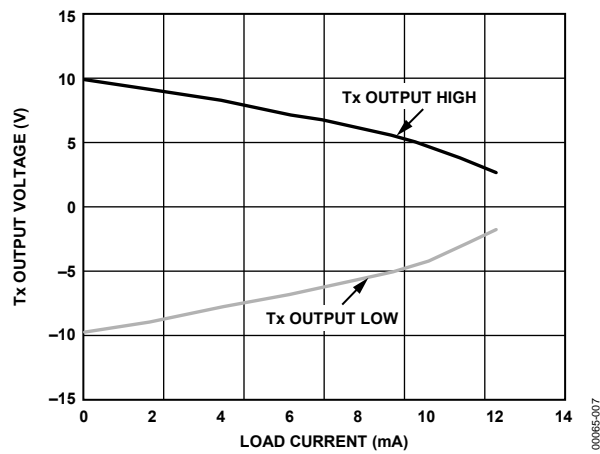


Figure 7. Transmitter (Tx) Output Voltage vs. Load Current

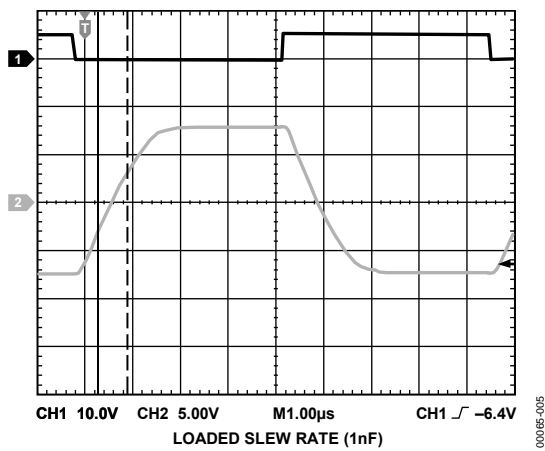


Figure 5. Transmitter Fully Loaded Slew Rate

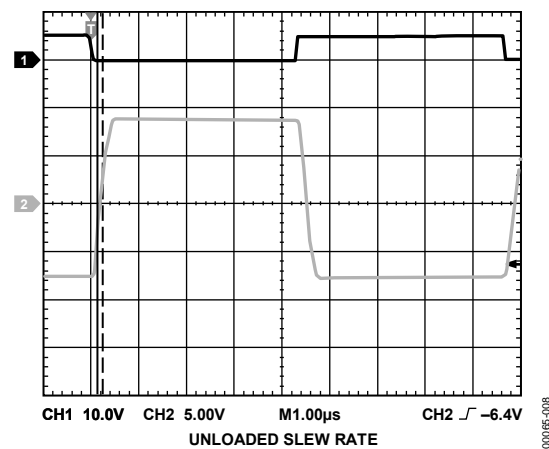


Figure 8. Transmitter Unloaded Slew Rate

THEORY OF OPERATION

The [ADM202](#) is an RS-232 driver/receiver designed to solve interface problems by meeting the TIA/EIA-232E specifications while using a single digital 5 V supply. The EIA standard requires that transmitters deliver ± 5 V minimum on the transmission channel and that receivers can accept signal levels down to ± 3 V. The device achieves this by integrating step-up voltage converters and level shifting transmitters and receivers

on the same chip. CMOS technology keeps the power dissipation to an absolute minimum.

The [ADM202](#) contains an internal voltage doubler and a voltage inverter that generates ± 10 V from the 5 V input. External 0.1 μ F capacitors are required for the internal voltage converter.

APPLICATIONS INFORMATION

The internal circuitry consists of three main sections, as follows:

- A charge pump dc-to-dc voltage converter
- TTL/CMOS to RS-232 transmitters
- RS-232 to TTL/CMOS receivers

CHARGE PUMP DC-TO-DC VOLTAGE CONVERTER

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ± 10 V supply from the input 5 V level in two stages, using a switched capacitor technique as illustrated in Figure 9 and Figure 10. First, the 5 V input supply is doubled to 10 V using Capacitor C1 as the charge storage element. The 10 V level is then inverted to generate -10 V using C2 as the storage element.

Capacitors C3 and C4 reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors, C1 and C2, can also be reduced at the expense of higher output impedance on the $V+$ and $V-$ supplies.

The $V+$ and $V-$ supplies can be used to power external circuitry if the current requirements are small.

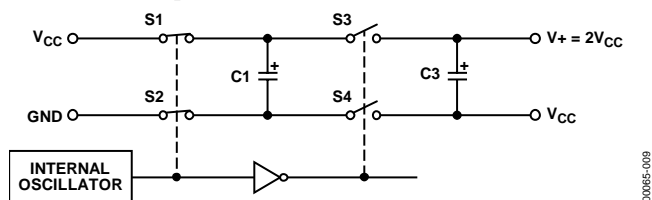


Figure 9. Charge Pump Voltage Doubler

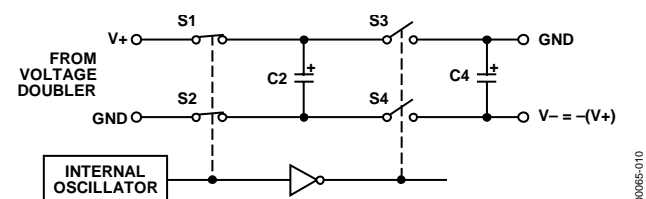


Figure 10. Charge Pump Voltage Inverter

TTL/CMOS TO RS-232 TRANSMITTERS (DRIVERS)

The drivers convert TTL/CMOS input levels into TIA/EIA-232-E output levels. With $V_{CC} = 5$ V and driving a typical TIA/EIA-232-E load, the output voltage swing is ± 9 V. Even under worst case conditions, the drivers are guaranteed to meet the ± 5 V TIA/EIA-232-E minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal $V_{CC} = 5$ V, the switching threshold is 1.25 V typical. Unused inputs can be left unconnected, as an internal 400 k Ω pull-up resistor pulls them high, forcing the outputs into a low state.

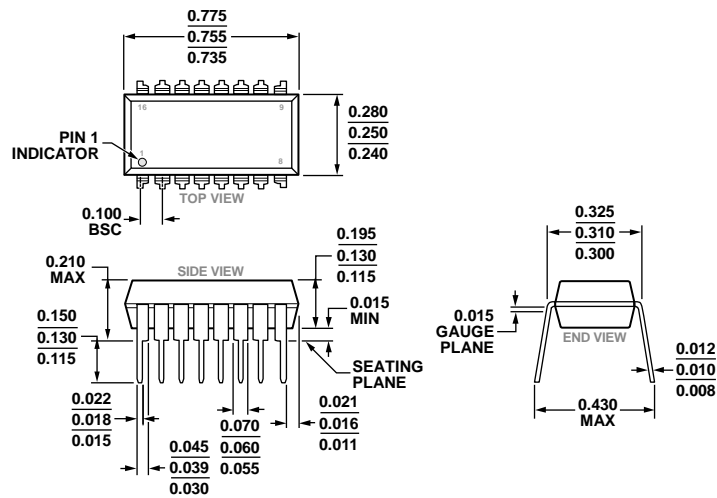
As required by the TIA/EIA-232-E standard, the slew rate is limited to less than 30 V/ μ s without the need for an external slew limiting capacitor, and the output impedance in the power-down state is greater than 300 Ω .

RS-232 TO TTL/CMOS RECEIVERS

The receivers are inverting level shifters that accept TIA/EIA-232-E input levels (± 5 V to ± 15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 k Ω pull-down resistors to ground and are protected against overvoltages of up to ± 30 V. The guaranteed switching thresholds are 0.8 V (V_{INH}) and 2.4 V (V_{INL}), which are well within the ± 3 V TIA/EIA-232-E requirement. The low level threshold is deliberately positive because it ensures that an unconnected input is interpreted as a low level.

The receivers have a Schmitt triggered input with a hysteresis level of 0.5 V. This hysteresis level ensures error free reception, both for noisy inputs and for inputs with slow transition times.

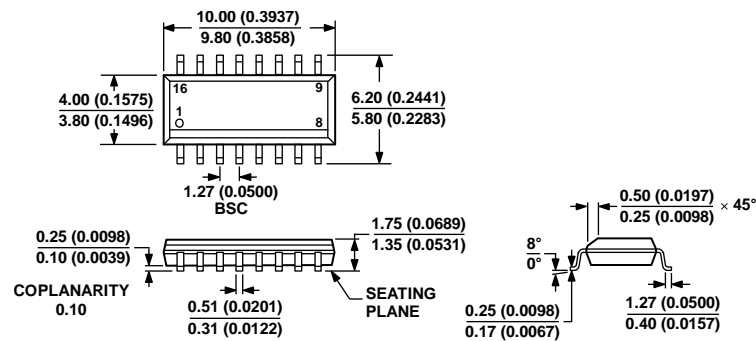
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BB

Figure 11. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)

Dimensions shown in inches

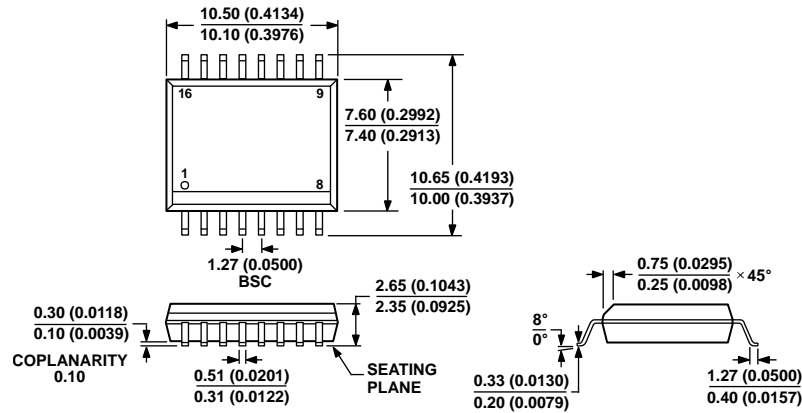


COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 12. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 13. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)

Dimensions shown in millimeters and (inches)

03-27-2007-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADM202JNZ	0°C to 70°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADM202JRN	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADM202JRN-REEL	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADM202JRN-REEL7	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADM202JRNZ	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADM202JRNZ-REEL	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADM202JRNZ-REEL7	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADM202JRWZ	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM202JRWZ-REEL	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16

¹ Z = RoHS Compliant Part.