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REVISION HISTORY

3/16—Rev. B to Rev. C

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Changes to Offset Voltage Parameter and Input Resistance Parameter, Table 3 ... 5
Changes to Table 5 ... 7
Updated Outline Dimensions ... 19
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1/10—Rev. A to Rev. B

Added ADA4051-1, 5-Lead SC-70 Package ... Universal
Added Figure 2; Renumbered Sequentially ... 1
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10/09—Rev. 0 to Rev. A

Added ADA4051-1, 5-Lead SOT-23 Package ... Universal
Added ADA4051-2, 8-Lead LFCSP Package ... Universal
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7/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

V_{SY} = 1.8 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, R_L = 100 kΩ to GND, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
ADA4051-2		0 V ≤ V_{CM} ≤ 1.8 V		2	15	µV
ADA4051-1		0 V ≤ V_{CM} ≤ 1.8 V		2	17	µV
		−40°C ≤ T_A ≤ +125°C			27	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.02	0.1	µV/°C
Input Bias Current	I_B			5	50	pA
		−40°C ≤ T_A ≤ +125°C			200	pA
Input Offset Current	I_{OS}			10	100	pA
		−40°C ≤ T_A ≤ +125°C			150	pA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	0		1.8	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.8 V	105	125		dB
		−40°C ≤ T_A ≤ +125°C	100			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ to V_{CM}, 0.1 V ≤ V_{OUT} ≤ V_{SY} − 0.1 V	106	130		dB
		−40°C ≤ T_A ≤ +125°C	100			dB
Input Resistance						
Differential Mode	R_{INDM}			8		MΩ
Common Mode	R_{INCM}			250		GΩ
Input Capacitance, Differential Mode	C_{INDM}			2		pF
Input Capacitance, Common Mode	C_{INCM}			5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}	1.796	1.799		V
		−40°C ≤ T_A ≤ +125°C	1.79			V
		R_L = 10 kΩ to V_{CM}	1.76	1.796		V
		−40°C ≤ T_A ≤ +125°C	1.7			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}		1	3	mV
		−40°C ≤ T_A ≤ +125°C			9	mV
		R_L = 10 kΩ to V_{CM}		3	20	mV
		−40°C ≤ T_A ≤ +125°C			40	mV
Short-Circuit Current	I_{SC}	V_{OUT} = V_{SY} or GND		13		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, G = 10		1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	1.8 V ≤ V_{SY} ≤ 5.5 V	110	135		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Supply Current per Amplifier	I_{SY}					
ADA4051-2		V_{OUT} = V_{SY}/2		13	17	µA
ADA4051-1		V_{OUT} = V_{SY}/2		15	18	µA
		−40°C ≤ T_A ≤ +125°C			20	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	R_L = 10 kΩ, C_L = 100 pF, G = 1		0.04		V/µs
	SR−	R_L = 10 kΩ, C_L = 100 pF, G = 1		0.03		V/µs
Settling Time	t_S	To 0.1%, V_{IN} = 1 V p-p, R_L = 10 kΩ, C_L = 100 pF		120		µs
Gain Bandwidth Product	GBP	C_L = 100 pF, G = 1		115		kHz
Phase Margin	Φ_M	C_L = 100 pF, G = 1		40		Degrees
Channel Separation	CS	V_{IN} = 1.7 V, f = 100 Hz		140		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		1.96		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		95		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		100		fA/√Hz

ELECTRICAL CHARACTERISTICS—5 V OPERATION

V_{SY} = 5.0 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, R_L = 100 kΩ to GND, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
ADA4051-2		0 V ≤ V_{CM} ≤ 5 V		2	15	µV
ADA4051-1		0 V ≤ V_{CM} ≤ 5 V		2	17	µV
		−40°C ≤ T_A ≤ +125°C			27	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.02	0.1	µV/°C
Input Bias Current	I_B			20	70	pA
		−40°C ≤ T_A ≤ +125°C			200	pA
Input Offset Current	I_{OS}			40	100	pA
		−40°C ≤ T_A ≤ +125°C			150	pA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	0		5	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 5 V	110	135		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ to V_{CM}, 0.1 V ≤ V_{OUT} ≤ V_{SY} − 0.1 V	115	135		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Input Resistance						
Differential Mode	R_{INDM}			8		MΩ
Common Mode	R_{INCM}			250		GΩ
Input Capacitance, Differential Mode	C_{INDM}			2		pF
Input Capacitance, Common Mode	C_{INCM}			5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}	4.996	4.998		V
		−40°C ≤ T_A ≤ +125°C	4.985			V
		R_L = 10 kΩ to V_{CM}	4.96	4.99		V
		−40°C ≤ T_A ≤ +125°C	4.9			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}		1	4	mV
		−40°C ≤ T_A ≤ +125°C			13	mV
		R_L = 10 kΩ to V_{CM}		9	30	mV
		−40°C ≤ T_A ≤ +125°C			90	mV
Short-Circuit Current	I_{SC}	V_{OUT} = V_{SY} or GND		15		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, G = 10		1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	1.8 V ≤ V_{SY} ≤ 5.5 V	110	135		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Supply Current per Amplifier	I_{SY}					
ADA4051-2		V_{OUT} = V_{SY}/2		13	17	µA
ADA4051-1		V_{OUT} = V_{SY}/2		15	18	µA
		−40°C ≤ T_A ≤ +125°C			20	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	R_L = 10 kΩ, C_L = 100 pF, G = 1		0.06		V/µs
	SR−	R_L = 10 kΩ, C_L = 100 pF, G = 1		0.04		V/µs
Settling Time	t_S	To 0.1%, V_{IN} = 1 V p-p, R_L = 10 kΩ, C_L = 100 pF		110		µs
Gain Bandwidth Product	GBP	C_L = 100 pF, G = 1		125		kHz
Phase Margin	Φ_M	C_L = 100 pF, G = 1		40		Degrees
Channel Separation	CS	V_{IN} = 4.99 V, f = 100 Hz		140		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		1.96		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		95		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		100		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$\pm V_{SY} \pm 0.3$ V
Input Current[1]	±10 mA
Differential Input Voltage[2]	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.
[2] Inputs are protected against high differential voltages by internal series 1.33 kΩ resistors and back-to-back diode-connected N-MOSFETs (with a typical V_T of 0.7 V for V_{CM} of 0 V).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered on a circuit board for surface-mount packages with its exposed paddle soldered to a pad, if applicable. Table 5 shows simulated thermal values for a 4-layer (2S2P) JEDEC standard thermal test board, unless otherwise specified.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
5-Lead SOT-23 (RJ-5)	190	°C/W
5-Lead SC-70 (KS-5)	534	°C/W
8-Lead MSOP (RM-8)	142	°C/W
8-Lead LFCSP (CP-8-13)		
1-Layer JEDEC Board	272	°C/W
2-Layer JEDEC Board	145	°C/W
2-Layer JEDEC Board with 2 × 2 Vias	55	°C/W

POWER SEQUENCING

The op amp supplies must be established simultaneously with or before any input signals are applied. If this is not possible, the input current must be limited to 10 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

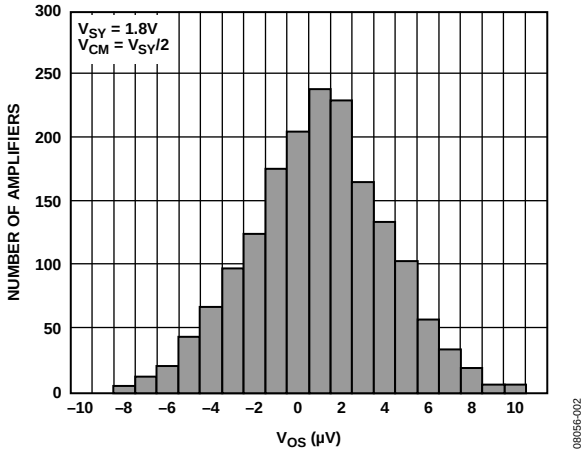


Figure 5. Input Offset Voltage Distribution

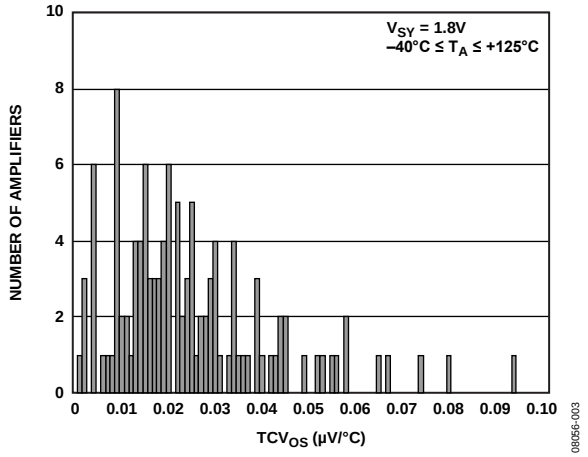


Figure 6. Input Offset Voltage Drift Distribution with Temperature

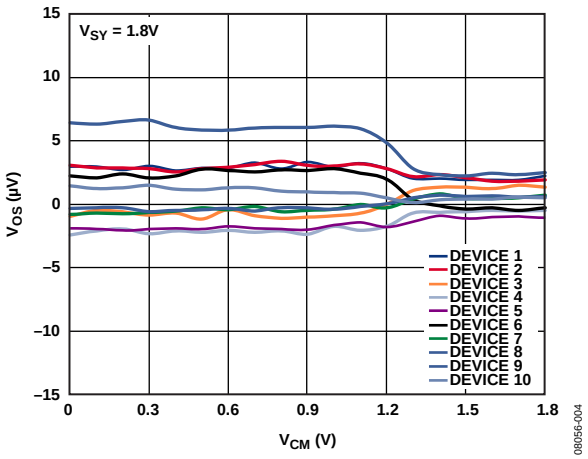


Figure 7. Input Offset Voltage vs. Input Common-Mode Voltage

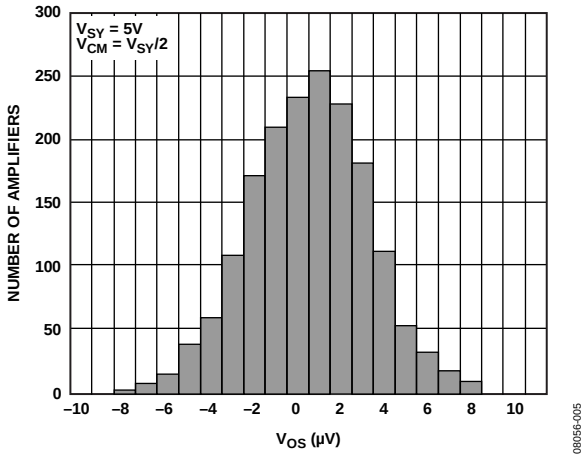


Figure 8. Input Offset Voltage Distribution

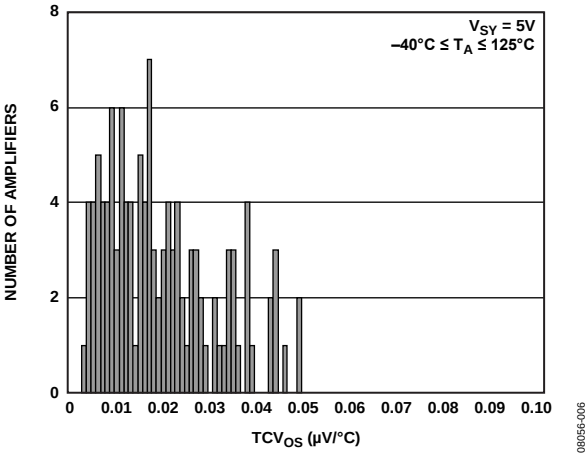


Figure 9. Input Offset Voltage Drift Distribution with Temperature

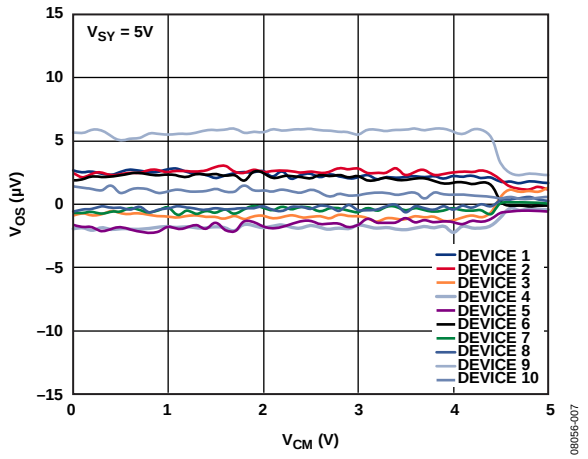


Figure 10. Input Offset Voltage vs. Input Common-Mode Voltage

T_A = 25°C, unless otherwise noted.

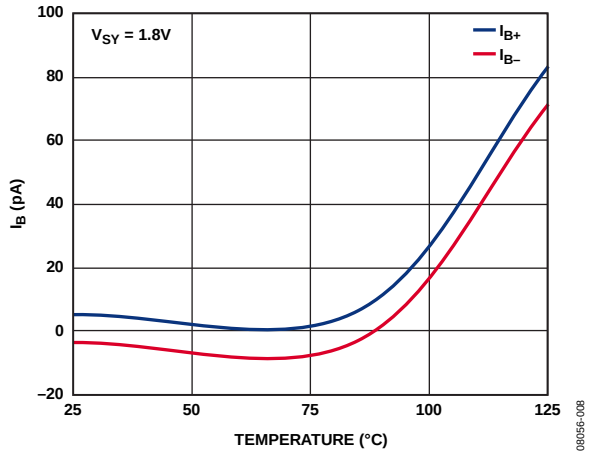


Figure 11. Input Bias Current vs. Temperature

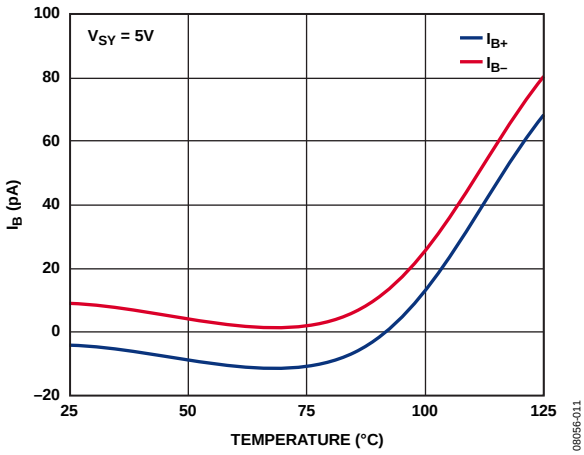


Figure 14. Input Bias Current vs. Temperature

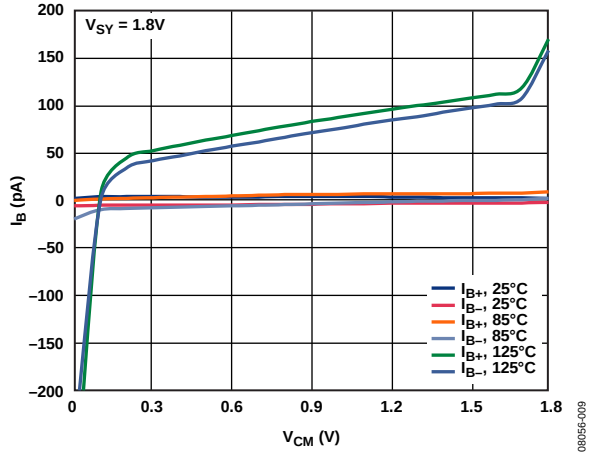


Figure 12. Input Bias Current vs. Common-Mode Voltage and Temperature

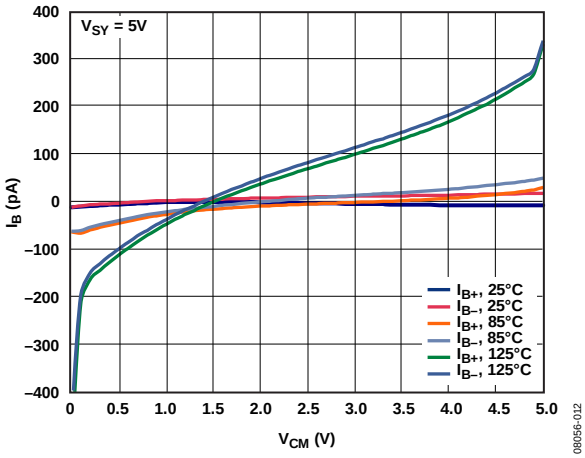


Figure 15. Input Bias Current vs. Common-Mode Voltage and Temperature

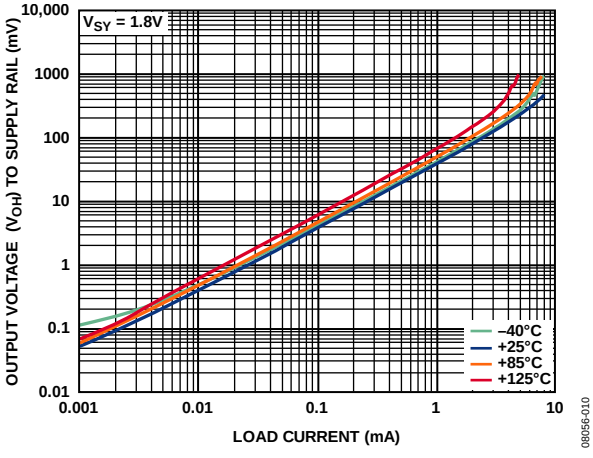


Figure 13. Output Voltage (V_{OH}) to Supply Rail vs. Load Current and Temperature

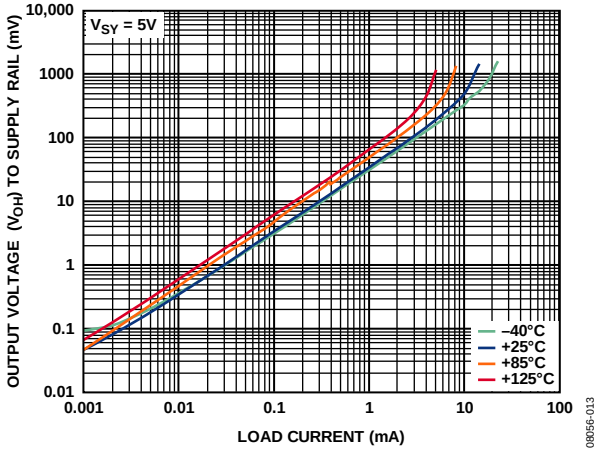


Figure 16. Output Voltage (V_{OH}) to Supply Rail vs. Load Current and Temperature

T_A = 25°C, unless otherwise noted.

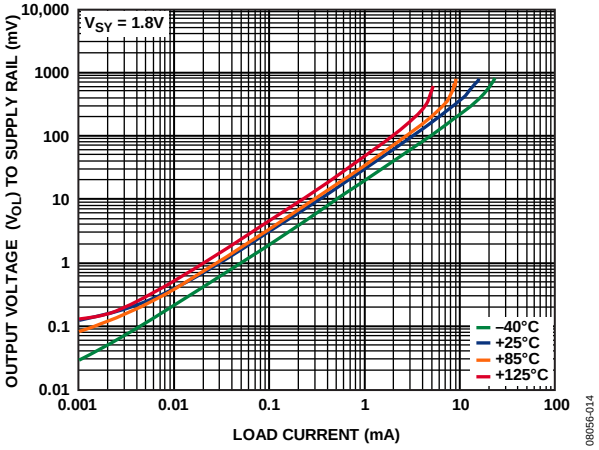


Figure 17. Output Voltage (V_{OL}) to Supply Rail vs. Load Current and Temperature

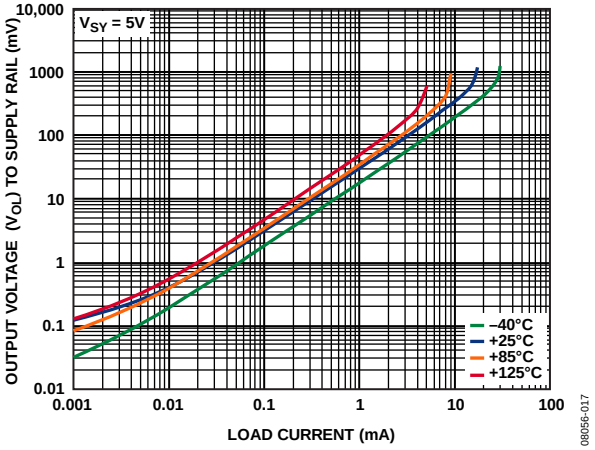


Figure 20. Output Voltage (V_{OL}) to Supply Rail vs. Load Current and Temperature

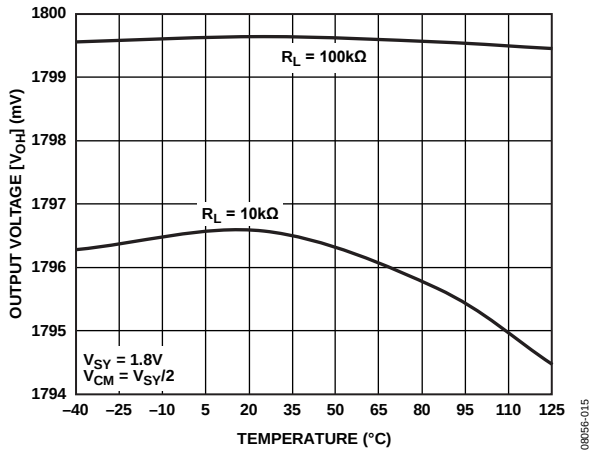


Figure 18. Output Voltage (V_{OH}) vs. Temperature

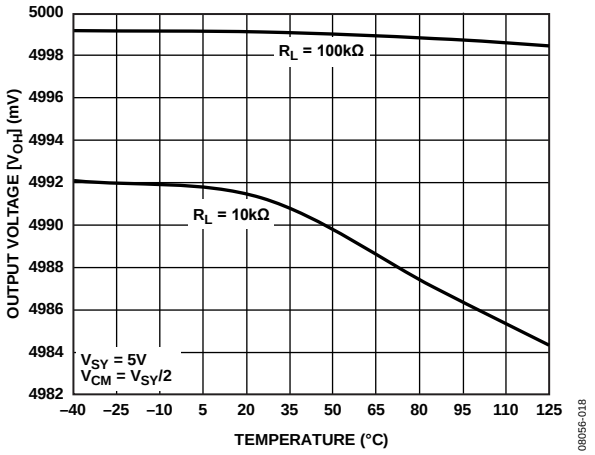


Figure 21. Output Voltage (V_{OH}) vs. Temperature

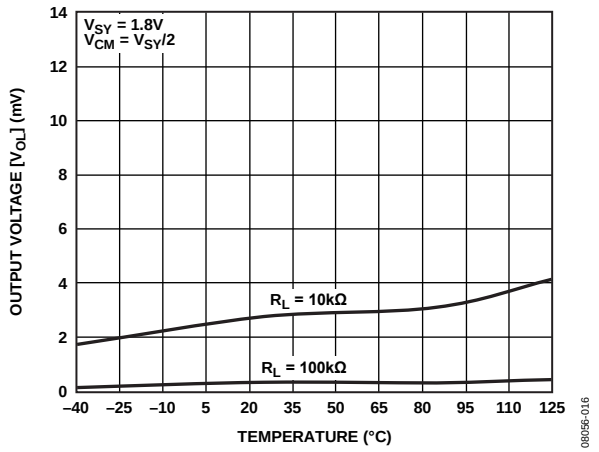


Figure 19. Output Voltage (V_{OL}) vs. Temperature

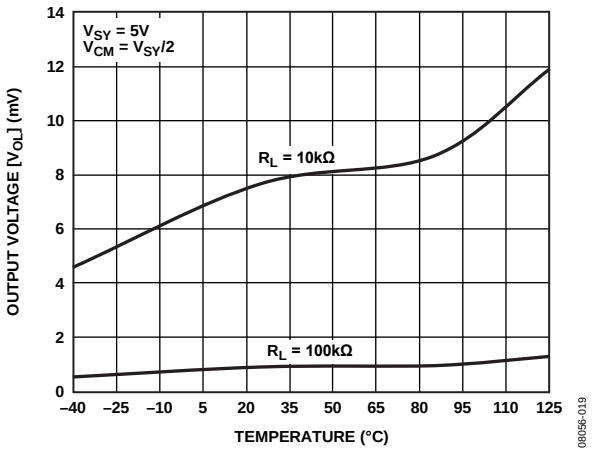


Figure 22. Output Voltage (V_{OL}) vs. Temperature

T_A = 25°C, unless otherwise noted.

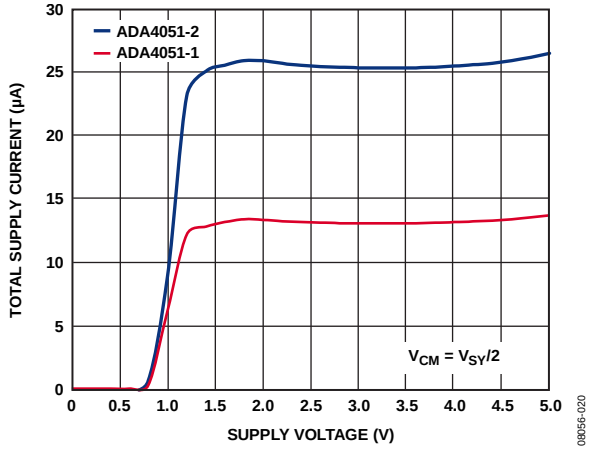


Figure 23. Total Supply Current vs. Supply Voltage

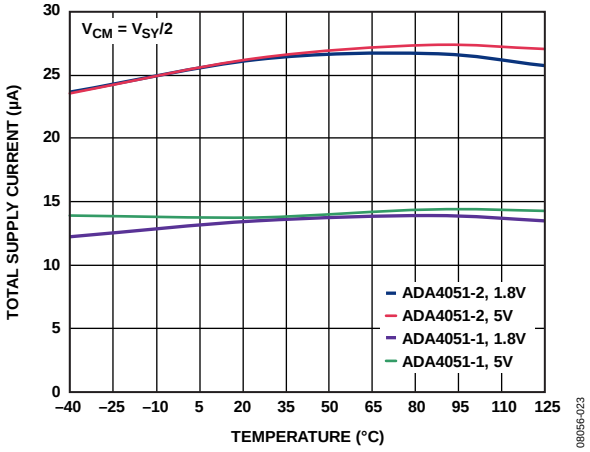


Figure 26. Total Supply Current vs. Temperature

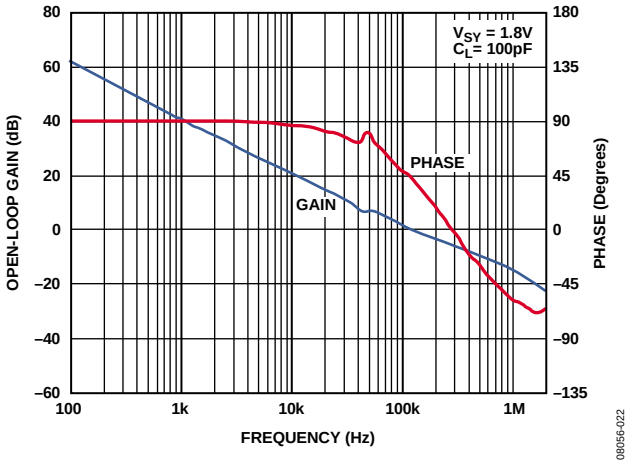


Figure 24. Open-Loop Gain and Phase vs. Frequency

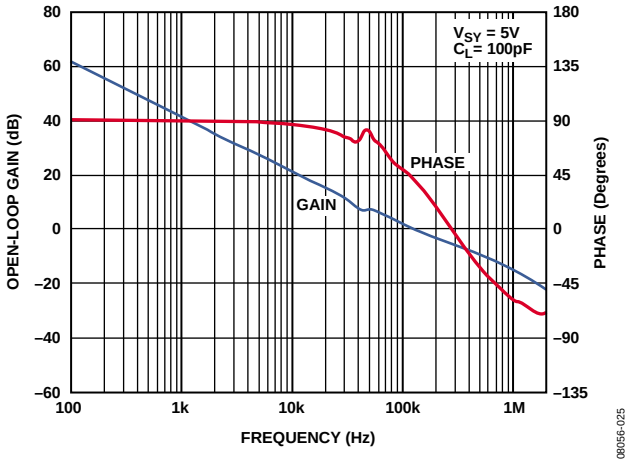


Figure 27. Open-Loop Gain and Phase vs. Frequency

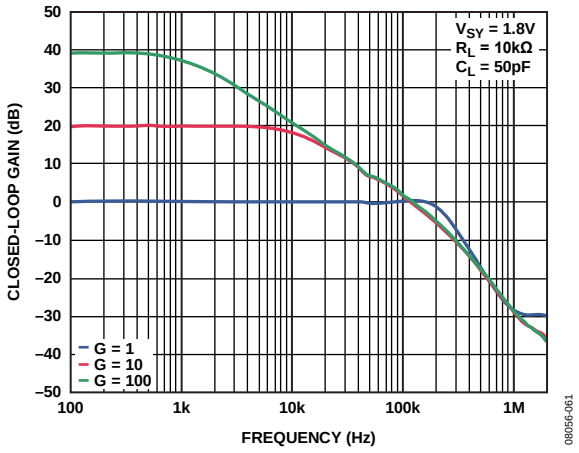


Figure 25. Closed-Loop Gain vs. Frequency

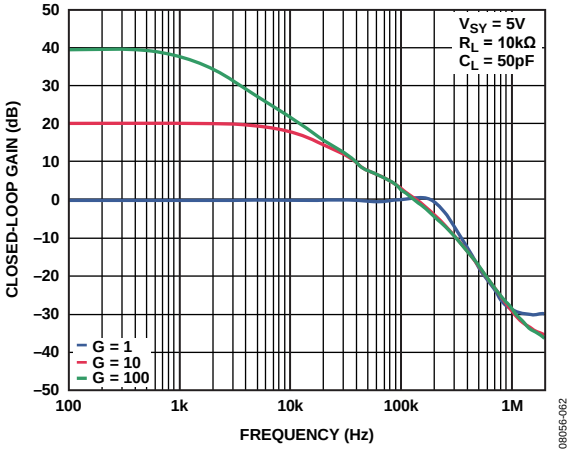


Figure 28. Closed-Loop Gain vs. Frequency

T_A = 25°C, unless otherwise noted.

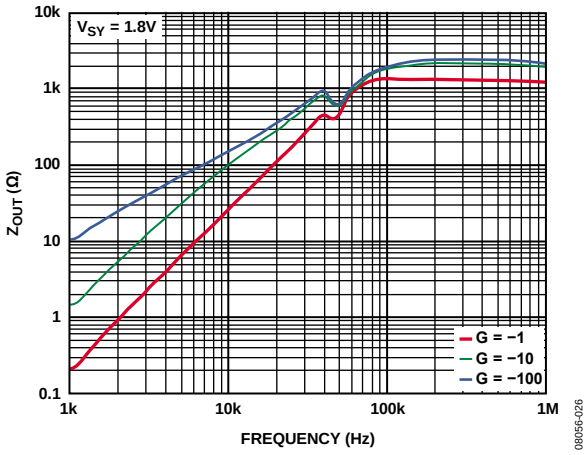


Figure 29. Output Impedance vs. Frequency

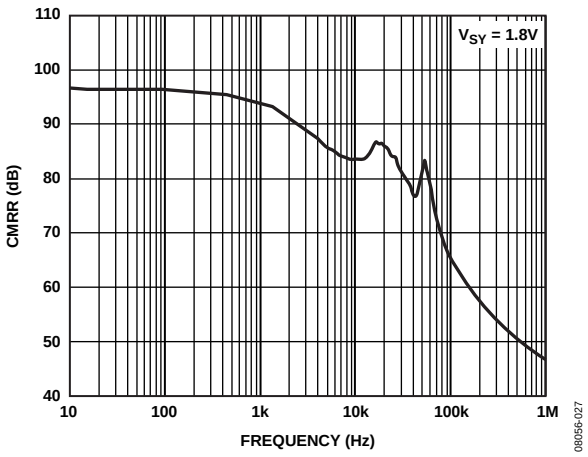


Figure 30. CMRR vs. Frequency

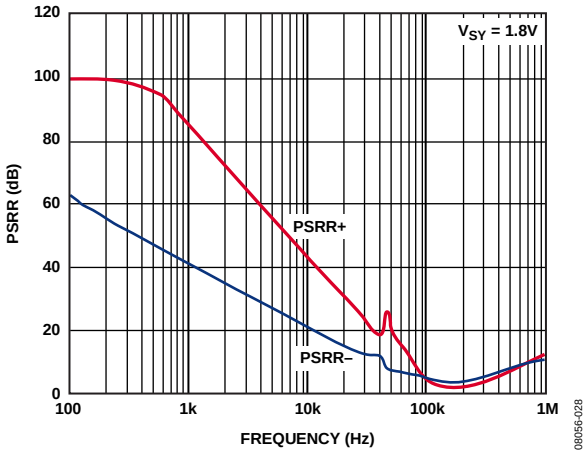


Figure 31. PSRR vs. Frequency

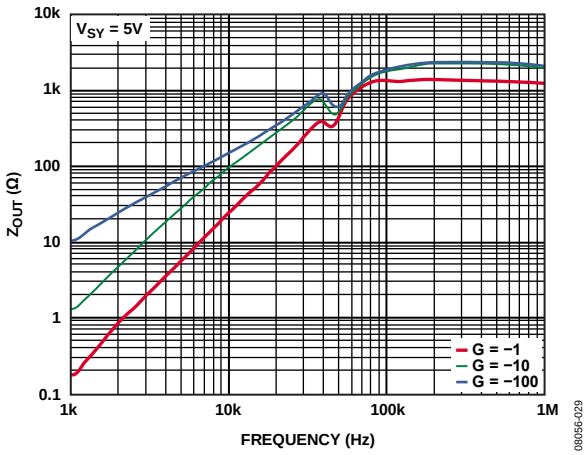


Figure 32. Output Impedance vs. Frequency

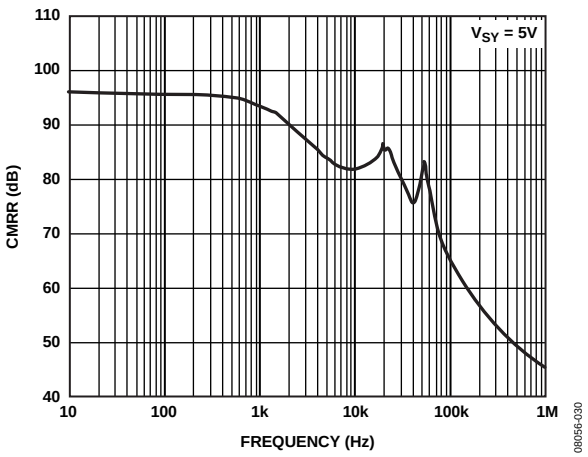


Figure 33. CMRR vs. Frequency

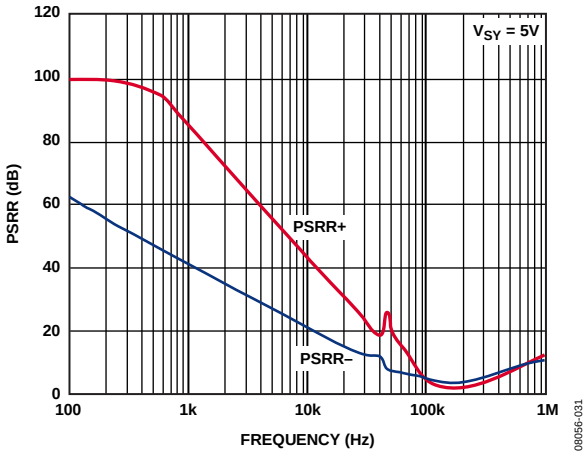


Figure 34. PSRR vs. Frequency

T_A = 25°C, unless otherwise noted.

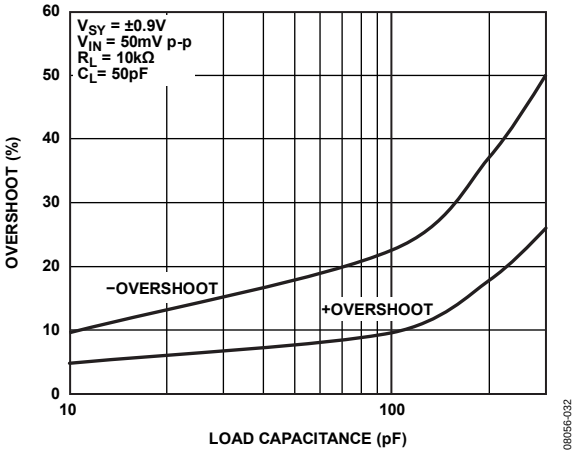


Figure 35. Small-Signal Overshoot vs. Load Capacitance

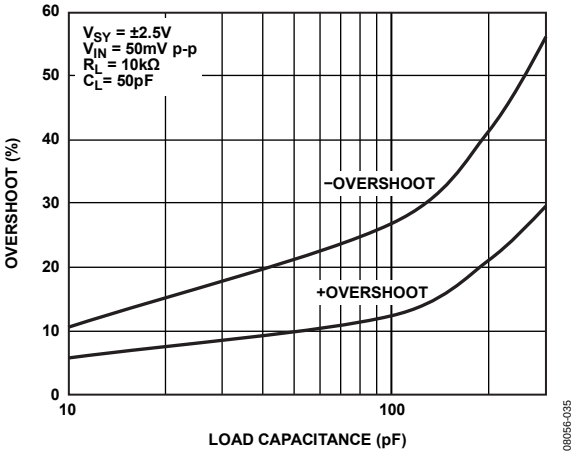


Figure 38. Small-Signal Overshoot vs. Load Capacitance

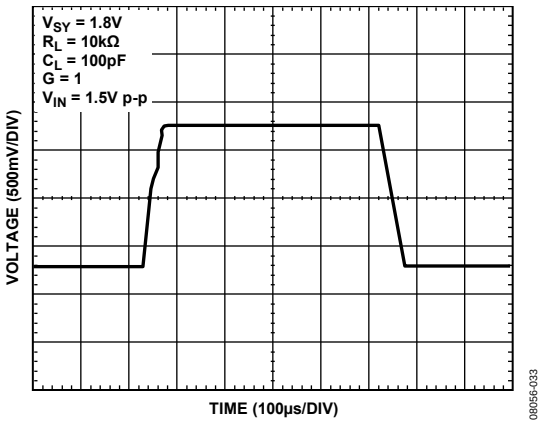


Figure 36. Large-Signal Transient Response

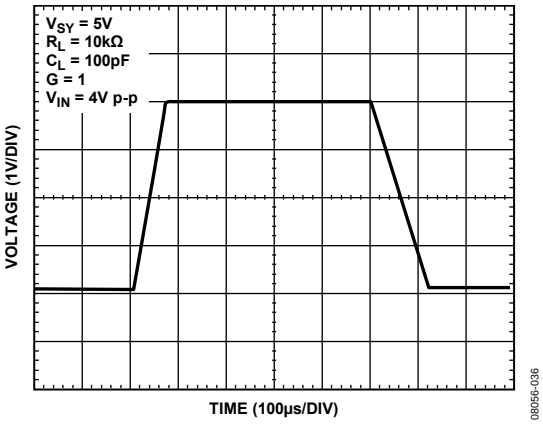


Figure 39. Large-Signal Transient Response

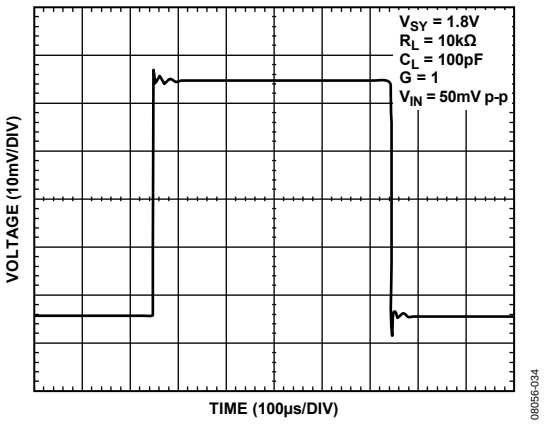


Figure 37. Small-Signal Transient Response

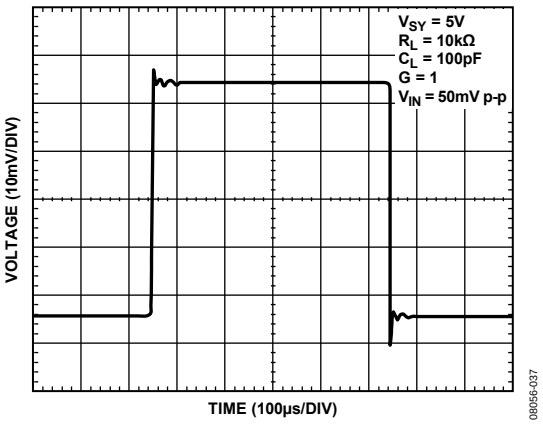


Figure 40. Small-Signal Transient Response

T_A = 25°C, unless otherwise noted.

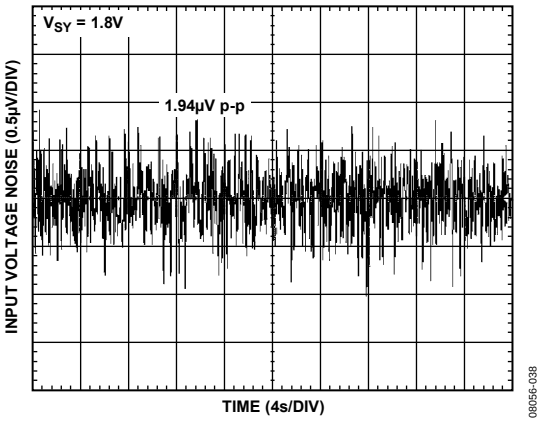


Figure 41. Input Voltage Noise, 0.1 Hz to 10 Hz

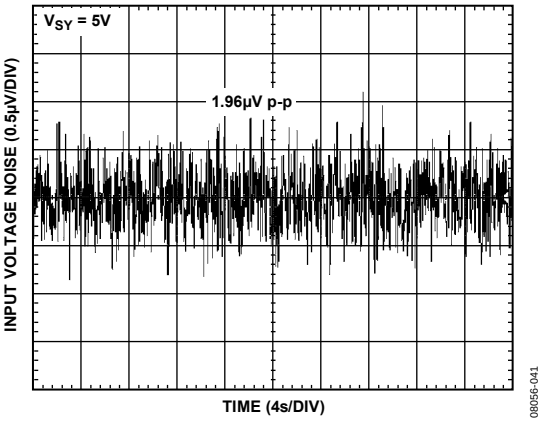


Figure 44. Input Voltage Noise, 0.1 Hz to 10 Hz

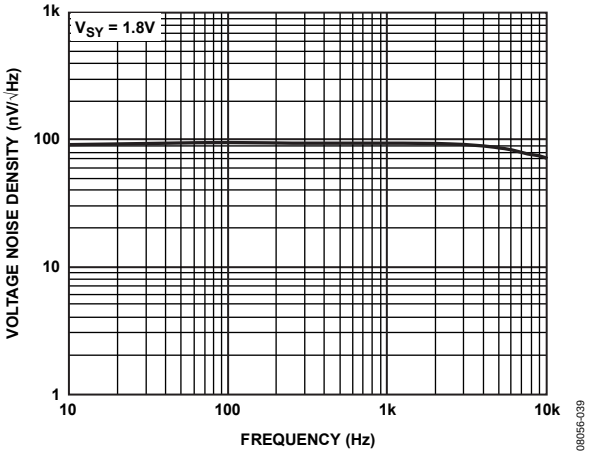


Figure 42. Voltage Noise Density vs. Frequency

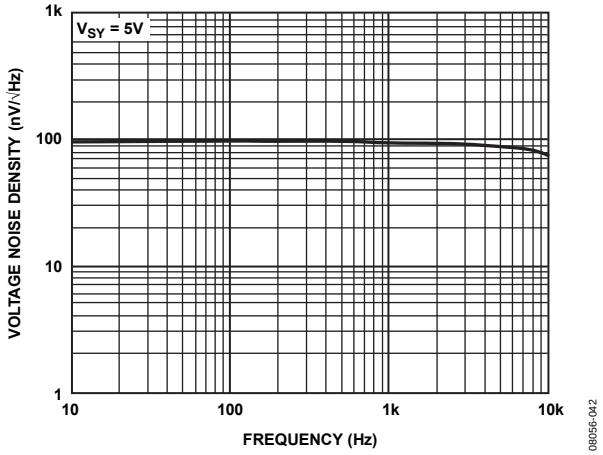


Figure 45. Voltage Noise Density vs. Frequency

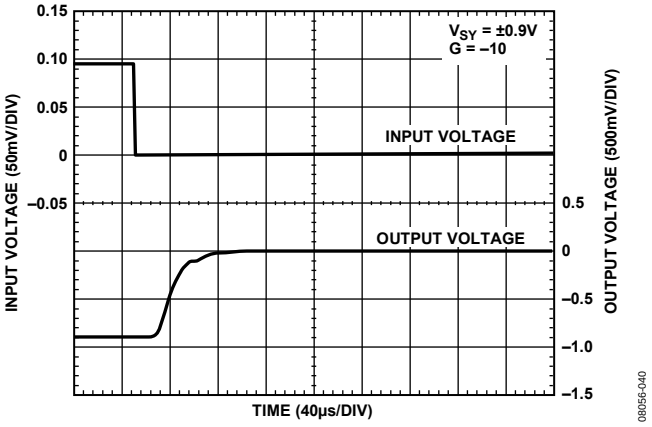


Figure 43. Positive Overload Recovery

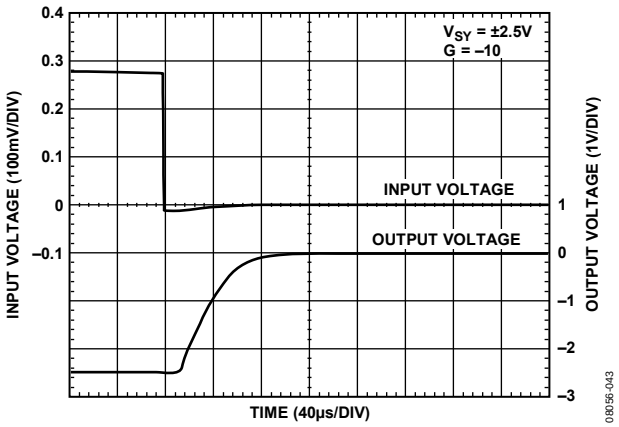


Figure 46. Positive Overload Recovery

T_A = 25°C, unless otherwise noted.

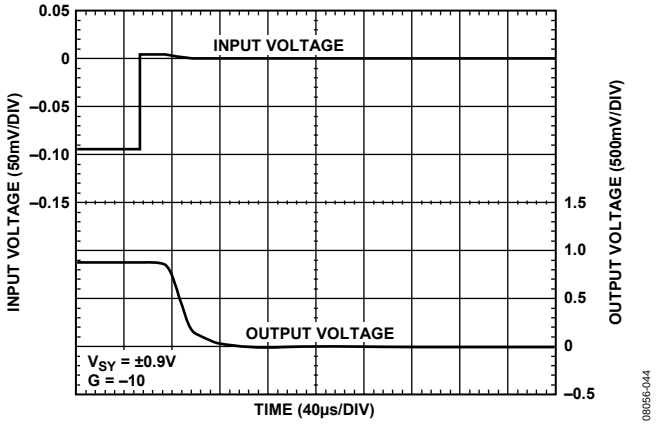


Figure 47. Negative Overload Recovery

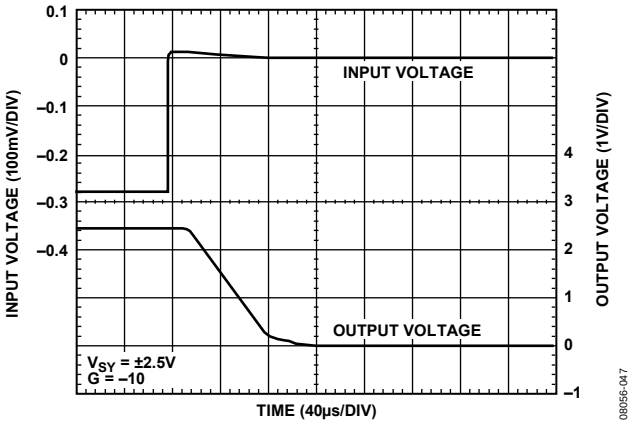


Figure 50. Negative Overload Recovery

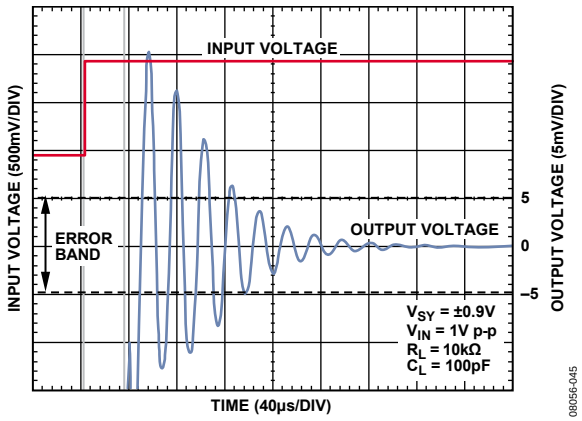


Figure 48. Positive Settling Time to 0.1%

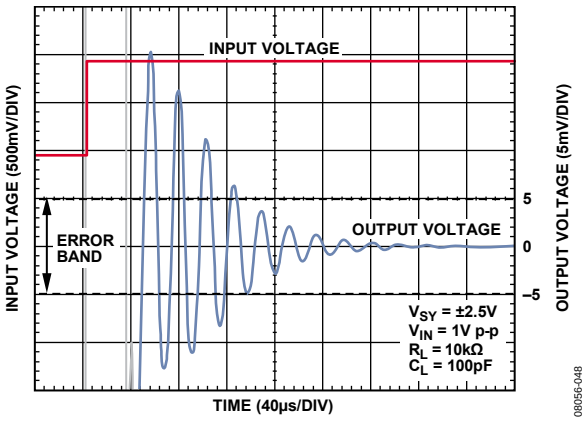


Figure 51. Positive Settling Time to 0.1%

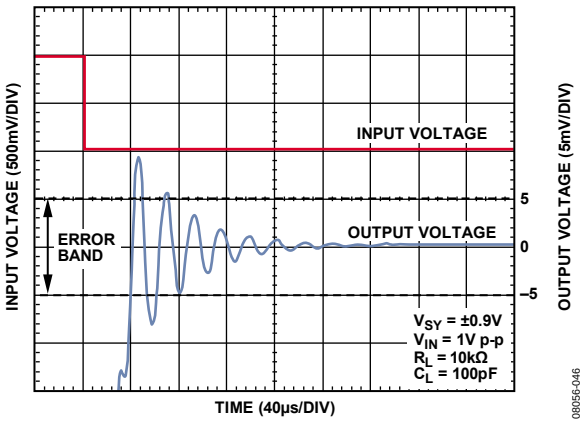


Figure 49. Negative Settling Time to 0.1%

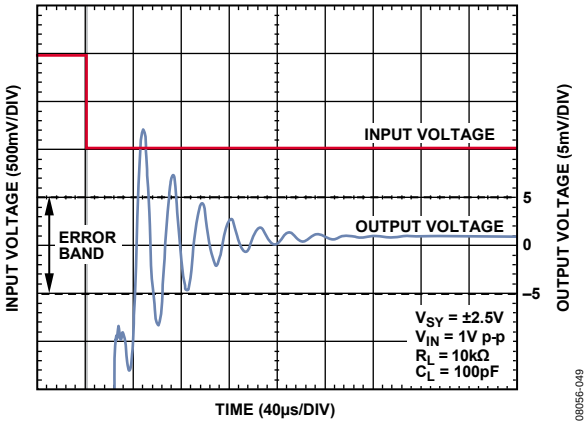


Figure 52. Negative Settling Time to 0.1%

T_A = 25°C, unless otherwise noted.

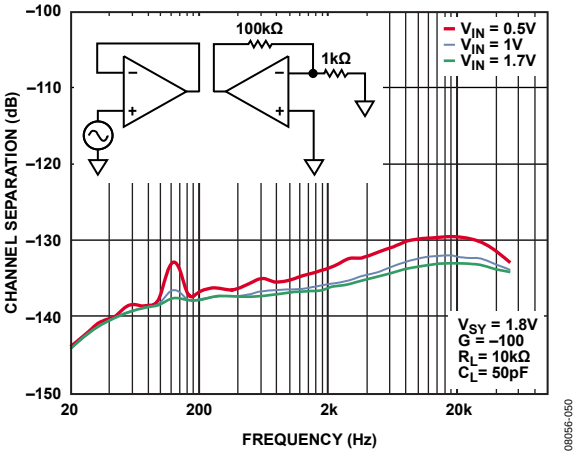


Figure 53. Channel Separation vs. Frequency

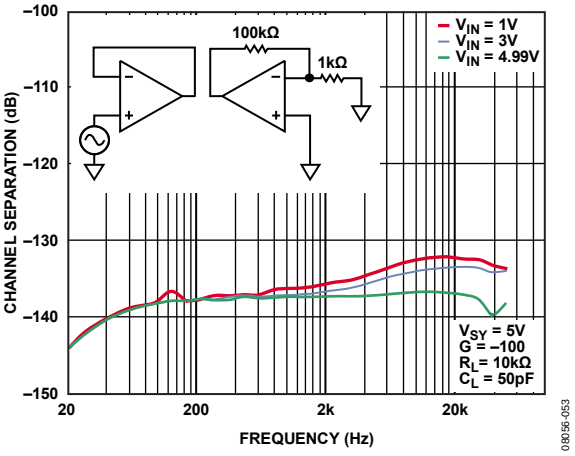


Figure 56. Channel Separation vs. Frequency

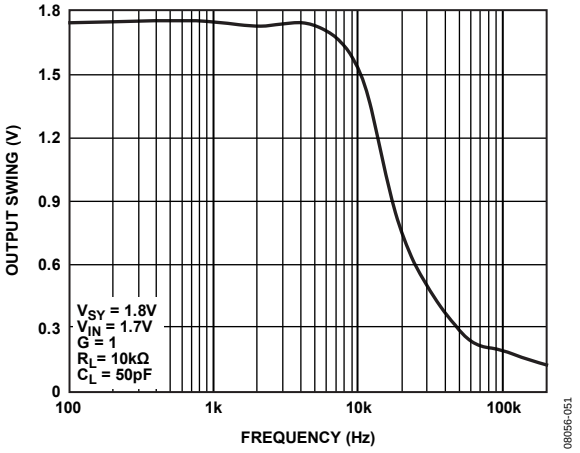


Figure 54. Output Swing vs. Frequency

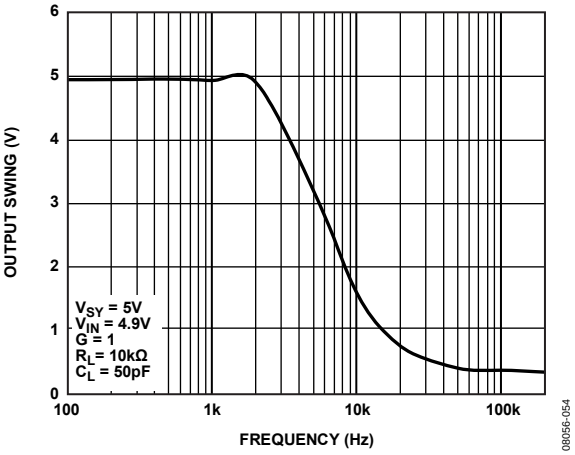


Figure 57. Output Swing vs. Frequency

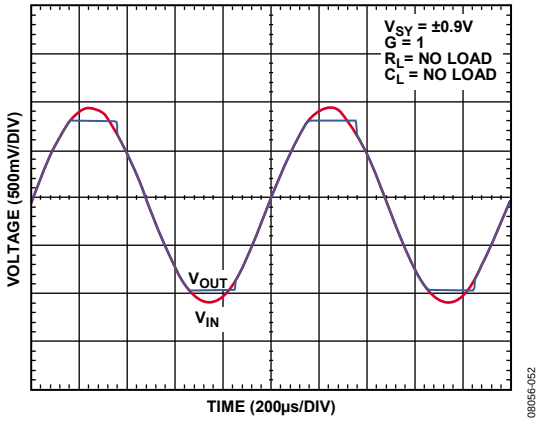


Figure 55. No Phase Reversal

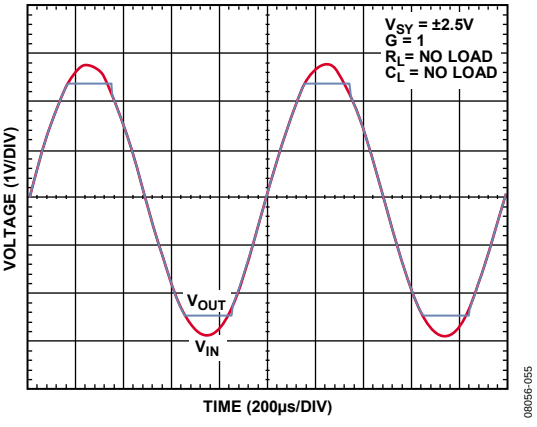


Figure 58. No Phase Reversal

THEORY OF OPERATION

The ADA4051-1/ADA4051-2 micropower chopper operational amplifiers feature a novel, patent-pending technique that suppresses offset-related ripple in a chopper amplifier. Instead of filtering the ripple in the ac domain, this technique nulls the initial offset of the amplifier in the dc domain, thus preventing ripple at the overall output.

Auto-zeroing and chopping are two techniques widely used in high precision CMOS amplifiers to achieve low offset, low offset drift, and no 1/f noise. Each of these techniques has pros and cons. Auto-zeroing results in more in-band noise due to aliasing introduced by sampling. On the other hand, chopping produces offset-related ripple because it modulates the initial offset associated with the amplifier up to its chopping frequency.

To accomplish the best noise vs. power trade-off, the chopping technique is the better approach when designing a low offset amplifier because there is no increased in-band noise. It is preferable to suppress the offset-related ripple inside a chopper amplifier because the offset-related ripple would otherwise need to be eliminated by an extra off-chip postfilter.

Figure 59 shows the block diagram design of the ADA4051-1/ADA4051-2 chopper amplifiers employing a local feedback loop called autocorrection feedback (ACFB). The main signal path contains an input chopping switch network (CHOP1), a first transconductance amplifier (Gm1), an output chopping switch network (CHOP2), a second transconductance amplifier (Gm2), and a third transconductance amplifier (Gm3). CHOP1 and CHOP2 operate at 40 kHz of chopping frequency to modulate the initial offset and 1/f noise from Gm1 up to the chopping frequency. A fourth transconductance amplifier (Gm4) in the ACFB senses the modulated ripple at the output of CHOP2, caused by the initial offset voltage of Gm1. Then, the ripple is demodulated down to a dc domain through a third chopping switch network (CHOP3), operating with the same chopping clock as CHOP1 and CHOP2. Finally, a null transconductance amplifier (Gm5) tries to null any dc component at the output of Gm1 that would otherwise appear in the overall output as ripple.

A switched-capacitor notch filter (NF) functions to selectively suppress the undesired offset-related ripple without disturbing the desired input signal from the overall input. The desired input dc signal appears as a dc signal at the output of CHOP2. Then, the initial offset is modulated up to the chopping frequency by CHOP3 and filtered out by the NF. Therefore, initial offset does not create any feedback and does not disturb the desired input signal. The NF is synchronized with the chopping clock to filter out the modulated component. In the same manner, the offset of Gm5 is filtered out by the combination of CHOP3 and the NF, enabling accurate ripple sensing at the output of CHOP2.

In parallel with the high dc gain path, a feedforward transconductance amplifier (Gm6) is added to bypass the phase shift introduced by the ACFB at the chopping frequency. Gm6 is designed to have the same transconductance as Gm1 to avoid pole-zero doublets. This design prevents any instability introduced by the ACFB in the overall feedback loop.

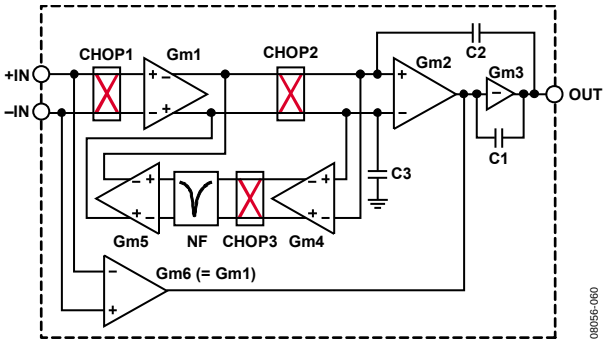


Figure 59. ADA4051-1/ADA4051-2 Chopper Amplifiers Block Diagram

The voltage noise density, which is equal to the thermal noise floor dominated by the Gm1, is essentially flat from dc to the chopping frequency because CHOP1 and CHOP2 eliminate the 1/f noise generated in Gm1 and the ACFB does not contribute any additional noise. Although the ACFB suppresses the ripple related to the chopping, there is a remaining voltage ripple. To further suppress the remaining ripple down to a desired level, it is recommended to have a postfilter at the output of the amplifier.

The remaining voltage ripple originates from two sources. The first type of ripple is due to the residual ripple associated with the initial offset of the Gm1. It is proportional to the magnitude of the initial offset and creates a spectrum at the chopping frequency (f_{CHOP}). When the amplifier is configured as a unity-gain buffer, this ripple has a typical value of 4.9 µV rms and a maximum of 34.7 µV rms. The second type of ripple is due to the intermodulation between the high frequency input signal and the chopping frequency. This ripple depends on the input frequency (f_{IN}) and creates a spectrum at frequencies equal to the difference between the chopping frequency and the input frequency ($f_{CHOP} - f_{IN}$), as well as at frequencies equal to the summation of the chopping frequency and the input frequency ($f_{CHOP} + f_{IN}$). The magnitude of the ripple for different input frequencies is shown in Figure 60.

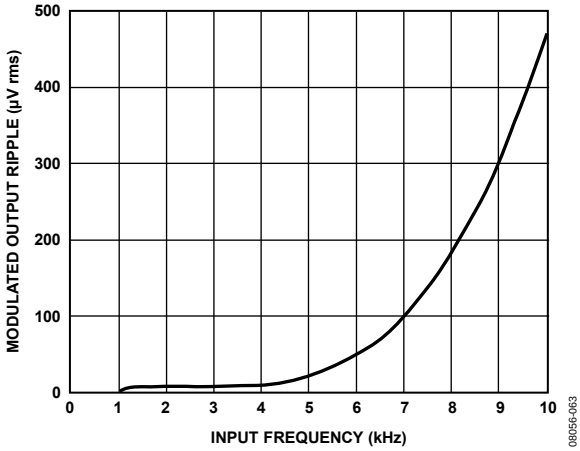


Figure 60. ADA4051-1/ADA4051-2 Modulated Output Ripple vs. Input Frequency

The design architecture of the ADA4051-1/ADA4051-2 specifically targets precision signal conditioning applications requiring accurate and stable performance from dc to 10 Hz bandwidth. In summary, the main features of the ADA4051-1/ADA4051-2 chopper amplifiers are

- Considerable suppression of the offset-related ripple
- No effect on the desired input signal as long as its frequency is much lower than the chopping frequency shown in Figure 60
- Achievement of low offset similar to a conventional chopper amplifier
- No introduction of excess noise

The ADA4051-1/ADA4051-2 chopper amplifiers provide a rail-to-rail input range with a 1.8 V to 5.5 V supply voltage range and 20 µA supply current consumption over the −40°C to +125°C extended industrial temperature range. The gain bandwidth is 125 kHz as a unity-gain stable amplifier up to 100 pF load capacitance.

INPUT VOLTAGE RANGE

The ADA4051-1/ADA4051-2 have internal ESD protection diodes. These diodes are connected between the inputs and each supply rail to protect the input MOSFETs from an electrical discharge event and are reversed-biased during normal operation. This protection scheme allows voltages as high as approximately 0.3 V beyond the supplies ($\pm V_{SY}$ ± 0.3 V) to be applied at the input of either terminal without causing permanent damage.

If either input exceeds one of the supply rails by more than 0.3 V, these ESD diodes become forward-biased and large amounts of current begin to flow through them. Without current limiting, this excessive current would cause permanent damage to the device. If the inputs are expected to be subject to overvoltage conditions, install a resistor in series with each input to limit the input current to 10 mA maximum.

The ADA4051-1/ADA4051-2 also have internal circuitry that protects the input stage from high differential voltages. This circuitry is composed of internal 1.33 kΩ resistors in series with each input and back-to-back diode-connected N-MOSFET (with a typical V_T of 0.7 V for a V_{CM} of 0 V) after these series resistors. With normal negative feedback operating conditions, the ADA4051-1/ADA4051-2 amplifiers correct their output to ensure that the two inputs are at the same voltage. However, if the device is configured as a comparator or there are unusual operating conditions, the input voltages can be forced to different potentials, which may cause excessive current to flow through the internal diode-connected N-MOSFETs.

Although the ADA4051-1/ADA4051-2 are rail-to-rail input amplifiers, take care to ensure that the potential difference between the inputs does not exceed $\pm V_{SY}$ to avert permanent damage to the device.

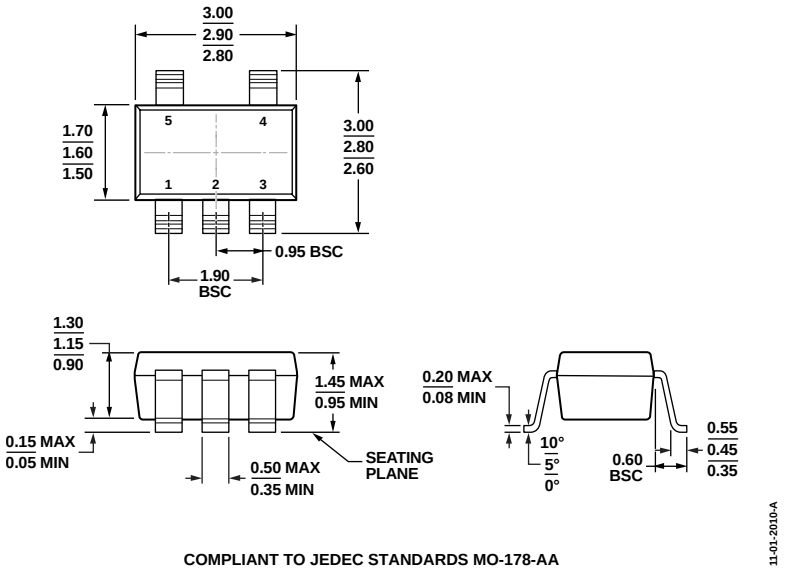
OUTPUT PHASE REVERSAL

Although output phase reversal can occur with other amplifiers when the input common-mode voltage range is exceeded, the ADA4051-1/ADA4051-2 amplifiers are designed to prevent any output phase reversal, provided both inputs are maintained approximately within 0.3 V above and below the supply voltages ($\pm V_{SY}$ ± 0.3 V).

With other amplifiers, the outputs may jump in the opposite direction to the supply rail when a common-mode voltage moves outside the common-mode range. This usually occurs when one of the internal stages of the amplifier no longer has sufficient bias voltage across it and subsequently turns off.

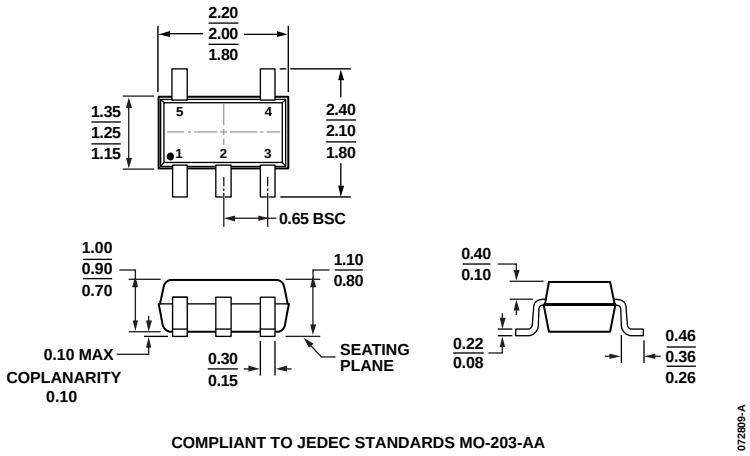
However, with the ADA4051-1/ADA4051-2 amplifiers, if one or both inputs exceed the input voltage range but remain within the $\pm V_{SY}$ ± 0.3 V range, an internal loop opens and the output remains in saturation mode, without phase reversal, until the input voltage is brought back to within the input voltage range limits as shown in Figure 55 and Figure 58.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 61. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 62. 5-Lead Thin Shrink Small Outline Transistor Package [SC-70]
(KS-5)
Dimensions shown in millimeters

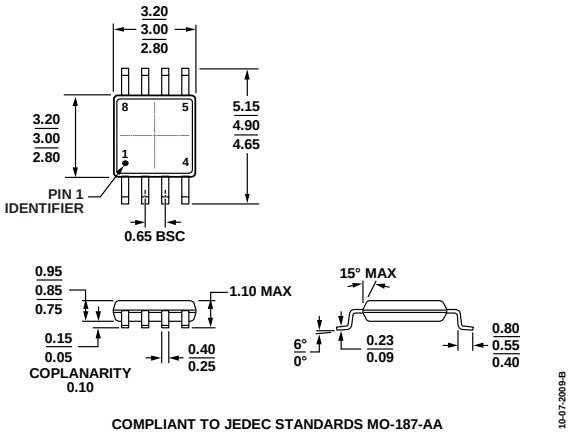


Figure 63. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

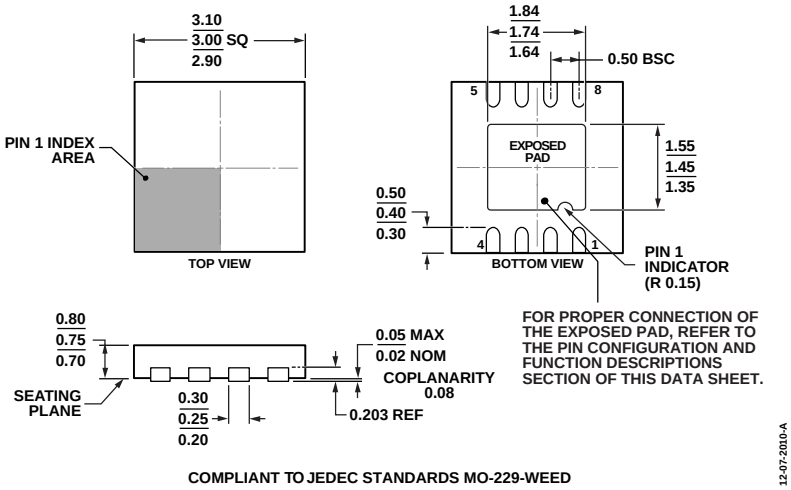


Figure 64. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4051-1ARJZ-R2	−40°C to +125°C	5-Lead Small Outline Transistor Package [SOT-23]	RJ-5	A0U
ADA4051-1ARJZ-R7	−40°C to +125°C	5-Lead Small Outline Transistor Package [SOT-23]	RJ-5	A0U
ADA4051-1ARJZ-RL	−40°C to +125°C	5-Lead Small Outline Transistor Package [SOT-23]	RJ-5	A0U
ADA4051-1AKSZ-R2	−40°C to +125°C	5-Lead Thin Shrink Small Outline Transistor Package [SC-70]	KS-5	A0U
ADA4051-1AKSZ-R7	−40°C to +125°C	5-Lead Thin Shrink Small Outline Transistor Package [SC-70]	KS-5	A0U
ADA4051-1AKSZ-RL	−40°C to +125°C	5-Lead Thin Shrink Small Outline Transistor Package [SC-70]	KS-5	A0U
ADA4051-2ACPZ-R2	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	A2M
ADA4051-2ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	A2M
ADA4051-2ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	A2M
ADA4051-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2M
ADA4051-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2M
ADA4051-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2M

[1] Z = RoHS Compliant Part.

NOTES

NOTES