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12/09—Rev. C to Rev. D

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ±5.0 V

V_S = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			20	75	μV
		−40°C < T_A < +125°C		30	125	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
AD8671				0.3	0.5	μV/°C
AD8672/AD8674				0.3	0.8	μV/°C
Input Bias Current	I_B		−12	+3	+12	nA
		+25°C < T_A < +125°C	−20	+5	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Offset Current	I_{OS}		−12	+6	+12	nA
		+25°C < T_A < +125°C	−20	+6	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Voltage Range			−2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −2.5 V to +2.5 V	100	120		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −3 V to +3 V	1000	6000		V/mV
Input Capacitance, Common Mode	C_{INCM}			6.25		pF
Input Capacitance, Differential Mode	C_{INDM}			7.5		pF
Input Resistance, Common Mode	R_{IN}			3.5		GΩ
Input Resistance, Differential Mode	R_{INDM}			15		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ, −40°C to +125°C	+3.8	+4.0		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ, −40°C to +125°C		−3.9	−3.8	V
Output Voltage High	V_{OH}	R_L = 600 Ω	+3.7	+3.9		V
Output Voltage Low	V_{OL}	R_L = 600 Ω		−3.8	−3.7	V
Output Current	I_{OUT}			±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V				
AD8671/AD8672			110	130		dB
AD8674			106	115		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3	3.5	mA
		−40°C < T_A < +125°C			4.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		4		V/μs
Settling Time	t_S	To 0.1% (4 V step, G = 1)		1.4		μs
		To 0.01% (4 V step, G = 1)		5.1		μs
Gain Bandwidth Product	GBP			10		MHz
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		77	100	nV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8	3.8	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.3		pA/√Hz
Channel Separation						
AD8672/AD8674	C_S	f = 1 kHz		−130		dB
		f = 10 kHz		−105		dB

ELECTRICAL CHARACTERISTICS, ±15 V

V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			20	75	µV
		−40°C < T_A < +125°C		30	125	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
AD8671				0.3	0.5	µV/°C
AD8672/AD8674				0.3	0.8	µV/°C
Input Bias Current	I_B		−12	+3	+12	nA
		+25°C < T_A < +125°C	−20	+5	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Offset Current	I_{OS}		−12	+6	+12	nA
		+25°C < T_A < +125°C	−20	+6	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Voltage Range			−12		+12	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12 V to +12 V	100	120		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −10 V to +10 V	1000	6000		V/mV
Input Capacitance, Common Mode	C_{INCM}			6.25		pF
Input Capacitance, Differential Mode	C_{INDM}			7.5		pF
Input Resistance, Common Mode	R_{IN}			3.5		GΩ
Input Resistance, Differential Mode	R_{INDM}			15		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ, −40°C to +125°C	+13.2	+13.8		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ, −40°C to +125°C		−13.8	−13.2	V
Output Voltage High	V_{OH}	R_L = 600 Ω	+11	+12.3		V
Output Voltage Low	V_{OL}	R_L = 600 Ω		−12.4	−11	V
Output Current	I_{OUT}			±20		mA
Short Circuit Current	I_{SC}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V				
AD8671/AD8672			110	130		dB
AD8674			106	115		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3	3.5	mA
		−40°C < T_A < +125°C			4.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		4		V/µs
Settling Time	t_S	To 0.1% (10 V step, G = 1)		2.2		µs
		To 0.01% (10 V step, G = 1)		6.3		µs
Gain Bandwidth Product	GBP			10		MHz
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		77	100	nV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8	3.8	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.3		pA/√Hz
Channel Separation						
AD8672/AD8674	C_S	f = 1 kHz		−130		dB
		f = 10 kHz		−105		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.[1]

Parameter	Rating
Supply Voltage	36 V
Input Voltage	V_S- to V_S+
Differential Input Voltage	±0.7 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
All Packages	−65°C to +150°C
Operating Temperature Range	
8-Lead Packages	−40°C to +125°C
14-Lead Packages	−40°C to +85°C
Junction Temperature Range	
All Packages	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

[1] Absolute maximum ratings apply at 25°C, unless otherwise noted.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

See the Applications section for a related discussion on power.

Table 5. Package Characteristics

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead MSOP (RM)	142	44	°C/W
8-Lead SOIC_N (R)	120	43	°C/W
14-Lead SOIC_N (R)	90	36	°C/W
14-Lead TSSOP (RU)	112	35	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is., θ_{JA} is specified for the device soldered on a 4-layer circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

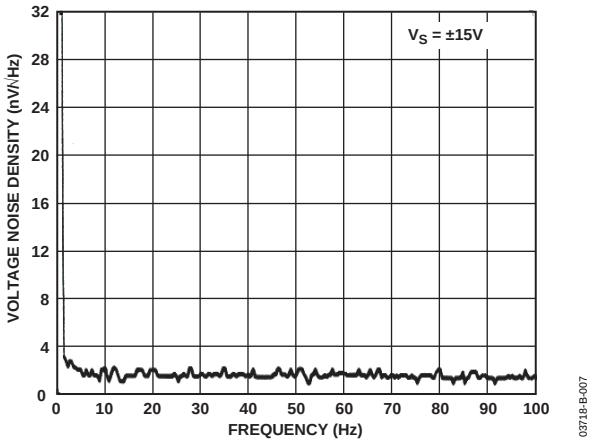


Figure 4. Voltage Noise Density vs. Frequency

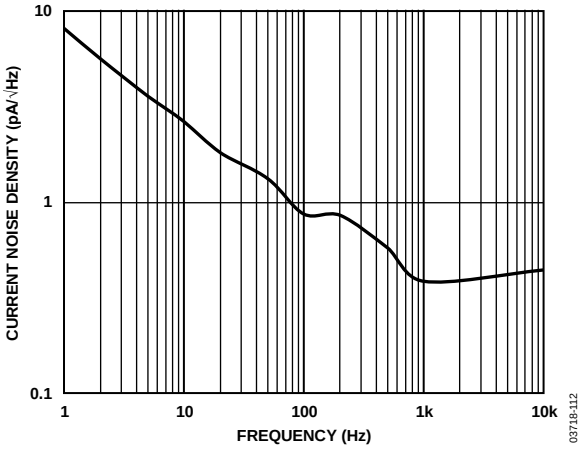


Figure 7. Current Noise Density V_S = ±15 V

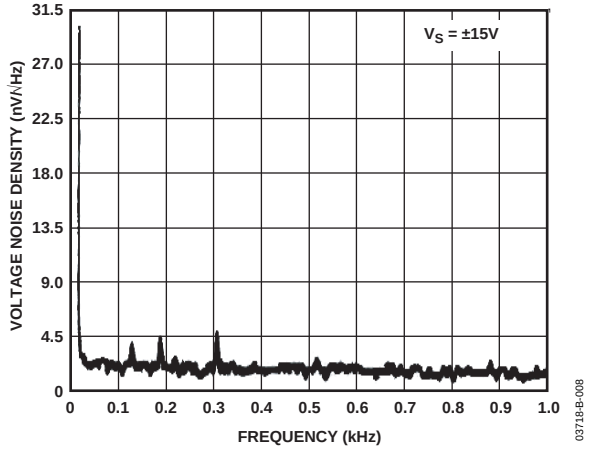


Figure 5. Voltage Noise Density vs. Frequency

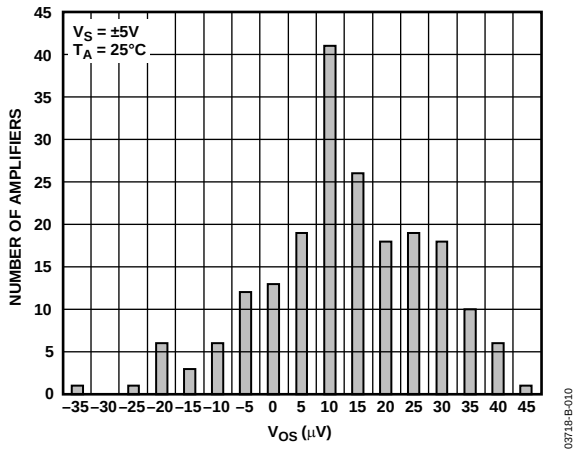


Figure 8. Input Offset Voltage Distribution

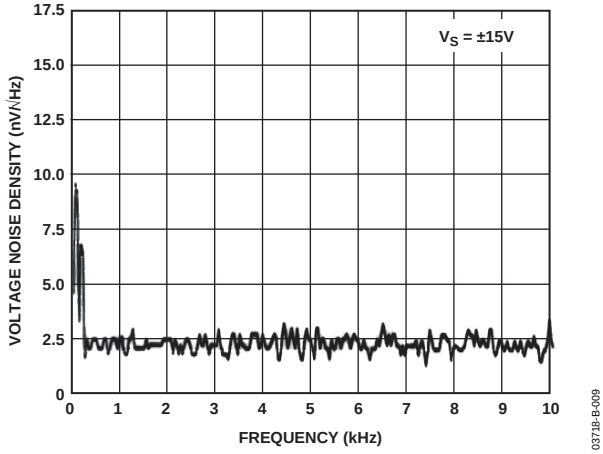


Figure 6. Voltage Noise Density vs. Frequency

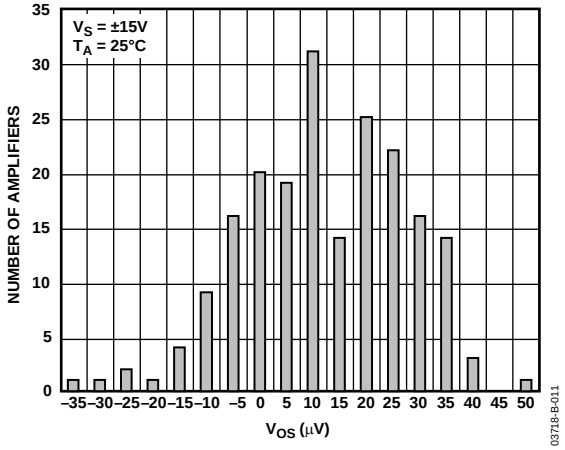


Figure 9. Input Offset Voltage Distribution

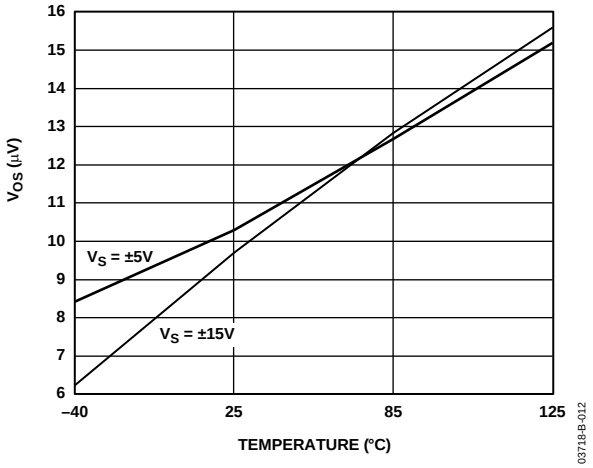


Figure 10. Input Offset Voltage vs. Temperature

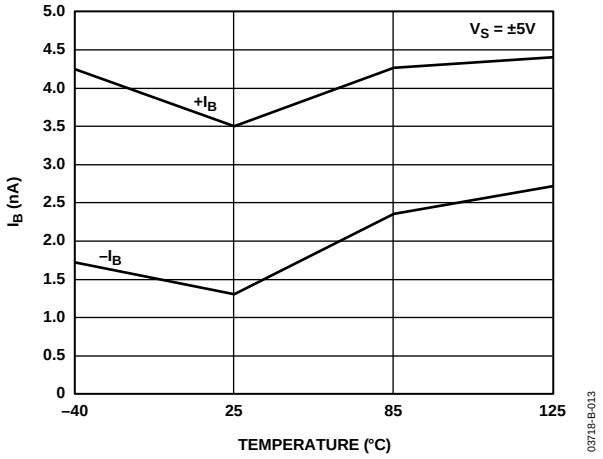


Figure 11. Input Bias Current vs. Temperature

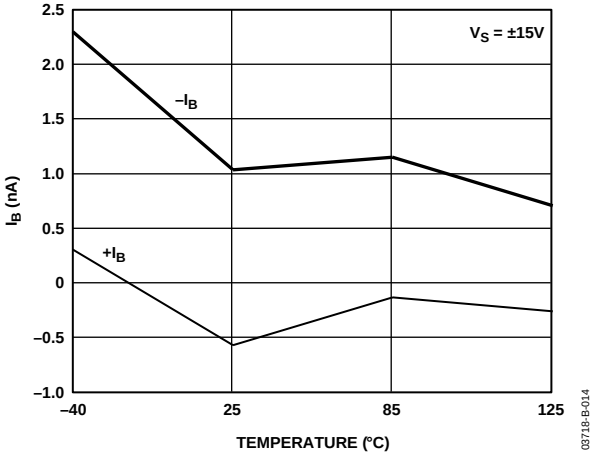


Figure 12. Input Bias Current vs. Temperature

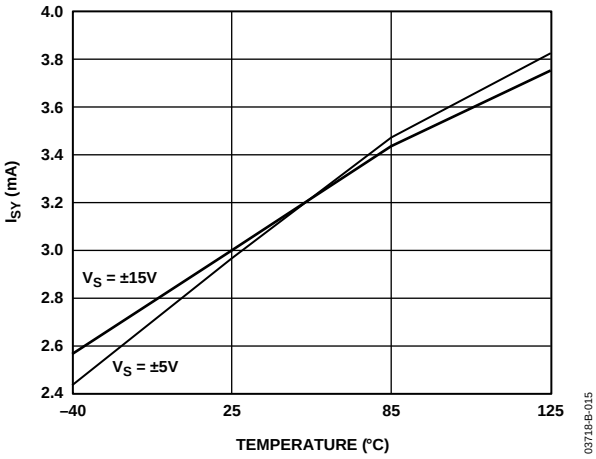


Figure 13. Supply Current vs. Temperature

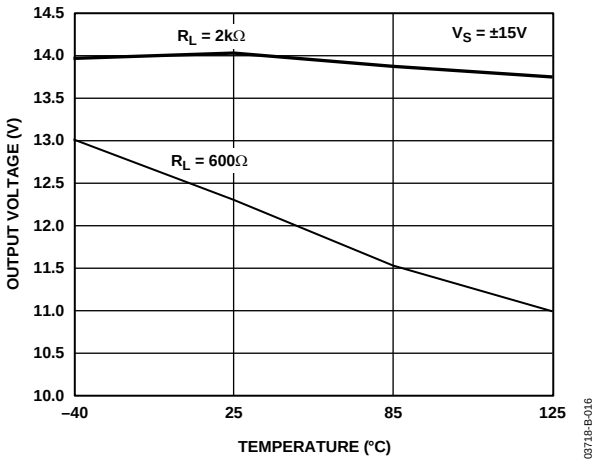


Figure 14. Output Voltage High vs. Temperature

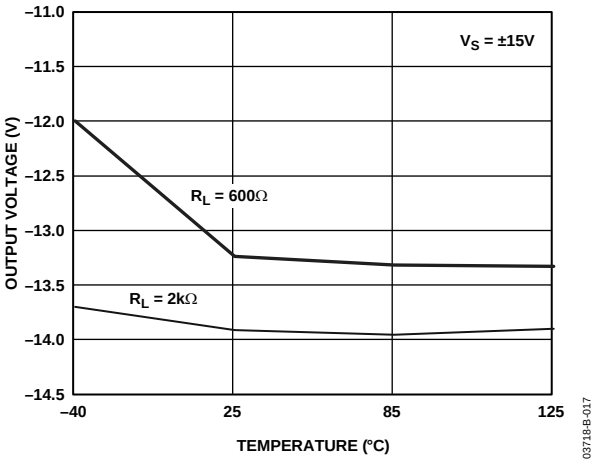


Figure 15. Output Voltage Low vs. Temperature

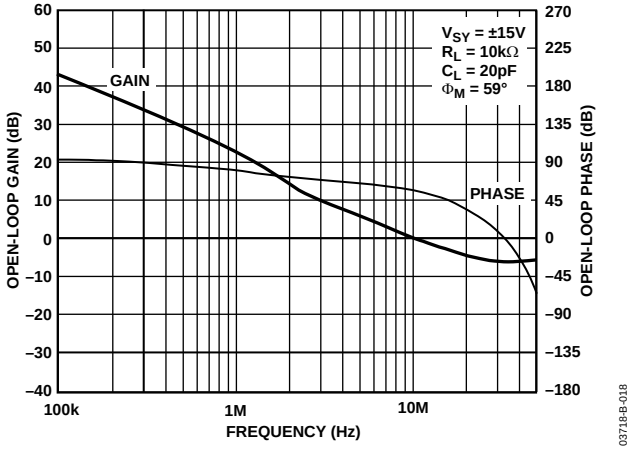


Figure 16. Open-Loop Gain and Phase Shift vs. Frequency

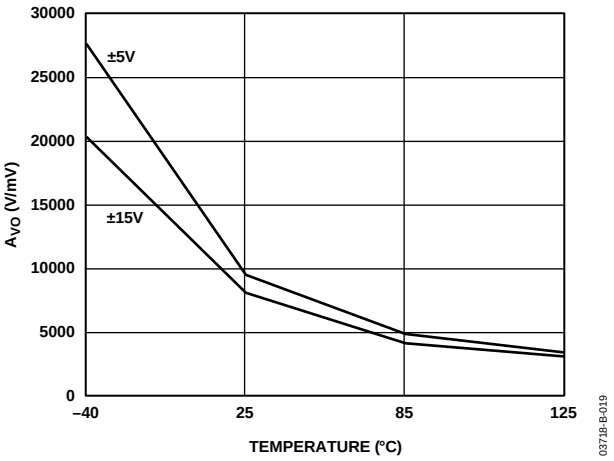


Figure 17. Open-Loop Gain vs. Temperature

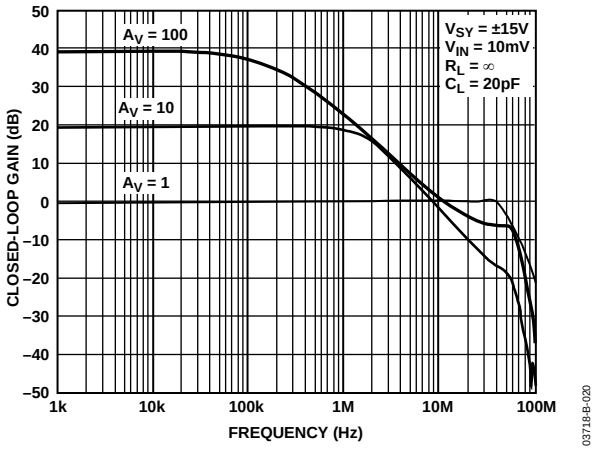


Figure 18. Closed-Loop Gain vs. Frequency

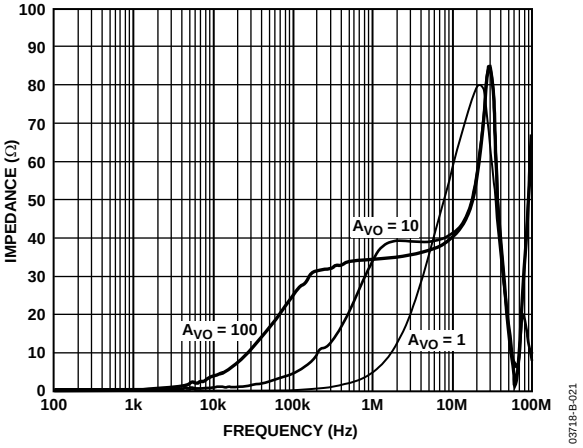


Figure 19. Output Impedance vs. Frequency

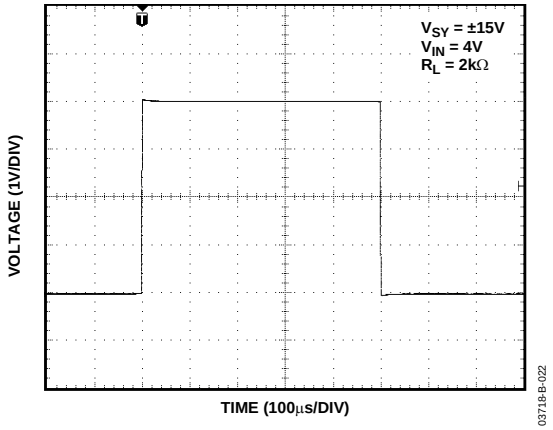


Figure 20. Large Signal Transient Response

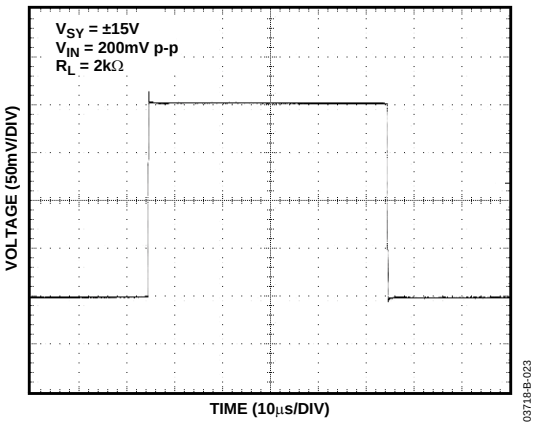


Figure 21. Small Signal Transient Response

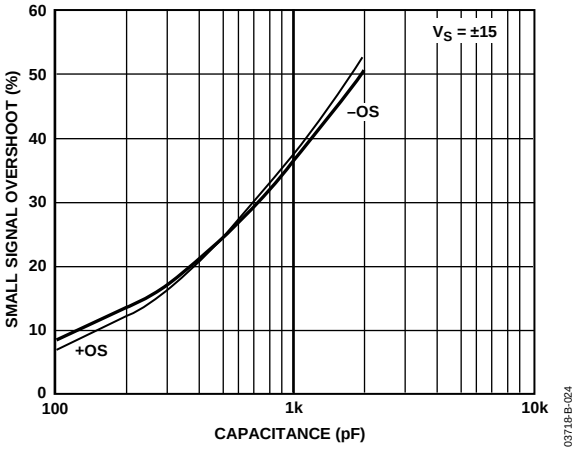


Figure 22. Small Signal Overshoot vs. Load Capacitance

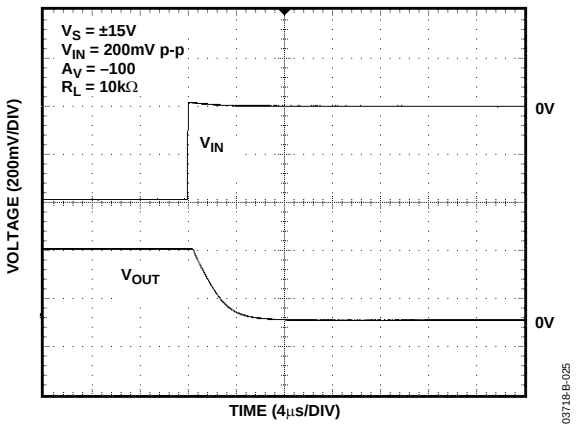


Figure 23. Positive Overdrive Recovery

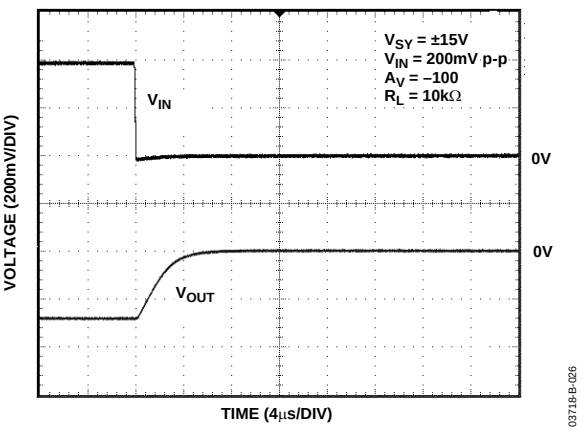


Figure 24. Negative Overdrive Recovery

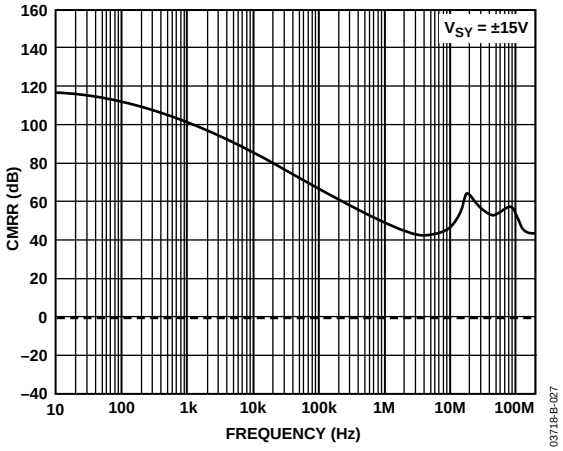


Figure 25. CMRR vs. Frequency

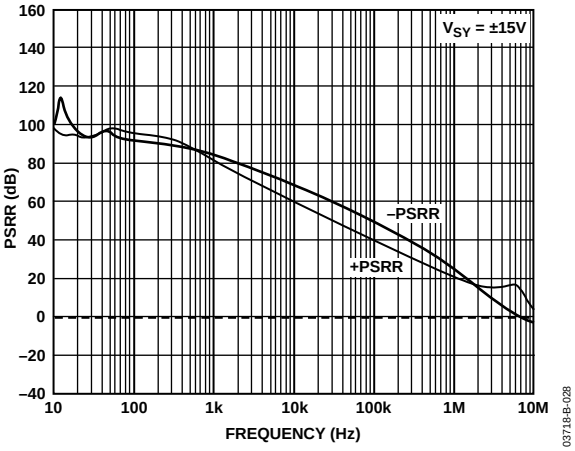


Figure 26. PSRR vs. Frequency

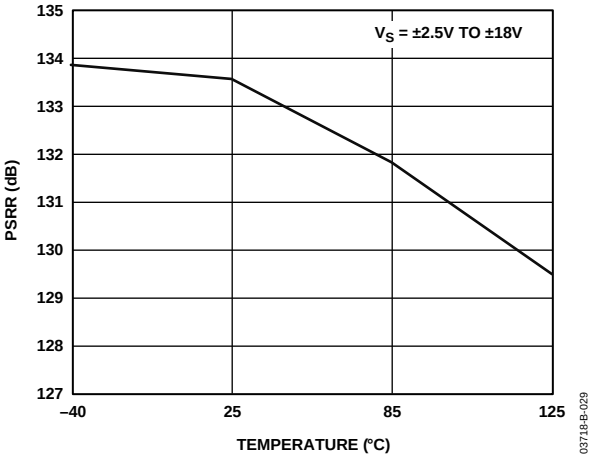


Figure 27. PSRR vs. Temperature

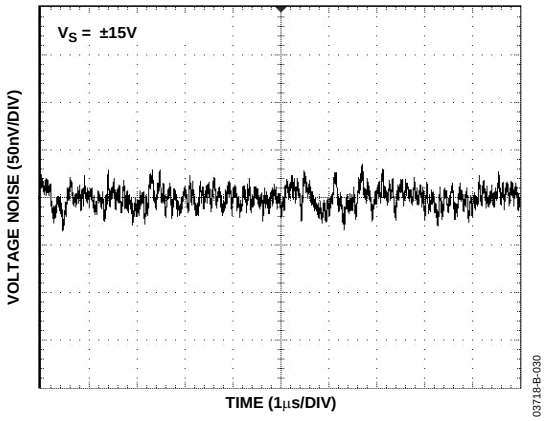


Figure 28. 0.1 Hz to 10 Hz Input Voltage Noise

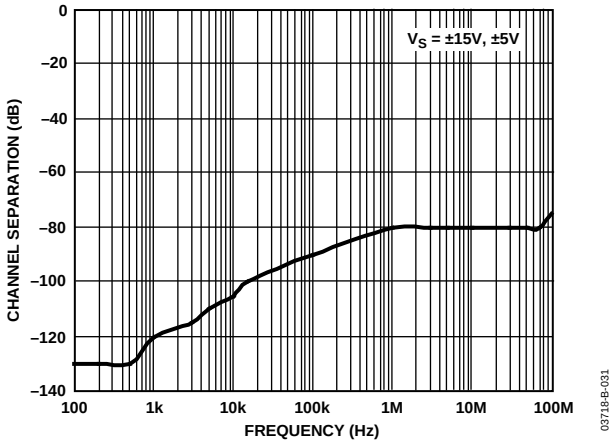


Figure 29. Channel Separation

APPLICATIONS

POWER DISSIPATION CALCULATIONS

To achieve low voltage noise in a bipolar op amp, the current must be increased. The emitter-base theoretical voltage noise is approximately

$$e_n = 10^9 kT\sqrt{\frac{2}{qI_C}}\ \text{nV}/\sqrt{\text{Hz}}$$

To achieve the low voltage noise of 2.8 nV/√Hz, the input stage current is higher than most op amps with an equivalent gain bandwidth product. The thermal noise of a 1 kΩ resistor is 4 nV/√Hz, which is higher than the voltage noise of AD8671 family. Low voltage noise requires using low values of resistors, so low voltage noise op amps should have good drive capability, such as a 600 Ω load. This means that the second stage and output stage are also biased at higher currents. As a result, the supply current of a single op amp is 3.5 mA maximum at room temperature.

Junction temperature has a direct affect on reliability. For more information, visit the following Analog Devices, Inc., website: http://www.analog.com/en/quality-and-reliability/reliability-data/content/index.html

MTTF and FIT calculations can be done based on the junction temperature and IC process. Use the following equation to determine the junction temperature:

$$T_J = T_A + P_D \times \theta_{JA}$$

For the AD8671 single in the 8-lead MSOP package, the thermal resistance, θ_{JA}, is 142°C/W. If the ambient temperature is 30°C and the supply voltages are ±12 V, the power dissipation is

24 V × 3.5 mA = 84 mW

Therefore, the rise above ambient temperature is

84 mW × 142°C/W = 12°C

If the ambient temperature is 30°C, the junction temperature is 42°C. The previously mentioned website that details the effect of the junction temperature on reliability has a calculator that requires only the part number and the junction temperature to determine the process technology.

For the AD8674 single in the 14-Lead TSSOP package, the thermal resistance, θ_{JA}, is 112°C/W. Although θ_{JA} is lower than it is for the 8-lead package, the four op amps are powered simultaneously. If the ambient temperature is 50°C and the supply voltages are ±15 V, the power dissipation is

30 V × 4.2 mA × four op amps = 504 mW

Therefore, the rise above ambient temperature is

504 mW × 112°C/W = 56°C

With an ambient temperature of 50°C, the junction temperature is 106°C. This is less than the specified absolute maximum junction temperature, but for systems with long product lifetimes (years), this should be considered carefully.

Note that these calculations do not include the additional dissipation caused by the load current on each op amp. Possible solutions to reduce junction temperature include system level considerations such as fans, Peltier thermoelectric coolers, and heat pipes. Board considerations include operation on lower voltages, such as ±12 V or ±5 V, and using two dual op amps instead of one quad op amp. If the extremely low voltage noise and high gain bandwidth is not required, using other quad op amps, such as ADA4091-4, OP4177, ADA4004-4, OP497, or AD704 can be considered.

UNITY-GAIN FOLLOWER APPLICATIONS

When large transient pulses (>1 V) are applied at the positive terminal of amplifiers (such as the OP27, LT1007, OPA227, and AD8671) with back-to-back diodes at the input stage, the use of a resistor in the feedback loop is recommended to avoid having the amplifier load the signal generator. The feedback resistor, R_F, should be at least 500 Ω. However, if large values must be used for R_F, a small capacitor, C_F, should be inserted in parallel with R_F to compensate for the pole introduced by the input capacitance and R_F.

Figure 30 shows the uncompensated output response with a 10 kΩ resistor in the feedback and the compensated response with C_F = 15 pF.

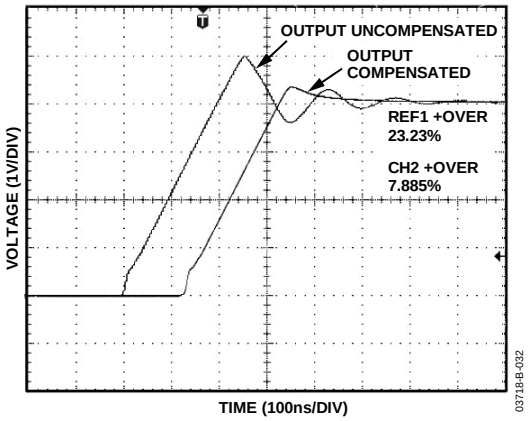


Figure 30. Transient Output Response

OUTPUT PHASE REVERSAL

Phase reversal is a change of polarity in the amplifier transfer function that occurs when the input voltage exceeds the supply voltage. The AD8671/AD8672/AD8674 do not exhibit phase reversal even when the input voltage is 1 V beyond the supplies.

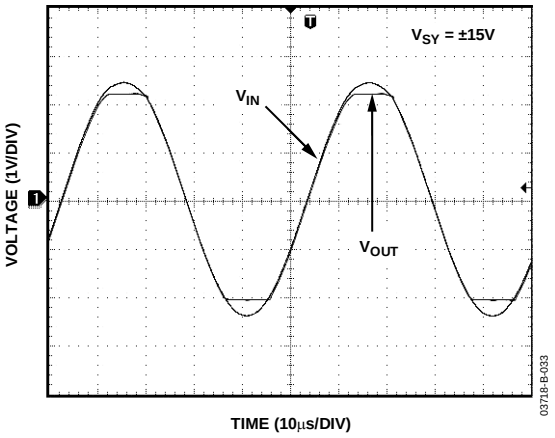


Figure 31. Output Phase Reversal

TOTAL NOISE VS. SOURCE RESISTANCE

The low input voltage noise of the AD8671/AD8672/AD8674 makes them a great choice for applications with low source resistance. However, because they have low input current noise, they can also be used in circuits with substantial source resistance.

Figure 32 shows the voltage noise, current noise, thermal noise, and total rms noise of the AD8671 as a function of the source resistance.

For R_S < 475 Ω, the input voltage noise, e_n, dominates.
For 475 Ω < R_S < 412 kΩ, thermal noise dominates.
For R_S > 412 kΩ, the input current noise dominates.

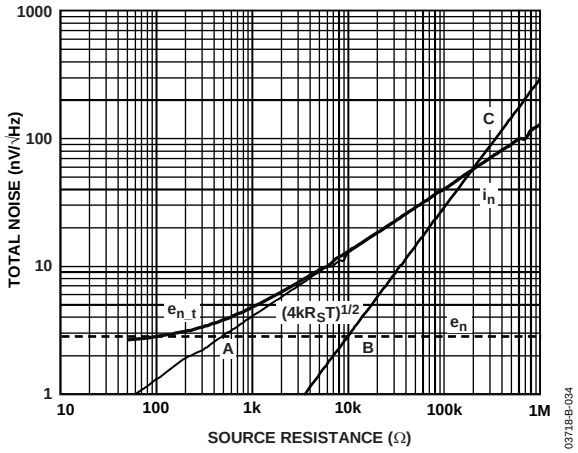


Figure 32. Noise vs. Source Resistance

TOTAL HARMONIC DISTORTION (THD) AND NOISE

The AD8671/AD8672/AD8674 exhibit low total harmonic distortion (THD) over the entire audio frequency range. This makes them suitable for applications with high closed-loop gains, including audio applications. Figure 33 shows approximately 0.0006% of THD + N in a positive unity gain, the worst-case configuration for distortion.

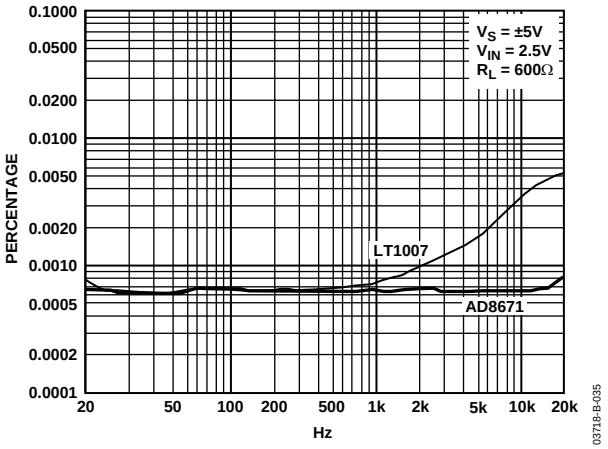


Figure 33. Total Harmonic Distortion and Noise

DRIVING CAPACITIVE LOADS

The AD8671/AD8672/AD8674 can drive large capacitive loads without causing instability. However, when configured in unity gain, driving very large loads can cause unwanted ringing or instability.

Figure 34 shows the output of the AD8671 with a capacitive load of 1 nF. If heavier loads are used in low closed-loop gain or unity-gain configurations, it is recommended to use external compensation as shown in the circuit in Figure 35. This technique reduces the overshoot and prevents the op amp from oscillation. The trade-off of this circuit is a reduction in output swing. However, a great added benefit stems from the fact that the input signal and the op amp's noise are filtered, and thus the overall output noise is kept to a minimum.

The output response of the circuit is shown in Figure 36.

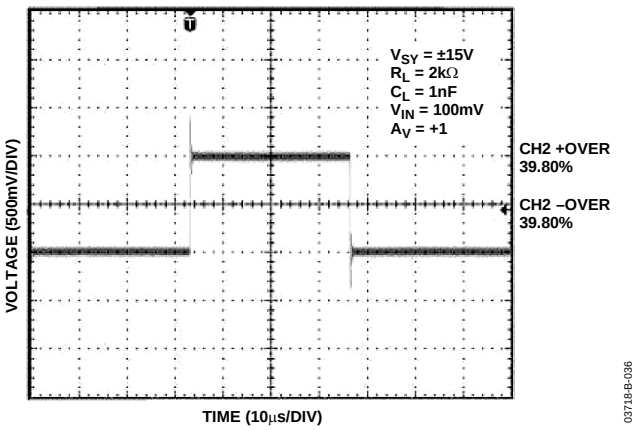


Figure 34. AD8671 Capacitive Load Drive

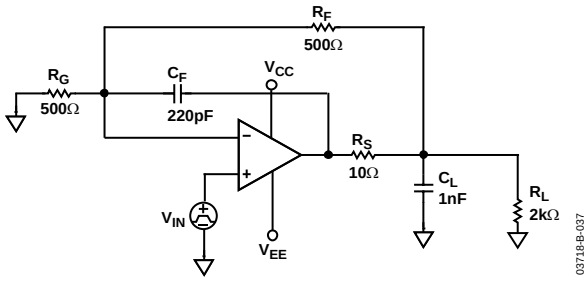


Figure 35. Recommended Capacitive Load Circuit

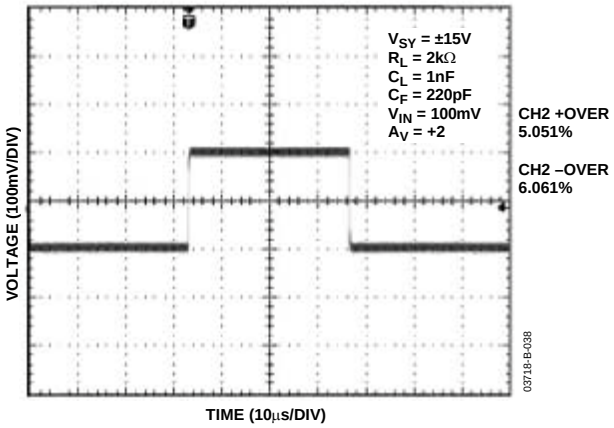


Figure 36. Compensated Load Drive

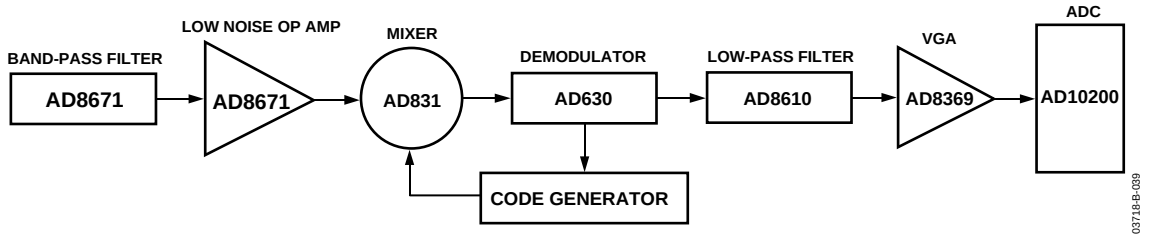


Figure 37. Simplified Block Diagram of a GPS Receiver

GPS RECEIVER

GPS receivers require low noise to minimize RF effects. The precision of the AD8671 makes it an excellent choice for such applications. Its very low noise and wide bandwidth make it suitable for band-pass and low-pass filters without the penalty of high power consumption.

Figure 37 shows a simplified block diagram of a GPS receiver. The next section details the design equations.

BAND-PASS FILTER

Filters are useful in many applications; for example, band-pass filters are used in GPS systems, as discussed in the previous section. Figure 38 shows a second-order band-pass KRC filter.

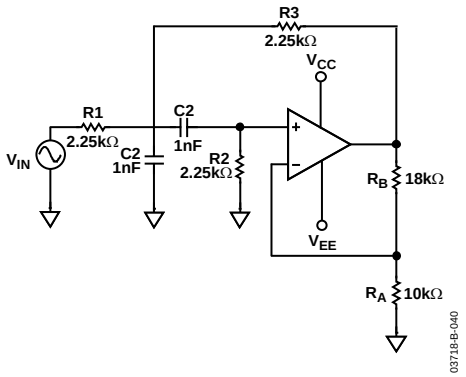


Figure 38. Band-Pass KRC Filter

The equal component topology yields a center frequency

$$fo = \frac{\sqrt{2}}{2\pi RC}$$

$$\text{and } Q = \frac{\sqrt{2}}{4-K}$$

where:

$$K = 1 + \frac{R_B}{R_A}$$

The band-pass response is shown in Figure 39.

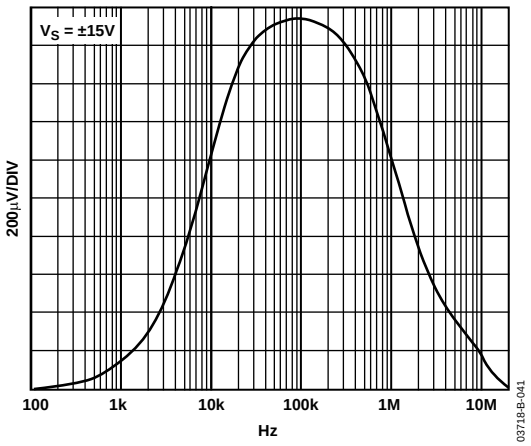


Figure 39. Band-Pass Response

PLL SYNTHESIZERS AND LOOP FILTERS

Phase-lock loop filters are used in AM/FM modulation.

Loop filters in PLL design require accuracy and care in their implementation. The AD8671/AD8672/AD8674 are ideal candidates for such filter design; the low offset voltage and low input bias current minimize the output error. In addition to the excellent dc specifications, the AD8671/AD8672/AD8674 have a unique performance at high frequencies; the high open-loop gain and wide bandwidth allow the user to design a filter with a high closed-loop gain if desirable. To optimize the filter design, it is recommended to use small value resistors to minimize the thermal noise. A simple example is shown in Figure 40.

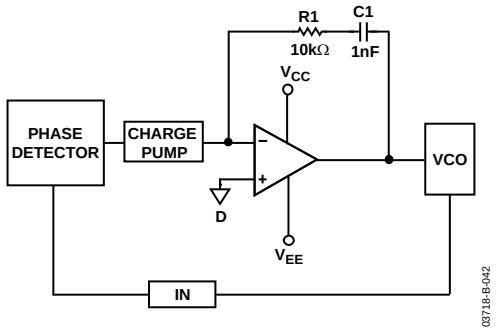


Figure 40. PLL Filter Simplified Block Diagram

OUTLINE DIMENSIONS

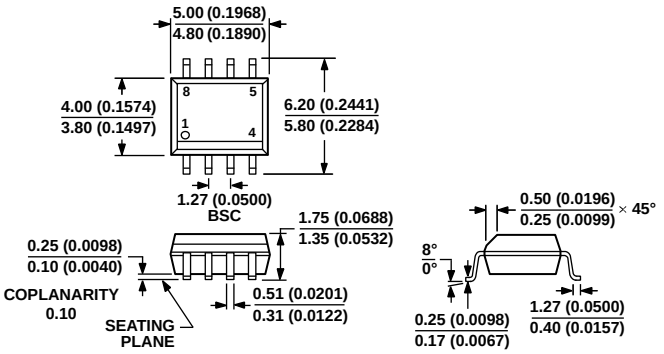


Figure 41. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

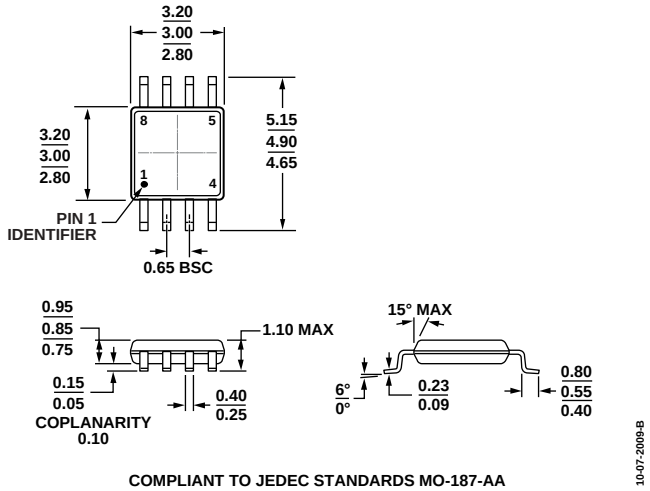
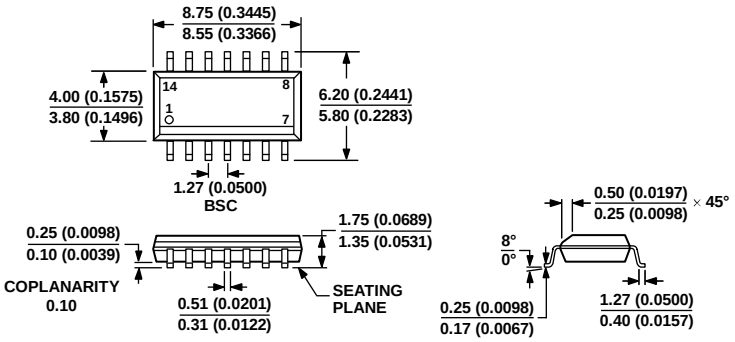


Figure 42. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

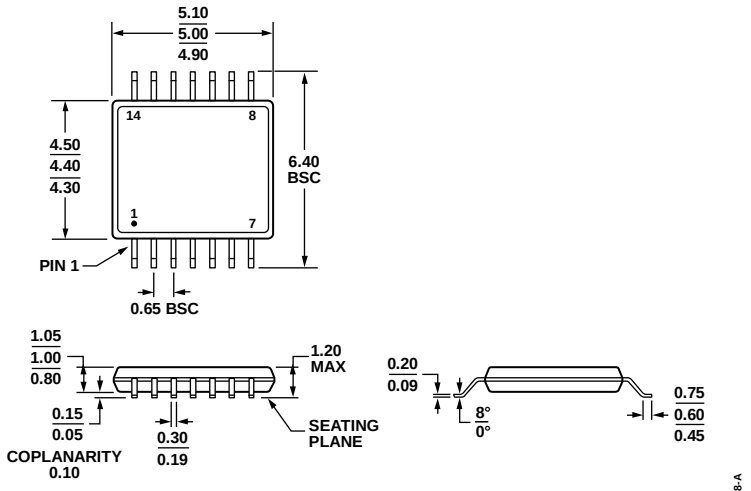


COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 43. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

061908-A

Figure 44. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8671ARZ	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARZ-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARZ-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARMZ	–40°C to +125°C	8-Lead MSOP	RM-8	A0V
AD8671ARMZ-REEL	–40°C to +125°C	8-Lead MSOP	RM-8	A0V
AD8672AR	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672AR-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672AR-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARZ	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARZ-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARZ-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARMZ	–40°C to +125°C	8-Lead MSOP	RM-8	A0W
AD8672ARMZ-REEL	–40°C to +125°C	8-Lead MSOP	RM-8	A0W
AD8674ARZ	–40°C to +85°C	14-Lead SOIC_N	R-14	
AD8674ARZ-REEL	–40°C to +85°C	14-Lead SOIC_N	R-14	
AD8674ARZ-REEL7	–40°C to +85°C	14-Lead SOIC_N	R-14	
AD8674ARU	–40°C to +85°C	14-Lead TSSOP	RU-14	
AD8674ARUZ	–40°C to +85°C	14-Lead TSSOP	RU-14	
AD8674ARUZ-REEL	–40°C to +85°C	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part.

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