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REVISION HISTORY

3/16—Rev. 0 to Rev. A

Changed CP-24 to CP-24-10 ... Universal
Changes to Figure 4 and Table 5 ... 6
Added Test Circuit Section ... 12
Moved Figure 33; Renumbered Sequentially ... 12
Updated Outline Dimensions ... 16
Changes to Ordering Guide ... 16

7/04—Revision 0: Initial Version

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SPECIFICATIONS

V_S = ±5V, V_{OCM} = 0 V @ 25°C, $R_{L, dm}$ = 200 Ω, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT PERFORMANCE					
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_O = 0.2 V p-p		450		MHz
−3 dB Large Signal Bandwidth	V_O = 2 V p-p		225		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		60		MHz
	V_O = 2 V p-p		55		MHz
Slew Rate	V_O = 2 V p-p, 25% to 75%		1600		V/µs
Settling Time to 0.1%	V_O = 2 V Step		15		ns
Isolation between Amplifiers	f = 10 MHz, between Amplifiers A and B		81		dB
DIFFERENTIAL INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range			−5 to +5		V
Input Resistance	Differential		1.5		kΩ
	Single-Ended Input		1.13		kΩ
Input Capacitance	Differential		1		pF
DC CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V		−50		dB
DIFFERENTIAL OUTPUT CHARACTERISTICS					
Differential Signal Gain	$\Delta V_{OUT, dm}/\Delta V_{IN, dm}$; $\Delta V_{IN, dm}$ = ±1 V	1.925	1.960	2.000	V/V
Output Voltage Swing	Each Single-Ended Output	V_{S-} + 1.9		V_{S+} − 1.6	V
Output Offset Voltage		−24	+4	+24	mV
Output Offset Drift	T_{MIN} to T_{MAX}		±30		µV/°C
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{IN, dm}$, $\Delta V_{OUT, dm}$ = 2 V p-p, f = 50 MHz		−60		dB
	DC		−70	−58	dB
Output Voltage Noise (RTO)	f = 1 MHz		25		nV/√Hz
Output Short-Circuit Current			90		mA
V_{OCM} to $V_{O, cm}$ PERFORMANCE					
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth	ΔV_{OCM} = 100 mV p-p		330		MHz
Slew Rate	V_{OCM} = −1 V to +1 V, 25% to 75%		1000		V/µs
DC Gain	ΔV_{OCM} = ±1 V	0.980	0.995	1.005	V/V
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range			±3.1		V
Input Resistance			70		kΩ
Input Offset Voltage		−15	−6	+15	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		±50		µV/°C
DC CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V		−42		dB
POWER SUPPLY					
Operating Range		+4.5		±6	V
Quiescent Current			28	29	mA
PSRR	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V		−84	−76	dB
OUTPUT PULL-DOWN PERFORMANCE					
OPD Input Low Voltage			V_{S-} to V_{S+} − 4.15		V
OPD Input High Voltage			V_{S+} − 3.15 to V_{S+}		V
OPD Input Bias Current			67	90	µA
OPD Assert Time			100		ns
OPD De-Assert Time			100		ns
Output Voltage When OPD Asserted	Each Output, OPD Input @ V_S+		V_{S-} + 0.86	V_{S-} + 0.90	V

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V_S = 5 V, V_{OCM} = 2.5 V @ 25°C, $R_{L, dm}$ = 200 Ω, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT PERFORMANCE					
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_O = 0.2 V p-p		400		MHz
−3 dB Large Signal Bandwidth	V_O = 2 V p-p		200		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		50		MHz
Slew Rate	V_O = 2 V p-p, 25% to 75%		1400		V/µs
Settling Time to 0.1%	V_O = 2 V Step		14		ns
Isolation Between Amplifiers	f = 10 MHz, between Amplifiers A and B		75		dB
DIFFERENTIAL INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range			0 to 5		V
Input Resistance	Differential		1.5		kΩ
	Single-Ended Input		1.13		kΩ
Input Capacitance	Differential		1		pF
DC CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V		−50		dB
DIFFERENTIAL OUTPUT CHARACTERISTICS					
Differential Signal Gain	$\Delta V_{OUT, dm}/\Delta V_{IN, dm}$; $\Delta V_{IN, dm}$ = ±1 V	1.925	1.960	2.000	
Output Voltage Swing	Each Single-Ended Output	V_{S-} + 1.25		V_{S+} − 1.15	V
Output Offset Voltage		−24	+4	+24	mV
Output Offset Drift	T_{MIN} to T_{MAX}		±30		µV/°C
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{IN, dm}$, $\Delta V_{OUT, dm}$ = 2 V p-p, f = 50 MHz		−60		dB
	DC		−70	−58	dB
Output Voltage Noise (RTO)	f = 1 MHz		25		nV/√Hz
Output Short-Circuit Current			90		mA
V_{OCM} PERFORMANCE					
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth	ΔV_{OCM} = 100 mV p-p		290		MHz
Slew Rate	V_{OCM} = −1 V to +1 V, 25% to 75%		700		V/µs
DC Gain	ΔV_{OCM} = ±1 V, T_{MIN} to T_{MAX}	0.980	0.995	1.005	V/V
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range			1.25 to 3.85		V
Input Resistance			70		kΩ
Input Offset Voltage		−15	+2	+15	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		±50		µV/°C
DC CMRR	$\Delta V_{O, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−42		dB
POWER SUPPLY					
Operating Range		+4.5		±6	V
Quiescent Current			26	27	mA
PSRR	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V		−84	−76	dB
OUTPUT PULL-DOWN PERFORMANCE					
OPD Input Low Voltage			V_{S-} to V_{S+} − 3.85		V
OPD Input High Voltage			V_{S+} − 2.85 to V_{S+}		V
OPD Input Bias Current			63	80	µA
OPD Assert Time			100		ns
OPD De-Assert Time			100		ns
Output Voltage When OPD Asserted	Each Output, OPD Input @ V_S+		V_{S-} + 0.79	V_{S-} + 0.82	V

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ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12 V
All V_{OCM}	$\pm V_S$
Power Dissipation	See Figure 3
Input Common-Mode Voltage	$\pm V_S$
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 4. Thermal Resistance with the Underside Pad Connected to the Plane

Package Type/PCB Type	θ_{JA}	Unit
24-Lead LFCSP/4-Layer	70	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the AD8133 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8133. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The load current consists of differential and common-mode currents flowing to the loads, as well as currents flowing through the internal differential and common-mode feedback loops. The internal resistor tap used in the common-mode feedback loop places a 4 kΩ differential load on the output. RMS output voltages should be considered when dealing with ac signals.

Airflow reduces θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a copper plane in order to achieve the specified θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package versus ambient temperature for the 24-lead LFCSP (70°C/W) package on a JEDEC standard 4-layer board with the underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

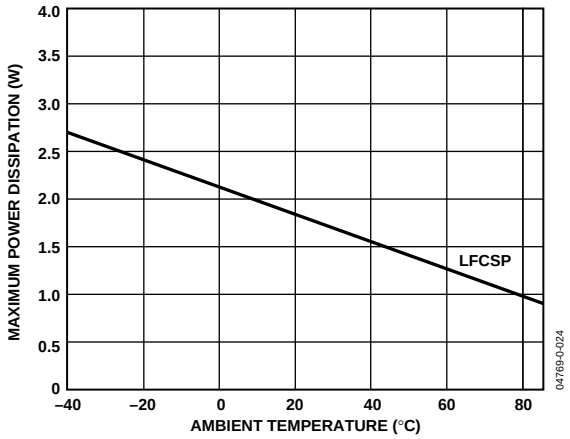

Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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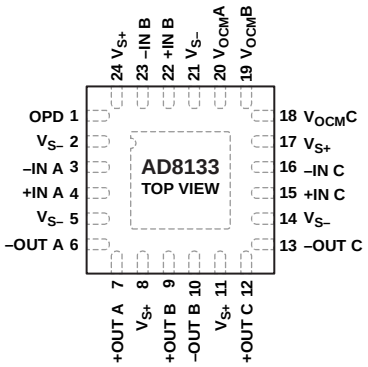
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PADDLE MUST BE SOLDERED TO A PAD ON TOP OF THE BOARD THAT IS CONNECTED TO AN INNER PLANE WITH SEVERAL THERMAL VIAS.

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Figure 4. 24-Lead LFCSP

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OPD	Output Pull-Down.
2, 5, 14, 21	V_{S-}	Negative Power Supply Voltage.
3	−IN A	Inverting Input, Amplifier A.
4	+IN A	Noninverting Input, Amplifier A.
6	−OUT A	Negative Output, Amplifier A.
7	+OUT A	Positive Output, Amplifier A.
8, 11, 17, 24	V_{S+}	Positive Power Supply Voltage.
9	+OUT B	Positive Output, Amplifier B.
10	−OUT B	Negative Output, Amplifier B.
12	+OUT C	Positive Output, Amplifier C.
13	−OUT C	Negative Output, Amplifier C.
15	+IN C	Noninverting Input, Amplifier C.
16	−IN C	Inverting Input, Amplifier C.
18	V_{OCM}C	Voltage Applied to This Pin Controls Output Common-Mode Voltage, Amplifier C.
19	V_{OCM}B	Voltage Applied to This Pin Controls Output Common-Mode Voltage, Amplifier B.
20	V_{OCM}A	Voltage Applied to This Pin Controls Output Common-Mode Voltage, Amplifier A.
22	+IN B	Noninverting Input, Amplifier B.
23	−IN B	Inverting Input, Amplifier B.
	EPAD	Exposed Pad. The exposed paddle must be soldered to a pad on top of the board that is connected to an inner plane with several thermal vias.

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, $R_{L, dm}$ = 200 Ω, V_S = ±5 V, T_A = 25°C, $V_{OCM}A = V_{OCM}B = V_{OCM}C$ = 0 V. Refer to the basic test circuit in Figure 33 for the definition of terms.

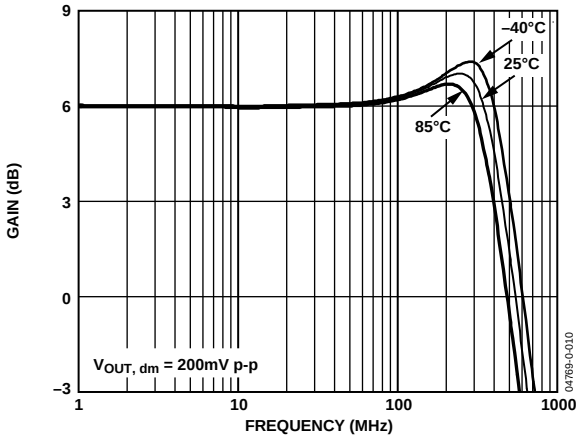

Figure 5. Small Signal Frequency Response at Various Temperatures

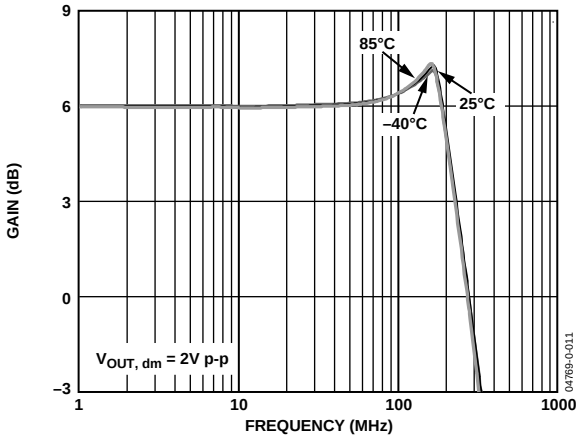

Figure 8. Large Signal Frequency Response at Various Temperatures

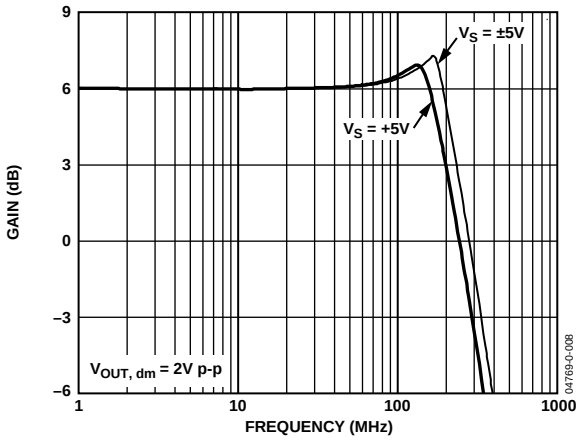

Figure 6. Large Signal Frequency Response for Various Power Supplies

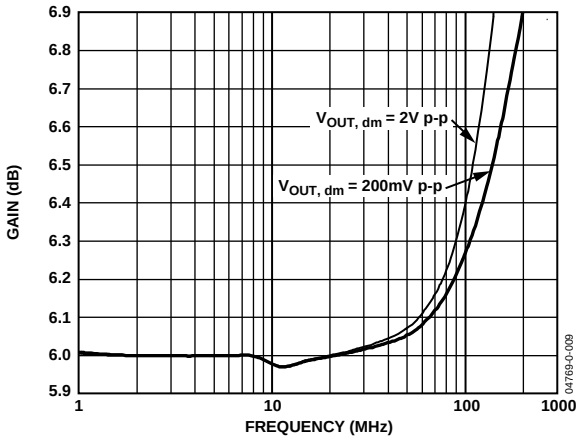

Figure 9. 0.1 dB Flatness Response

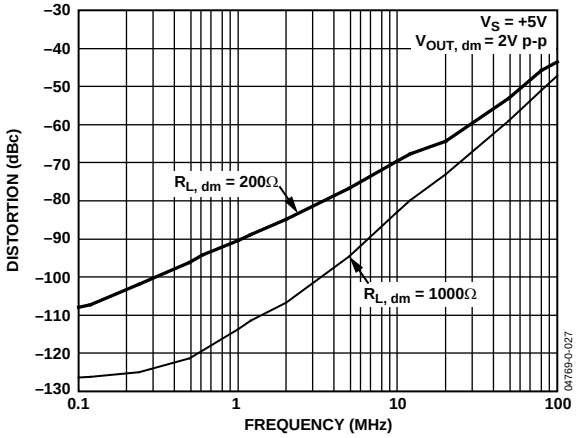

Figure 7. Second Harmonic Distortion at V_S = 5 V at Various Loads

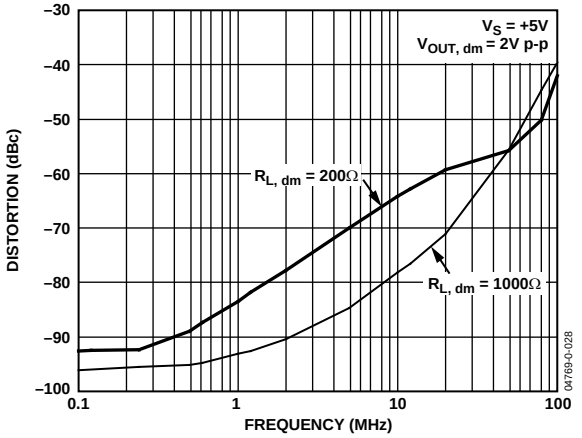

Figure 10. Third Harmonic Distortion at V_S = 5 V at Various Loads

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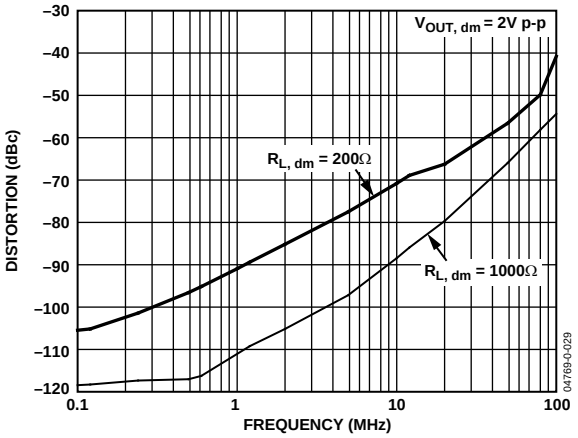

Figure 11. Second Harmonic Distortion at V_S = ±5 V at Various Loads

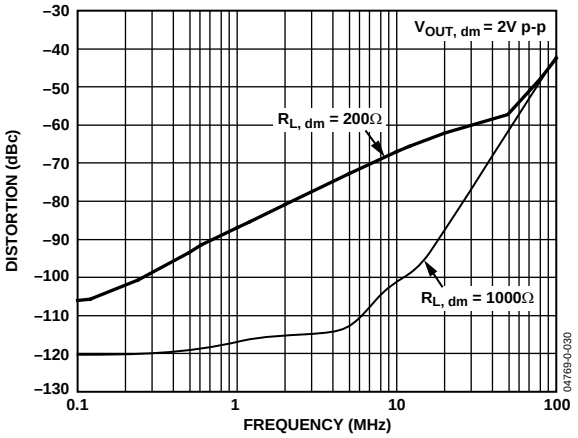

Figure 14. Third Harmonic Distortion at V_S = ±5 V at Various Loads

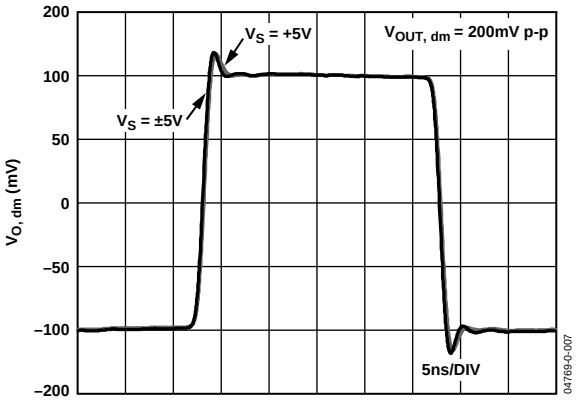

Figure 12. Small Signal Transient Response for Various Power Supply Voltages

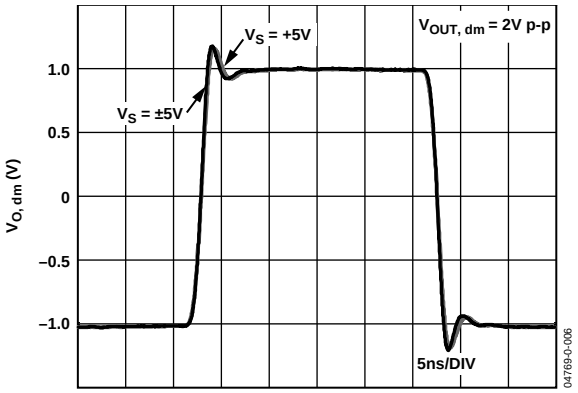

Figure 15. Large Signal Transient Response for Various Power Supply Voltages

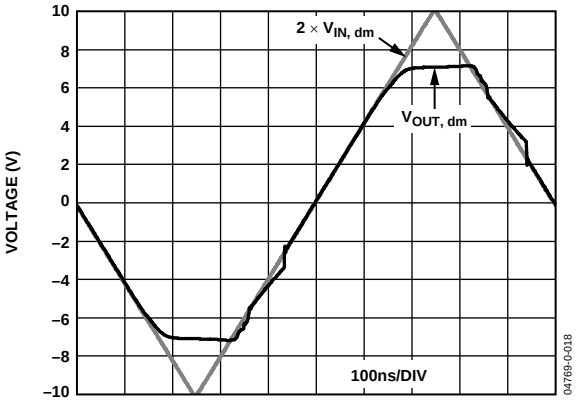

Figure 13. Overdrive Recovery

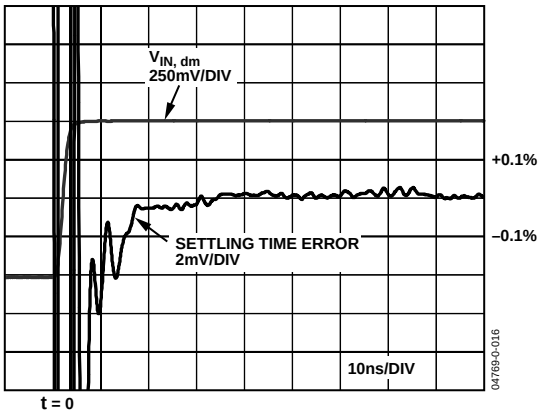

Figure 16. Settling Time (0.1%)

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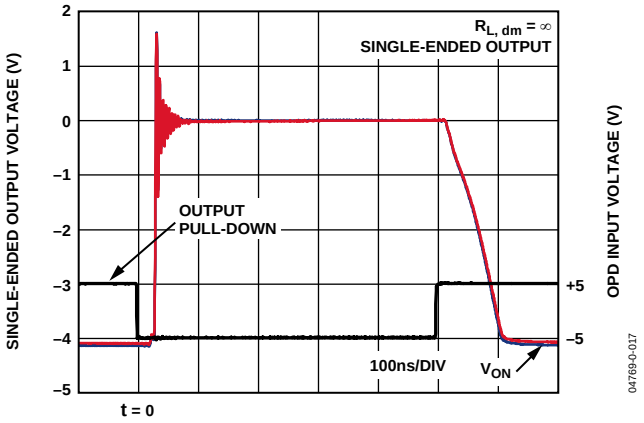

Figure 17. Output Pull-Down Response

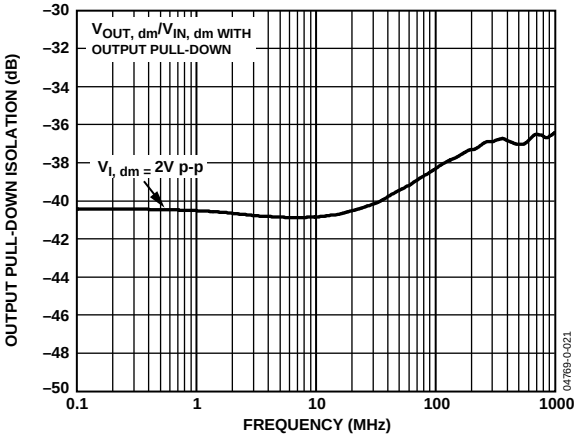

Figure 20. Output Pull-Down Isolation vs. Frequency

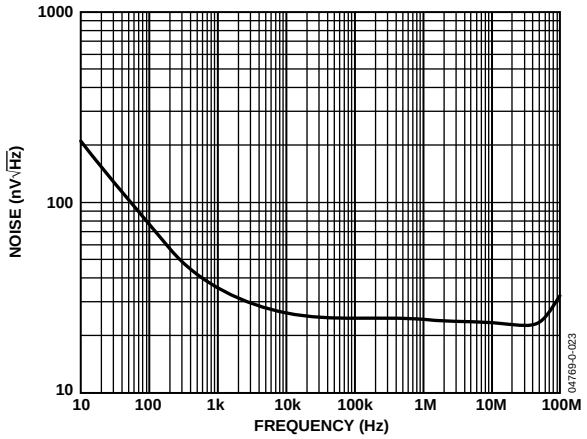

Figure 18. Output-Referred Voltage Noise vs. Frequency

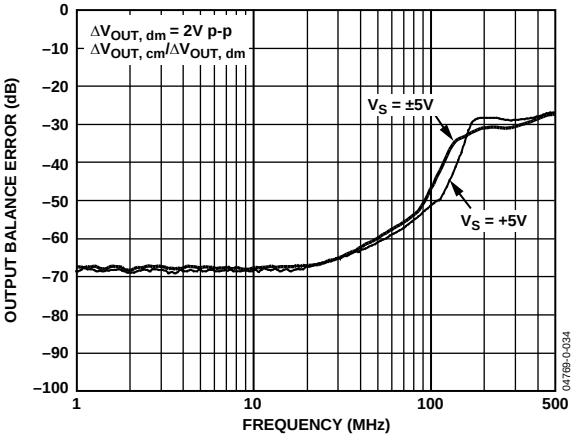

Figure 21. Output Balance vs. Frequency

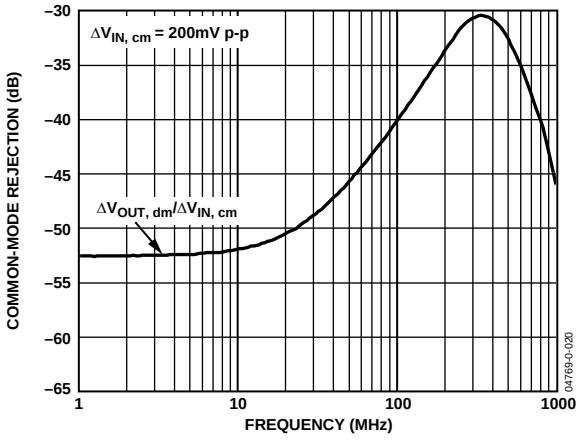

Figure 19. Common-Mode Rejection Ratio vs. Frequency

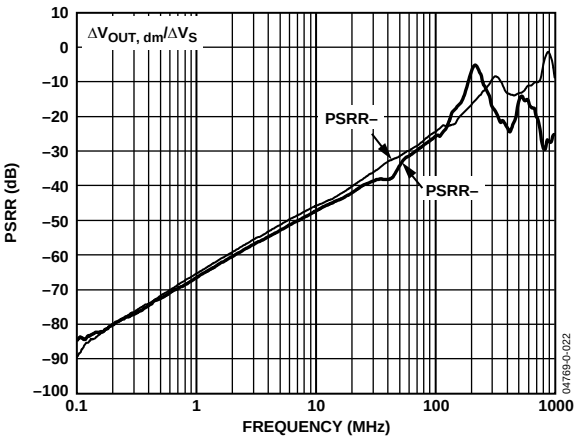

Figure 22. Power Supply Rejection Ratio vs. Frequency

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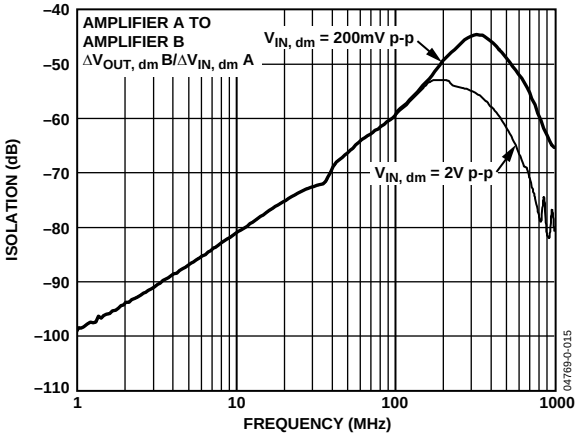

Figure 23. Amplifier-to-Amplifier Isolation vs. Frequency

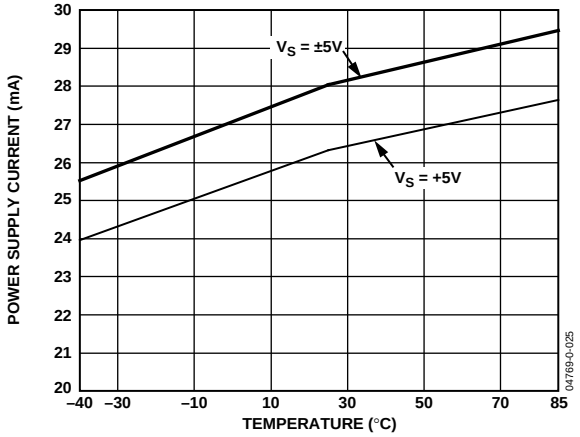

Figure 26. Power Supply Current vs. Temperature

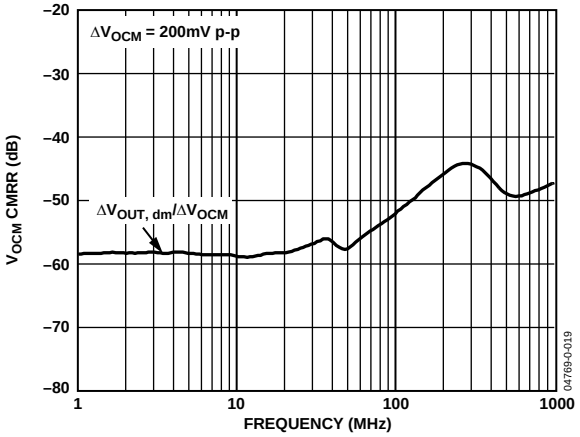

Figure 24 V_{OCM} CMRR vs. Frequency

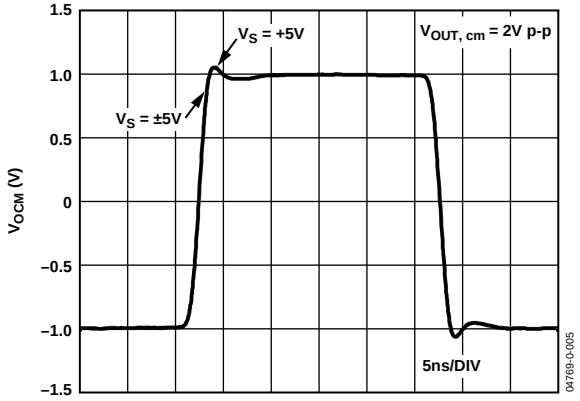

Figure 27. V_{OCM} Large Signal Transient Response for Various Power Supply Voltages

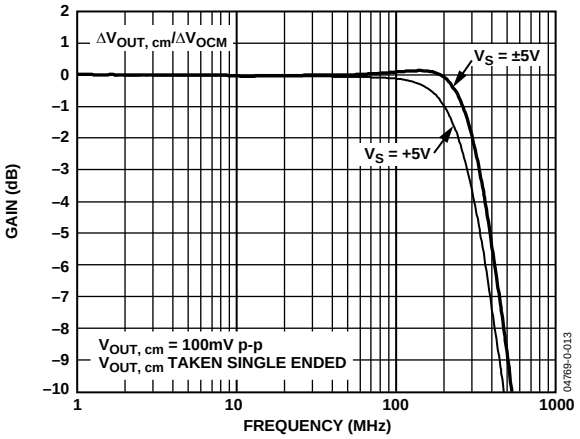

Figure 25. V_{OCM} Frequency Response for Various Power Supply Voltages

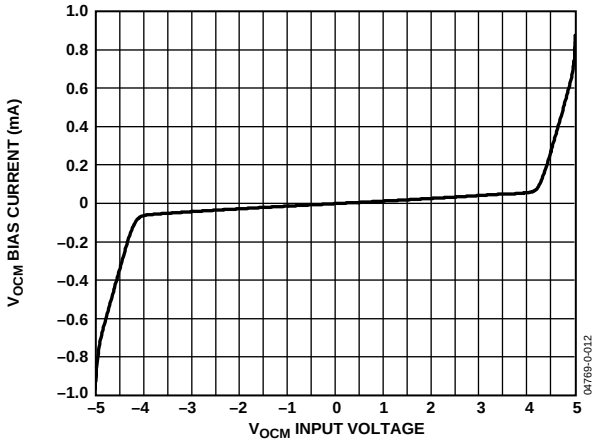

Figure 28. V_{OCM} Bias Current vs. V_{OCM} Input Voltage

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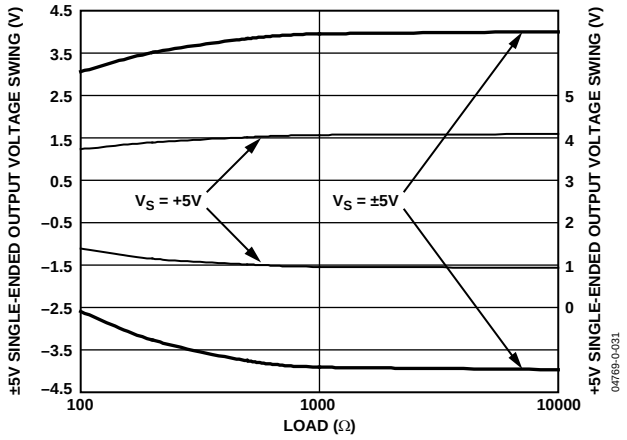

Figure 29. Output Saturation Voltage vs. Single-Ended Output Load

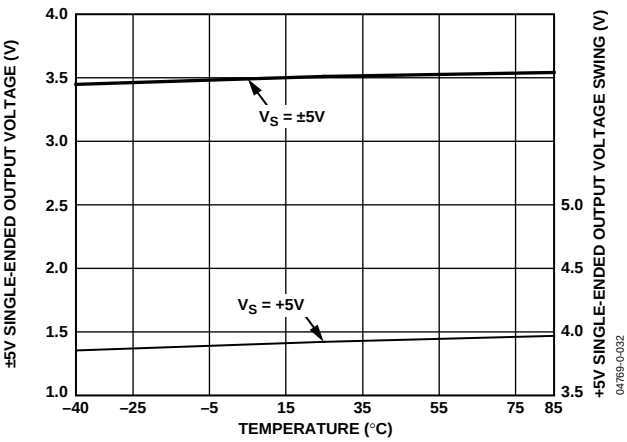

Figure 30. Positive Output Saturation Voltage vs. Temperature

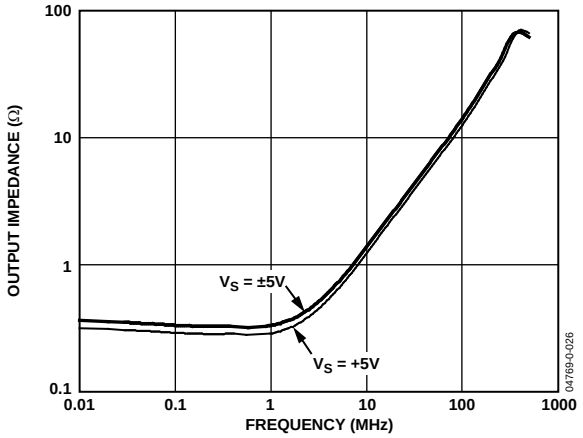

Figure 31. Single-Ended Output Impedance Magnitude vs. Frequency

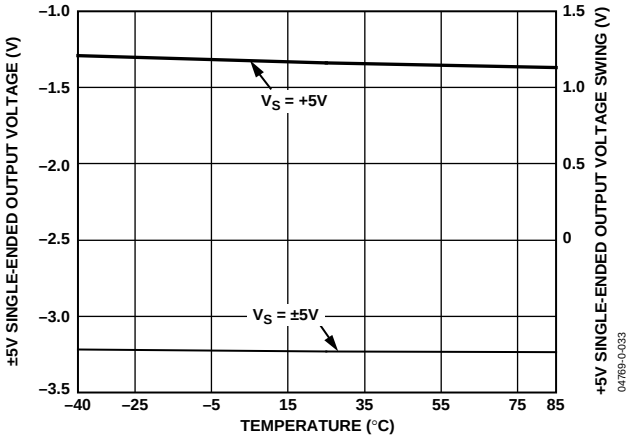

Figure 32. Negative Output Saturation Voltage vs. Temperature

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TEST CIRCUIT

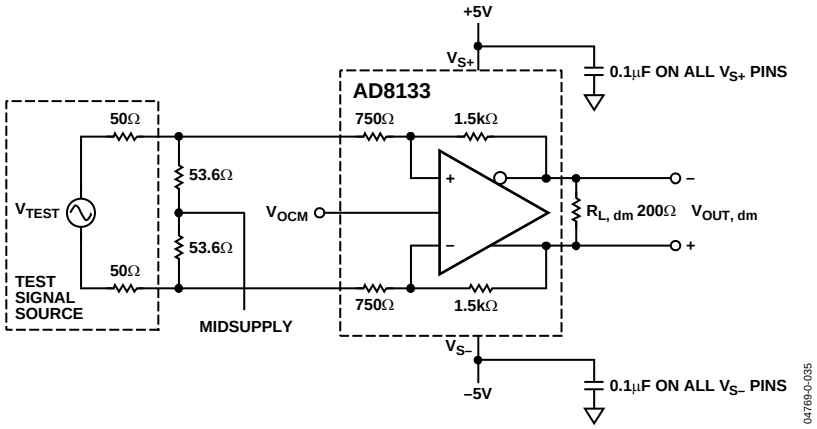

Figure 33. Basic Test Circuit

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THEORY OF OPERATION

Each differential driver in the AD8133 differs from a conventional op amp in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The AD8133 drivers make it easy to perform single-ended-to-differential conversion, common-mode level shifting, and amplification of differential signals.

Previous differential drivers, both discrete and integrated designs, have been based on using two independent amplifiers and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level shifting has also been difficult with previous differential drivers. Level shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes, the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

Each of the AD8133 drivers uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set by the internal resistors, controls only the differential output voltage. The internal common-mode feedback loop controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level by simply applying a voltage to the V_{OCM} input. The output common-mode voltage is forced, by internal common-mode feedback, to equal the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The AD8133 architecture results in outputs that are highly balanced over a wide frequency range without requiring external components or adjustments. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs of identical amplitude that are exactly 180° apart in phase.

DEFINITION OF TERMS

Differential Voltage

Differential voltage refers to the difference between two node voltages that are balanced with respect to each other. For example, in Figure 34 the output differential voltage (or equivalently output differential mode voltage) is defined as

$$V_{OUT,dm} = (V_{OP} - V_{ON})$$

Common-mode voltage refers to the average of two node voltages with respect to a common reference. The output common-mode voltage is defined as

$$V_{OUT,cm} = \frac{(V_{OP} + V_{ON})}{2}$$

Output Balance

Output balance is a measure of how well the differential output signals are matched in amplitude and how close they are to exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential output voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal. By this definition, output balance error is the magnitude of the change in output common-mode voltage divided by the magnitude of the change in output differential-mode voltage in response to a differential input signal.

$$Output\ Balance\ Error = \left|\frac{\Delta V_{OUT,cm}}{\Delta V_{OUT,dm}}\right|$$

ANALYZING AN APPLICATION CIRCUIT

The AD8133 uses high open-loop gain and negative feedback to force its differential and common-mode output voltages to minimize the differential and common-mode input error voltages. The differential input error voltage is defined as the voltage between the differential inputs labeled V_{AP} and V_{AN} in Figure 34. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

CLOSED-LOOP GAIN

The differential mode gain of the circuit in Figure 34 can be described by the following equation.

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G} = 2$$

where R_F = 1.5 kΩ and R_G = 750 Ω nominally.

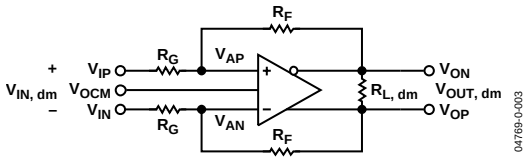

Figure 34.

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CALCULATING AN APPLICATION CIRCUIT'S INPUT IMPEDANCE

The effective input impedance of a circuit such as that in Figure 34 at V_{IP} and V_{IN} depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the differential input impedance, $R_{IN, dm}$, between the inputs V_{IP} and V_{IN} is simply

$$R_{IN,dm} = 2 \times R_G = 1.5\text{k}\Omega$$

In the case of a single-ended input signal (for example, if V_{IN} is grounded and the input signal is applied to V_{IP}), the input impedance becomes:

$$R_{IN,dm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) = 1.125\text{k}\Omega$$

The circuit's input impedance is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The inputs of the AD8133 are designed to facilitate level-shifting of ground referenced input signals on a single power supply. For a single-ended input, this would imply, for example, that the voltage at V_{IN} in Figure 34 would be 0 V when the amplifier's negative power supply voltage was also set to 0 V.

It is important to ensure that the common-mode voltage at the amplifier inputs, V_{AP} and V_{AN}, stays within its specified range. Since voltages V_{AP} and V_{AN} are driven to be essentially equal by negative feedback, the amplifier's input common-mode voltage can be expressed as a single term, V_{ACM}. V_{ACM} can be calculated as follows

$$V_{ACM} = \frac{V_{OCM} + 2V_{ICM}}{3}$$

where V_{ICM} is the common-mode voltage of the input signal, i.e., $V_{ICM} = \frac{V_{IP} + V_{IN}}{2}$.

DRIVING A CAPACITIVE LOAD

A purely capacitive load can react with the output impedance of the AD8133 to reduce phase margin, resulting in high frequency ringing in the pulse response. The best way to minimize this effect is to place a small resistor in series with each of the amplifier's outputs to buffer the load capacitance.

OUTPUT PULL-DOWN (OPD)

The AD8133 has an OPD pin that when pulled high significantly reduces the power consumed while simultaneously pulling the outputs to within less than 1 V of V_{S-} when used with series diodes (see the Applications section). The equivalent schematic of the output pull-down circuit is shown in Figure 35. (The ESD diodes shown in Figure 35 are for ESD protection and are distinct from the series diodes used with the output pull-down feature.) See Figure 17 and Figure 20 for the output pull-down transient and isolation performance plots. The threshold levels for the OPD pin are referenced to the positive power supply voltage and are presented in the Specifications tables. When the OPD pin is pulled high, the AD8133 enters the output low disable state.

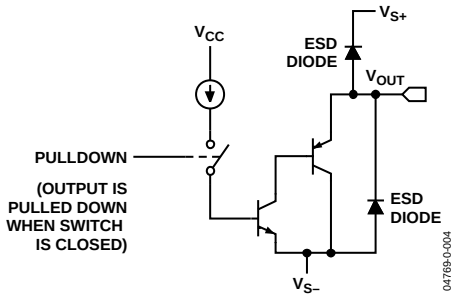

Figure 35. Output Pull-Down Equivalent Circuit

OUTPUT COMMON-MODE CONTROL

The AD8133 allows the user to control each of the three common-mode output levels independently through the three V_{OCM} input pins. The V_{OCM} pins pass a signal to the common-mode output level of each of their respective amplifiers with 330 MHz of small signal bandwidth and an internally fixed gain of one. In this way, additional control and communication signals can be embedded on the common-mode levels as the user sees fit.

With no external circuitry, the level at the V_{OCM} input of each amplifier defaults to approximately midsupply. An internal resistive divider with an impedance of approximately 100 kΩ sets this level. To limit common-mode noise in dc common-mode applications, external bypass capacitors should be connected from each of the V_{OCM} input pins to ground.

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APPLICATIONS

DRIVING RGB VIDEO SIGNALS OVER CATEGORY-5 UTP CABLE

The foremost application of the AD8133 is driving RGB video signals over UTP cable in KVM networks. Single-ended video signals are easily converted to differential signals for transmission over the cable, and the internally fixed gain of 2 automatically compensates for the losses incurred by the source and load terminations. The common topologies used in KVM networks, such as daisy-chained, star, and point-to-point, are supported by the AD8133. Figure 36 shows the AD8133 in a triple single-ended-to-differential application when driven from a 75 Ω source, which is typical of how RGB video is driven over an UTP cable. In applications that use the OPD feature, the Schottky diodes are placed in series with each of the 49.9 Ω resistors in the outputs.

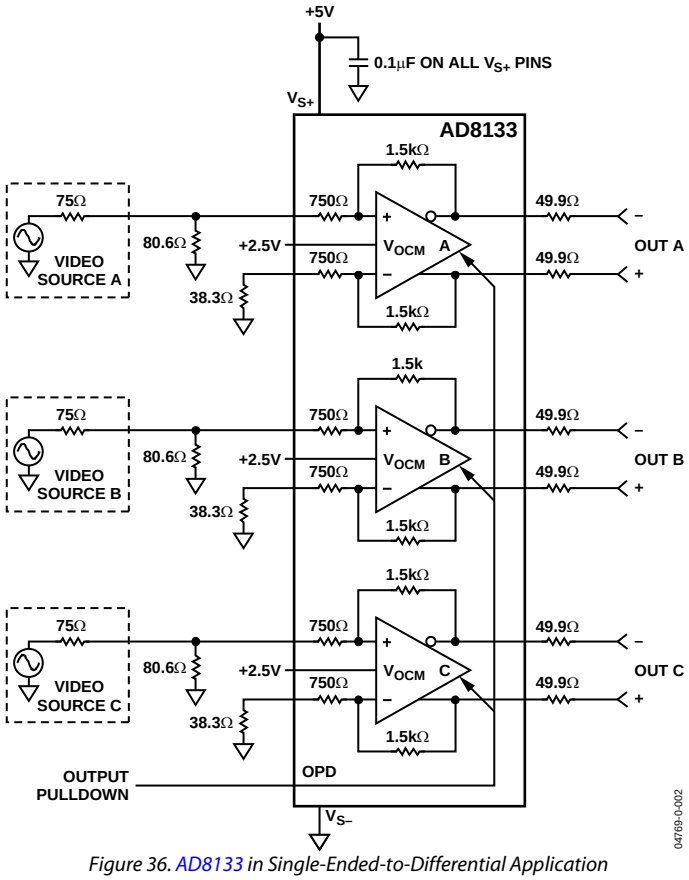

Figure 36. AD8133 in Single-Ended-to-Differential Application

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OUTPUT PULL-DOWN

The output pull-down feature, when used in conjunction with series Schottky diodes, offers a convenient means to connect a number of AD8133 outputs together to form a video network. The OPD pin is a binary input that controls the state of the AD8133 outputs. Its binary input level is referenced to the most positive power supply (see the Specifications tables for the logic levels). When the OPD input is driven to its low state, the AD8133 output is enabled and operates in its normal fashion. In this state, the V_{OCM} input can be used to provide a positive bias on the series diodes, allowing the AD8133 to transmit signals over the network. When the OPD input is driven to its high state, the outputs of the AD8133 are forced to a low voltage, irrespective of the level on the V_{OCM} input, reverse-biasing the series diodes and thus presenting high impedance to the network. This feature allows a three-state output to be realized that maintains its high impedance state even when the AD8133 is not powered. This condition can occur in KVM networks where the AD8133s do not all reside in the same module, and some modules in the network are not powered.

It is recommended that the output pull-down feature only be used in conjunction with series diodes in such a way as to ensure that the diodes are reverse-biased when the output pull-down feature is asserted, since some loading conditions can prevent the output voltage from being pulled all the way down.

KVM NETWORKS

In daisy-chained KVM networks, the drivers are distributed along one cable and a triple receiver is located at one end. Schottky diodes in series with the driver outputs are biased such that the one driver that is transmitting video signals has its diodes forward-biased and the disabled drivers have their diodes reverse-biased. The output common-mode voltage, set by the V_{OCM} input, supplies the forward-biased voltage. When the output pull-down feature is asserted, the differential outputs are pulled to a low voltage, reverse-biasing the diodes.

In star networks, all cables radiate out from a central hub, which contains a triple receiver. The series diodes are all located at the receiver in the star network. Only one ray of the star is transmitting at a given time, and all others are isolated by the reverse-biased diodes. Diode biasing is controlled in the same way as in the daisy-chained network.

In the daisy-chained and star networks that use diodes for isolation, return paths are required for the common-mode currents that flow through the series diodes. A common-mode tap can be implemented at each receiver by splitting the100 Ω termination resistor into two 50 Ω resistors in series. The diode currents are routed from the tap between the 50 Ω resistors back to the respective transmitters over one of the wires of the fourth twisted pair in the UTP cable. Series resistors in the common-mode return path are generally required to set the desired diode current.

In point-to-point networks, there is one transmitter and one receiver per cable, and the switching is generally implemented with a crosspoint switch. In this case, there is no need to use diodes or the output pull-down feature.

Diode and crosspoint switching are by no means the only type of switching that can be used with the AD8133. Many other types of mechanical, electromechanical, and electronic switches can be used.

LAYOUT AND POWER SUPPLY DECOUPLING CONSIDERATIONS

Standard high speed PCB layout practices should be adhered to when designing with the AD8133. A solid ground plane is recommended and good wideband power supply decoupling networks should be placed as close as possible to the supply pins. Small surface-mount ceramic capacitors are recommended for these networks, and tantalum capacitors are recommended for bulk supply decoupling.

AMPLIFIER-TO-AMPLIFIER ISOLATION

The least amount of isolation between the three amplifiers exists between Amplifier A and Amplifier B. This is therefore viewed as the worst-case isolation and is what is reflected in the Specifications tables and Typical Performance Characteristics. Refer to the Basic Test Circuit shown in Figure 33 for the test conditions.

EXPOSED PADDLE (EP)

The LFCSP-24 package has an exposed paddle on the underside of its body. In order to achieve the specified thermal resistance, it must have a good thermal connection to one of the PCB planes. The exposed paddle must be soldered to a pad on the top of the board that is connected to an inner plane with several thermal vias.

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OUTLINE DIMENSIONS

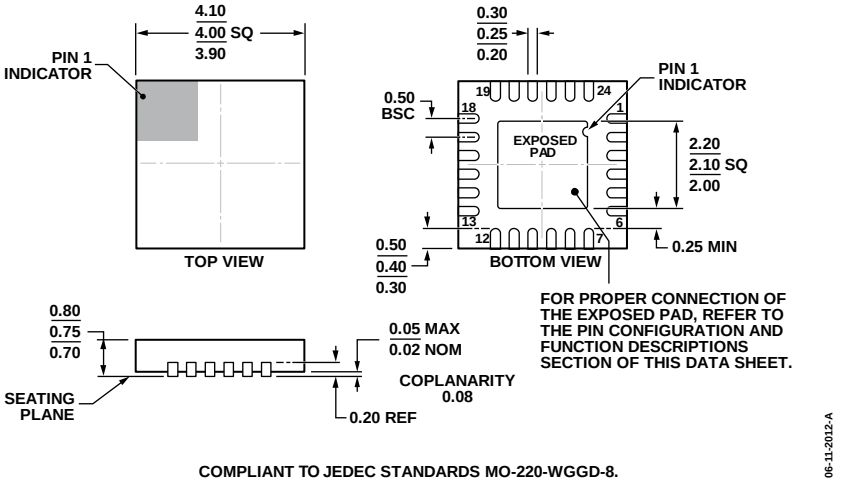

Figure 37. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Package	Package Description	Package Outline
AD8133ACPZ-R2	−40°C to +85°C	24-Lead LFCSP	CP-24-10
AD8133ACPZ-REEL	−40°C to +85°C	24-Lead LFCSP	CP-24-10
AD8133ACPZ-REEL7	−40°C to +85°C	24-Lead LFCSP	CP-24-10

[1] Z = RoHS Compliant Part.

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