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REVISION HISTORY

3/14—Rev. A to Rev. B

Updated Format ... Universal
Deleted Operating Temperature Range Parameter, Table 1 ... 3
Changes to Table 3 ... 5
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Changes to Ordering Guide ... 13

8/99—Rev. 0 to Rev. A

SPECIFICATIONS

±5 V SUPPLIES

At T_A = +25°C, V_S = ±5 V, R_L = 1 kΩ, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE	R_F = 3.01 kΩ for N-8 Package or R_F = 2.49 kΩ for R-8 Package or R_F = 2.10 kΩ for RJ-5 Package				
−3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	225	270		MHz
	G = +2, V_O = 0.2 V p-p	140	170		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p	10	30		MHz
Large Signal Bandwidth	G = +10, V_O = 4 V p-p, R_F = 499 Ω		40		MHz
Slew Rate (Rising Edge)	G = +2, V_O = 4 V Step		280		V/µs
	G = −1, V_O = 4 V Step, R_F = 1.5 kΩ		1500		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		28		ns
DISTORTION/NOISE PERFORMANCE	R_F = 3.01 kΩ for N-8 Package or R_F = 2.49 kΩ for R-8 Package or R_F = 2.10 kΩ for RJ-5 Package				
Total Harmonic Distortion	f_C = 1 MHz, V_O = 2 V p-p, G = +2		−63		dBc
	f_C = 10 MHz, V_O = 2 V p-p, G = +2		−50		dBc
Differential Gain	NTSC, G = +2		0.11		%
Differential Phase	NTSC, G = +2		0.4		Degrees
Input Voltage Noise	f = 10 MHz		4.0		nV/√Hz
Input Current Noise	f = 10 MHz, $+I_{IN}$		1.1		pA/√Hz
	$-I_{IN}$		9.1		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			5	30	±mV
	T_{MIN} to T_{MAX}			50	±mV
Offset Drift			40		µV/°C
+Input Bias Current			0.5	1	±µA
	T_{MIN} to T_{MAX}			2	±µA
−Input Bias Current			5	10	±µA
	T_{MIN} to T_{MAX}			12	±µA
Input Bias Current Drift (±)			6		nA/°C
Open-Loop Transimpedance		400	1000		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		90		MΩ
	−Input		260		Ω
Input Capacitance	+Input		1.6		pF
Input Common-Mode Voltage Range			3.8		±V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	46	54		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Positive	+3.7	+3.90		V
	Negative		−3.90	−3.7	V
Output Current	R_L = 50 Ω		10		mA
Short Circuit Current			60		mA
POWER SUPPLY					
Quiescent Current			400	475	µA
	T_{MIN} to T_{MAX}			560	µA
Power Supply Rejection Ratio	V_S = ±4 V to ±6 V	56	66		dB

+5 V SUPPLY

At T_A = +25°C, V_S = +5 V, R_L = 1 kΩ to 2.5 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE	R_F = 3.01 kΩ for N-8 Package or R_F = 2.49 kΩ for R-8 Package or R_F = 2.10 kΩ for RJ-5 Package				
−3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	190	225		MHz
	G = +2, V_O = 0.2 V p-p	110	130		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p	10	30		MHz
Large Signal Bandwidth	G = +10, V_O = 4 V p-p, R_F = 499 Ω		45		MHz
Slew Rate (Rising Edge)	G = +2, V_O = 4 V Step		260		V/µs
	G = −1, V_O = 4 V Step, R_F = 1.5 kΩ		775		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		30		ns
DISTORTION/NOISE PERFORMANCE	R_F = 3.01 kΩ for N-8 Package or R_F = 2.49 kΩ for R-8 Package or R_F = 2.10 kΩ for RJ-5 Package				
Total Harmonic Distortion	f_C = 1 MHz, V_O = 2 V p-p, G = +2		−60		dBc
	f_C = 10 MHz, V_O = 2 V p-p, G = +2		−50		dBc
Differential Gain	NTSC, G = +2		0.14		%
Differential Phase	NTSC, G = +2		0.70		Degrees
Input Voltage Noise	f = 10 MHz		4.0		nV/√Hz
Input Current Noise	f = 10 MHz, $+I_{IN}$		1.1		pA/√Hz
	$-I_{IN}$		9.1		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			5	35	±mV
	T_{MIN} to T_{MAX}			50	±mV
Offset Drift			40		µV/°C
+Input Bias Current			0.5	1	±µA
	T_{MIN} to T_{MAX}			2	±µA
−Input Bias Current			5	10	±µA
	T_{MIN} to T_{MAX}			11	±µA
Input Bias Current Drift (±)			8		nA/°C
Open-Loop Transimpedance		50	500		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		120		MΩ
	−Input		300		Ω
Input Capacitance	+Input		1.6		pF
Input Common-Mode Voltage Range			1.5 to 3.5		V
Common-Mode Rejection Ratio	V_{CM} = 1.5 V to 3.5 V	48	54		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		1.1 to 3.9	0.95 to 4.05		V
Output Current	R_L = 50 Ω		10		mA
Short Circuit Current			30		mA
POWER SUPPLY					
Quiescent Current			350	425	µA
	T_{MIN} to T_{MAX}			470	µA
Power Supply Rejection Ratio	V_S = +4 V to +6 V	56	66		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Internal Power Dissipation[1]	
PDIP Package (N-8)	1.3 Watts
SOIC_N (R-8)	0.75 Watts
SOT-23 Package (RJ-5)	0.5 Watts
Input Voltage (Common Mode)	$\pm V_S \pm 1$ V
Differential Input Voltage	±3.5 V
Output Short Circuit Duration	Observe Power Derating Curves
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	+300°C

[1] See Table 4.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for device in free air.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead PDIP Package	90	°C/W
8-Lead SOIC_N Package	155	°C/W
5-Lead SOT-23 Package	240	°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8005 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily causes a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8005 is internally short circuit protected, this is not sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 5.

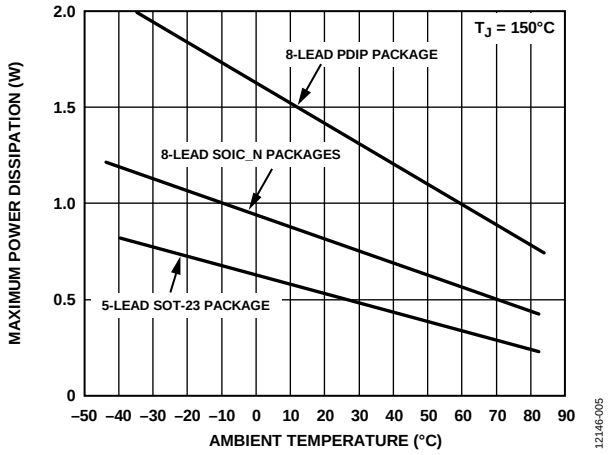


Figure 5. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

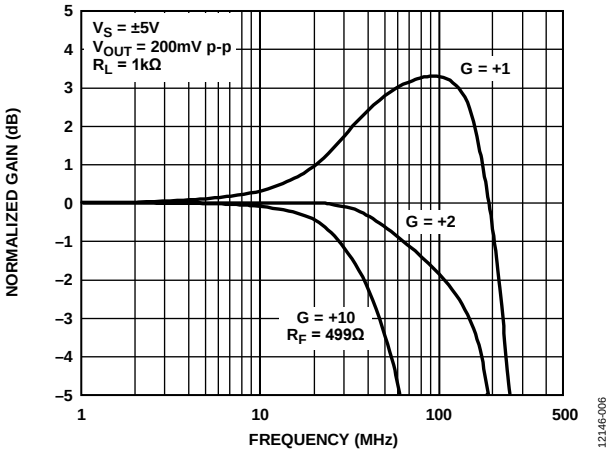


Figure 6. Frequency Response; G = +1, +2, +10; V_S = ±5 V

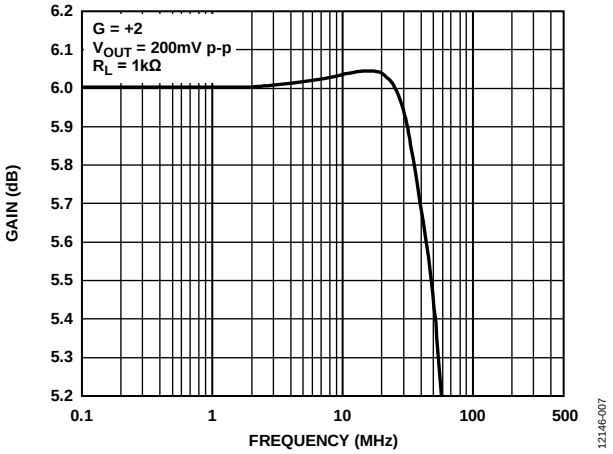


Figure 7. Gain Flatness; G = +2; V_S = ±5 V or +5 V

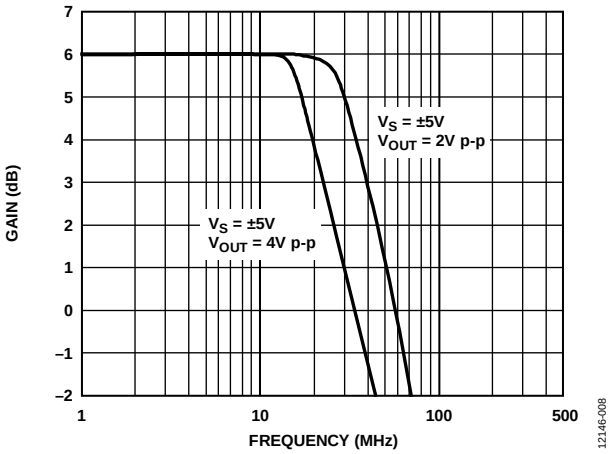


Figure 8. Large Signal Frequency Response; G = +2, R_L = 1 kΩ

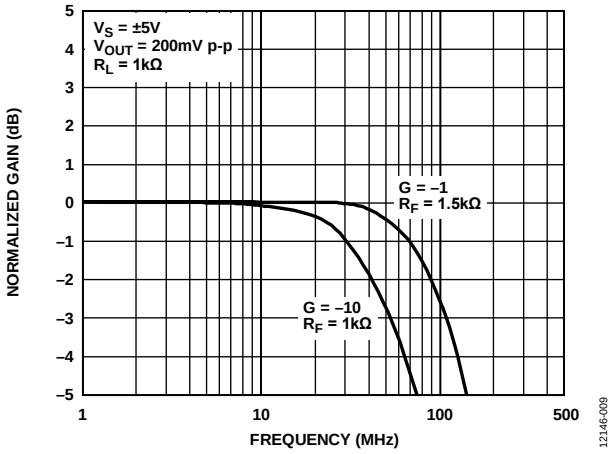


Figure 9. Frequency Response; G = –1, –10; V_S = ±5 V

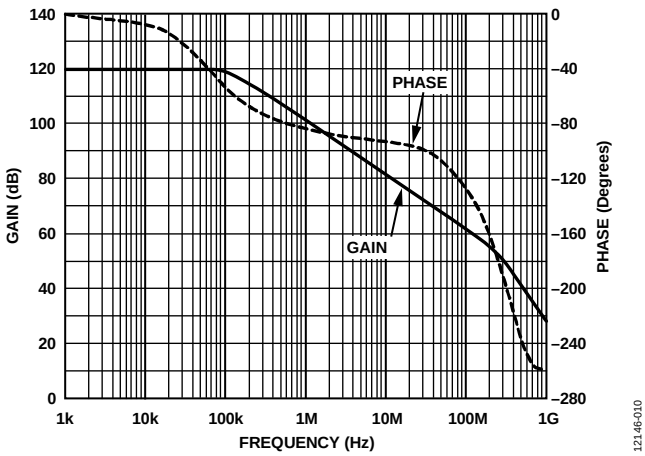


Figure 10. Transimpedance Gain and Phase vs. Frequency

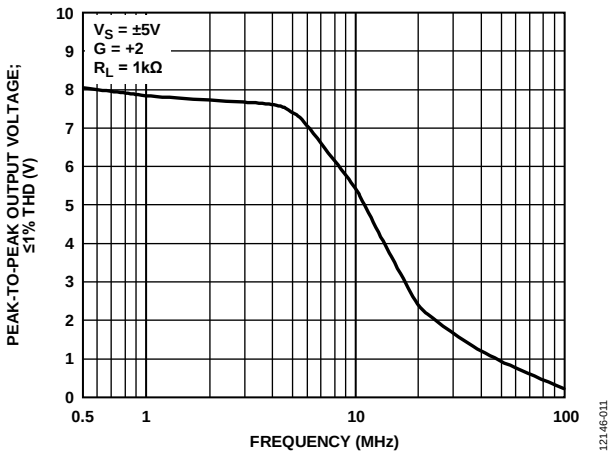


Figure 11. Output Swing vs. Frequency; V_S = ±5 V

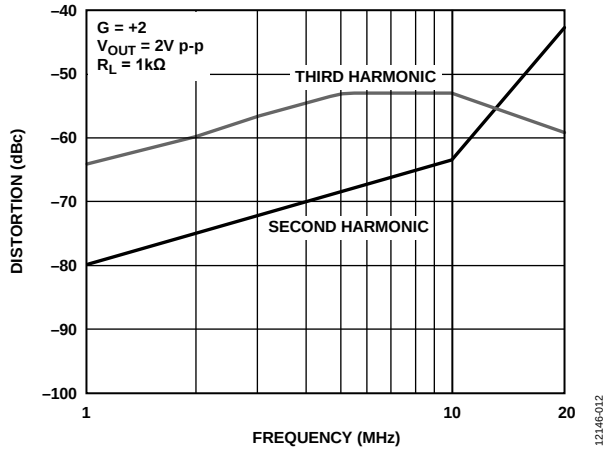


Figure 12. Distortion vs. Frequency; V_S = ±5 V

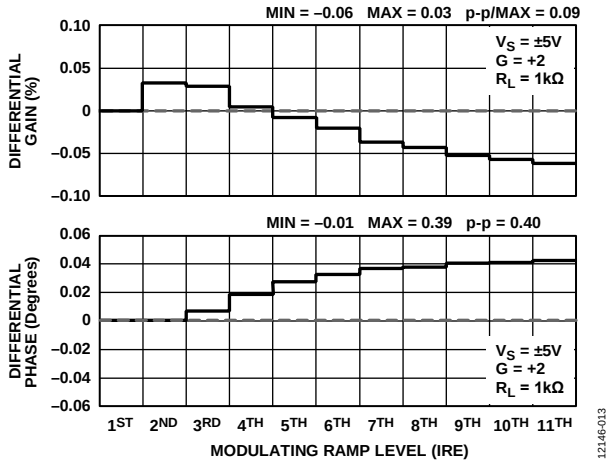


Figure 13. Differential Gain and Phase, V_S = ±5 V

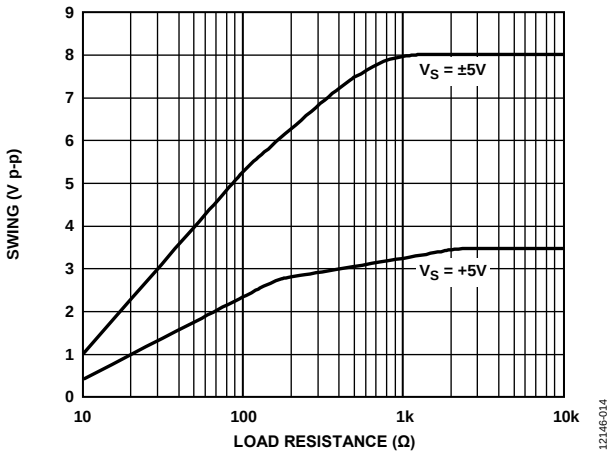


Figure 14. Output Voltage Swing vs. Load

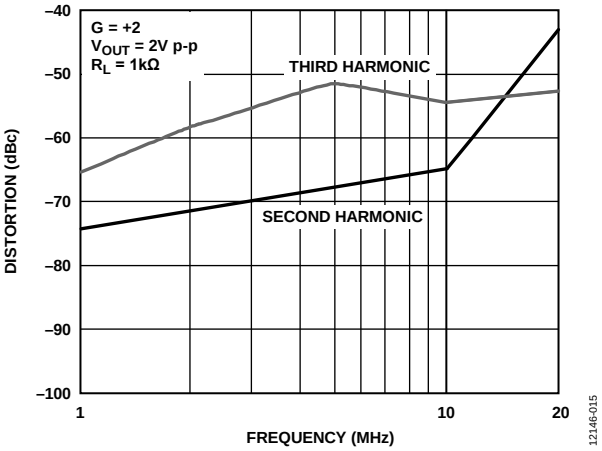


Figure 15. Distortion vs. Frequency V_S = +5 V

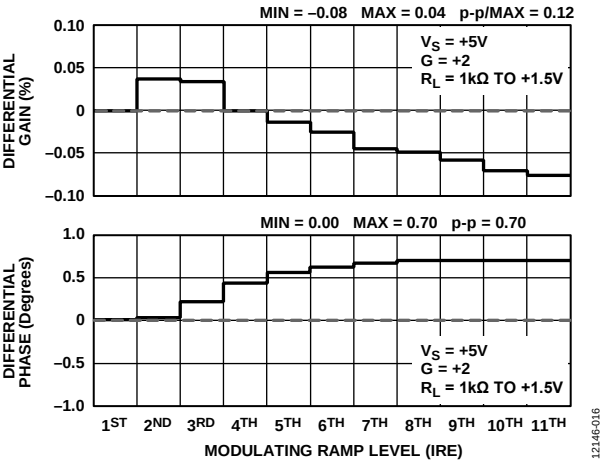


Figure 16. Differential Gain and Phase, V_S = +5 V

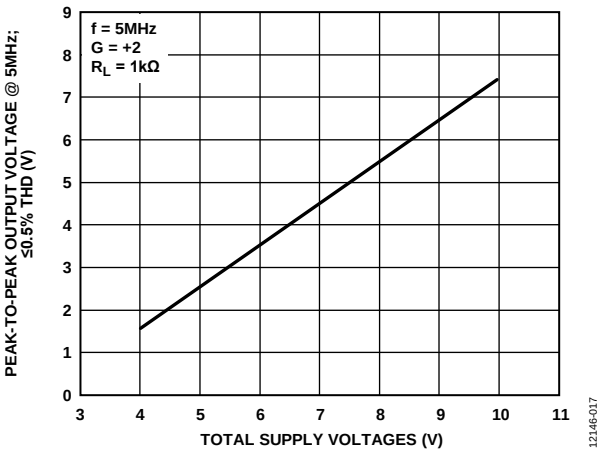


Figure 17. Output Swing vs. Supply

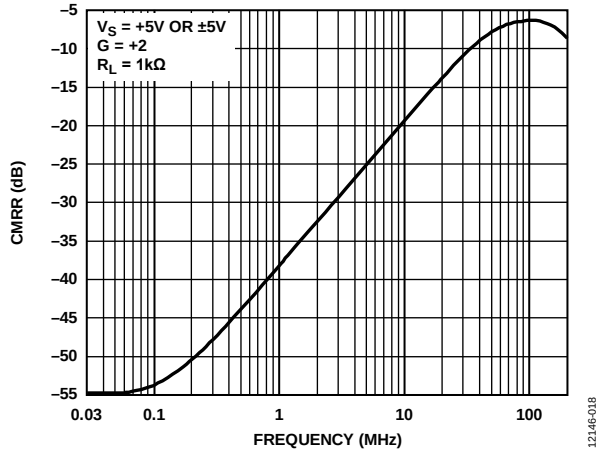


Figure 18. CMRR vs. Frequency; V_S = +5 V or ±5 V

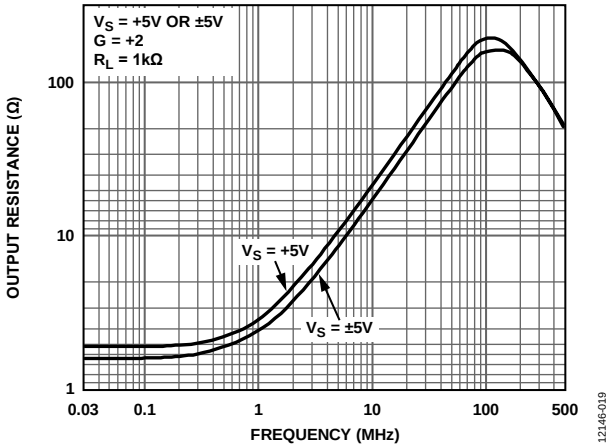


Figure 19. Output Resistance vs. Frequency; V_S = ±5 V and +5 V

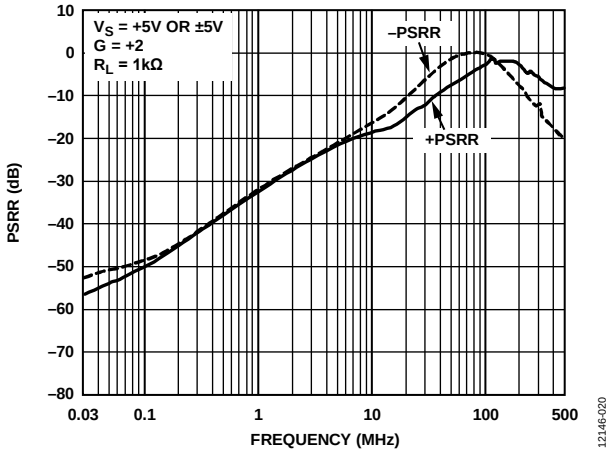


Figure 20. PSRR vs. Frequency; V_S = +5 V or ±5 V

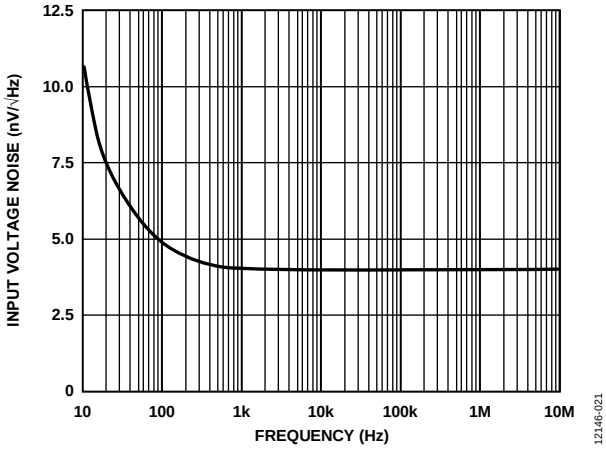


Figure 21. Noise vs. Frequency; V_S = +5 V or ±5 V

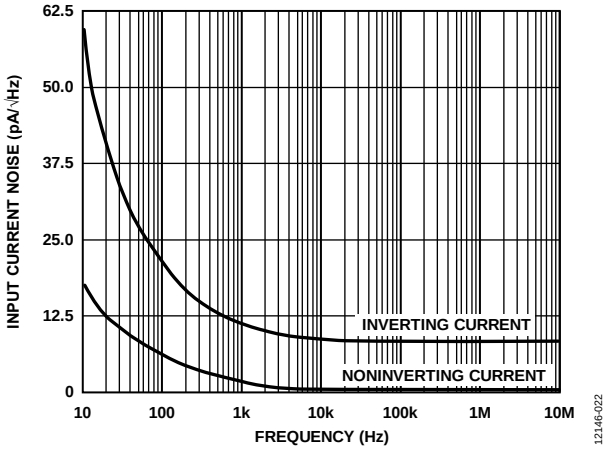


Figure 22. Noise vs. Frequency; V_S = +5 V or ±5 V

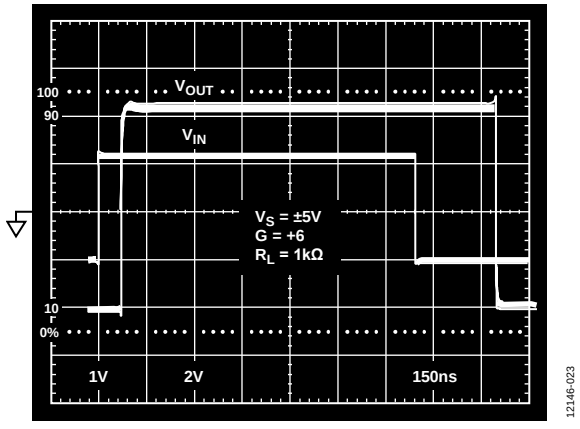


Figure 23. ±Overdrive Recovery, V_S = ±5 V, V_{IN} = 2 V Step

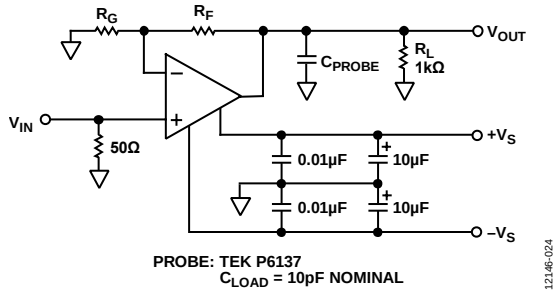


Figure 24. Test Circuit; G = +2; $R_F = R_G = 3.01$ kΩ for N-8 Package; $R_F = R_G = 2.49$ kΩ for R-8 and RJ-5 Packages

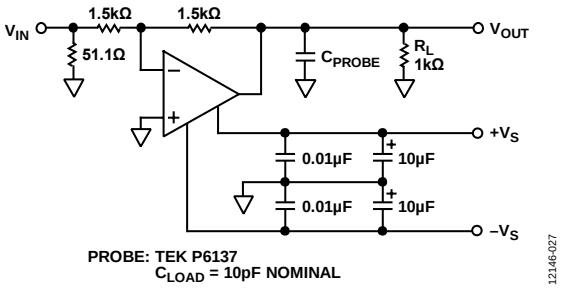


Figure 27. Test Circuit; G = −1, $R_F = R_G = 1.5$ kΩ for N-8, R-8, and RJ-5 Packages

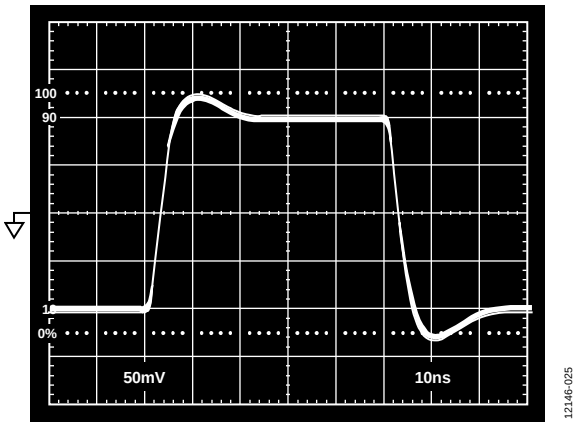


Figure 25. 200 mV Step Response; G = +2, $V_S = \pm 2.5$ V or ±5 V

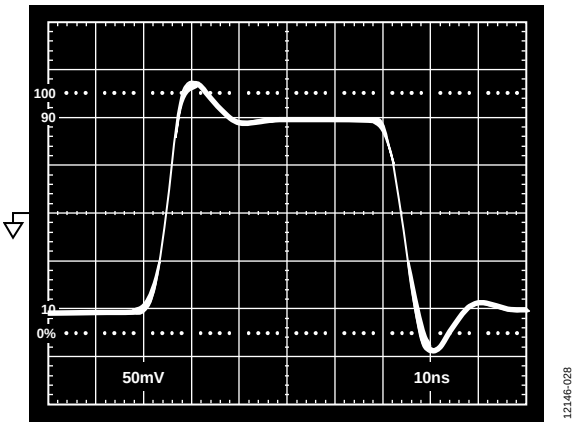


Figure 28. 200 mV Step Response; G = −1, $V_S = \pm 2.5$ V or ±5 V

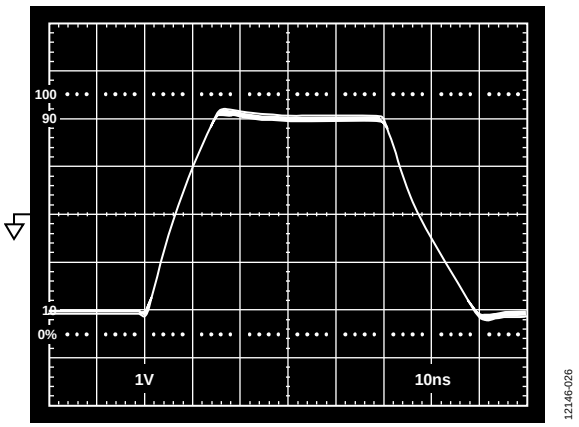


Figure 26. Step Response; G = +2, $V_S = \pm 5$ V

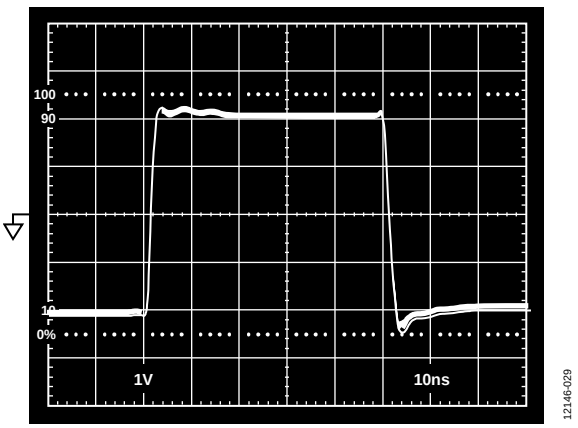


Figure 29. Step Response; G = −1, $V_S = \pm 5$ V

APPLICATIONS

DRIVING CAPACITIVE LOADS

Capacitive loads interact with the output impedance of an op amp to create an extra delay in the feedback path. This reduces circuit stability and can cause unwanted ringing and oscillation. A given value of capacitance causes much less ringing when the amplifier is used with a higher noise gain.

The capacitive load drive of the AD8005 can be increased by adding a low valued resistor in series with the capacitive load. Introducing a series resistor tends to isolate the capacitive load from the feedback loop, thereby diminishing its influence. Figure 31 shows the effects of a series resistor on capacitive drive for varying voltage gains. As the closed-loop gain is increased, the larger phase margin allows for larger capacitive loads with less overshoot. Adding a series resistor at lower closed-loop gains accomplishes the same effect. For large capacitive loads, the frequency response of the amplifier is dominated by the roll-off of the series resistor and capacitive load.

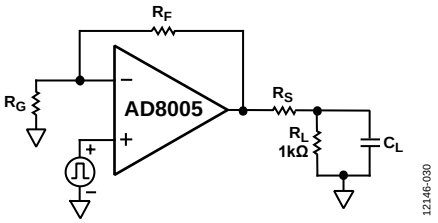


Figure 30. Driving Capacitive Loads

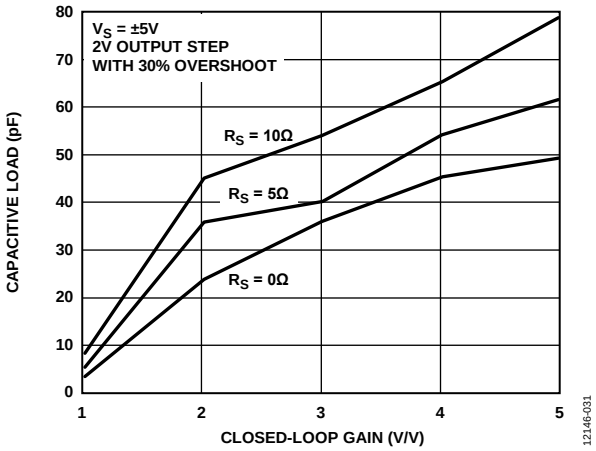


Figure 31. Capacitive Load Drive vs. Closed-Loop Gain

SINGLE-SUPPLY LEVEL SHIFTER

In addition to providing buffering, many systems require that an op amp provide level shifting. A common example is the level shifting required to move a bipolar signal into the unipolar range of many modern analog-to-digital converters (ADCs). In general, single supply ADCs have input ranges that are referenced neither to ground nor supply. Instead the reference level is some point in between, usually halfway between ground and supply (+2.5 V for a single supply 5 V ADC). Because high-speed ADCs typically have input voltage ranges of 1 V to 2 V, the op amp driving it must be single supply but not necessarily rail-to-rail.

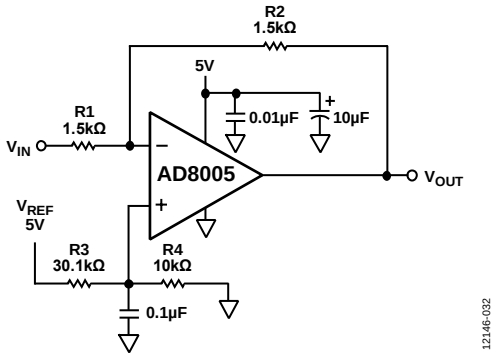


Figure 32. Bipolar to Unipolar Shift Lever

Figure 32 shows a level shifter circuit that can move a bipolar signal into a unipolar range. A positive reference voltage, derived from the +5 V supply, sets a bias level of +1.25 V at the noninverting terminal of the op amp. In ac applications, the accuracy of this voltage level is not important; however, noise is a serious consideration. A 0.1 mF capacitor provides useful decoupling of this noise.

The bias level on the noninverting terminal sets the input common-mode voltage to +1.25 V. Because the output is always positive, the op amp can be powered with a single +5 V power supply.

The overall gain function is given by the equation:

$$V_{OUT} = -\left(\frac{R2}{R1}\right)V_{IN} + \left(\frac{R4}{R3+R4}\right)\left(1+\frac{R2}{R1}\right)V_{REF}$$

In the above example, the equation simplifies to

$$V_{OUT} = -V_{IN} + 2.5\ V$$

SINGLE-ENDED-TO-DIFFERENTIAL CONVERSION

Many single supply ADCs have differential inputs. In such cases, the ideal common-mode operating point is usually halfway between supply and ground. Figure 33 shows how to convert a single-ended bipolar signal into a differential signal with a common-mode level of 2.5 V.

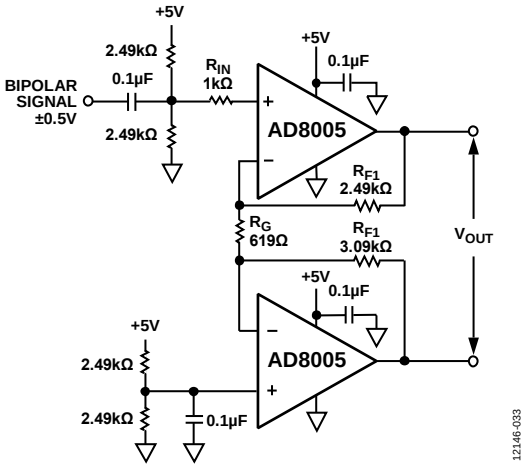


Figure 33. Single-Ended-to-Differential Converter

Amp 1 has its +input driven with the ac-coupled input signal while the +input of Amp 2 is connected to a bias level of +2.5 V. Thus the −input of Amp 2 is driven to virtual +2.5 V by its output. Therefore, Amp 1 is configured for a noninverting gain of five, $(1 + R_{F1}/R_G)$, because R_G is connected to the virtual +2.5 V of the −input of Amp 2.

When the +input of Amp 1 is driven with a signal, the same signal appears at the −input of Amp 1. This signal serves as an input to Amp 2 configured for a gain of −5, $(-R_{F2}/R_G)$. Thus the two outputs move in opposite directions with the same gain and create a balanced differential signal.

This circuit can be simplified to create a bipolar in/bipolar out single-ended to differential converter. Obviously, a single supply is no longer adequate and the $-V_S$ pins must now be powered with −5 V. The +input to Amp 2 is tied to ground. The ac coupling on the +input of Amp 1 is removed and the signal can be fed directly into Amp 1.

LAYOUT CONSIDERATIONS

In order to achieve the specified high-speed performance of the AD8005, the user must be attentive to board layout and component selection. Proper R_F design techniques and selection of components with low parasitics are necessary.

The printed circuit board (PCB) must have a ground plane that covers all unused portions of the component side of the board. This provides a low impedance path for signals flowing to ground. Remove the ground plane from the area under and around the chip (leave about 2 mm between the pin contacts and the ground plane). This helps to reduce stray capacitance. If both signal tracks and the ground plane are on the same side of the PCB, also leave a 2 mm gap between ground plane and track.

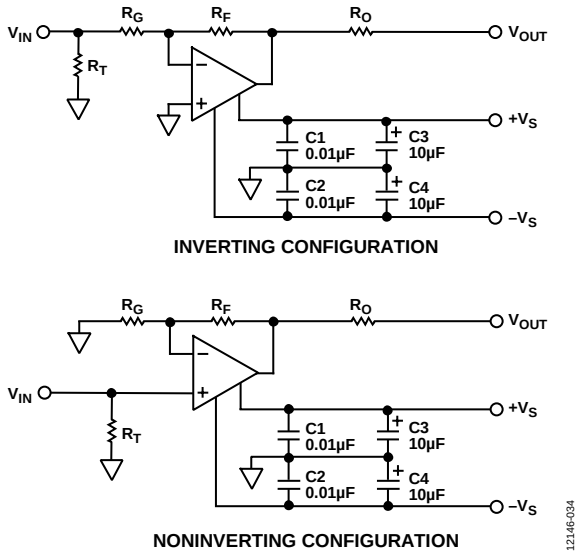


Figure 34. Inverting and Nonconverting Configurations

Chip capacitors have low parasitic resistance and inductance and are suitable for supply bypassing (see Figure 34). Make sure that one end of the capacitor is within 1/8 inch of each power pin with the other end connected to the ground plane. An additional large (0.47 µF − 10 µF) tantalum electrolytic capacitor must also be connected in parallel. This capacitor supplies current for fast, large signal changes at the output. It must not necessarily be as close to the power pin as the smaller capacitor.

Locate the feedback resistor close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1.5 pF at the inverting input significantly affect high-speed performance.

Use stripline design techniques for long signal traces (that is, greater than about 1 inch). Striplines must have a characteristic impedance of either 50 Ω or 75 Ω. For the stripline to be effective, correct termination at both ends of the line is necessary.

Table 5. Typical Bandwidth vs. Gain Setting Resistors

Gain	R_F	R_G	R_T	Small Signal −3 dB BW (MHz), V_S = ±5 V
−1	1.49 kΩ	1.49 kΩ	52.3	120 MHz
−10	1 kΩ	100 Ω	100 Ω	60 MHz
+1	2.49 kΩ	∞	49.9 Ω	270 MHz
+2	2.49 kΩ	2.49 kΩ	49.9 Ω	170 MHz
+10	499 Ω	56.2 Ω	49.9 Ω	40 MHz

INCREASING FEEDBACK RESISTORS

Unlike conventional voltage feedback op amps, the choice of feedback resistor has a direct impact on the closed-loop bandwidth and stability of a current feedback op amp circuit. Reducing the resistance below the recommended value makes the amplifier more unstable. Increasing the size of the feedback resistor reduces the closed-loop bandwidth.

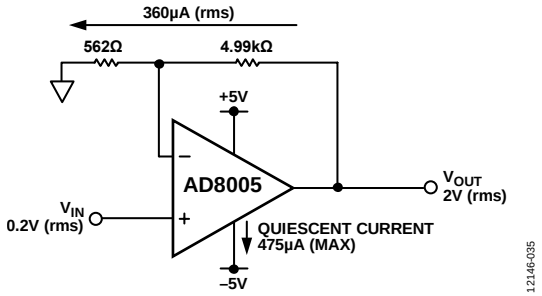
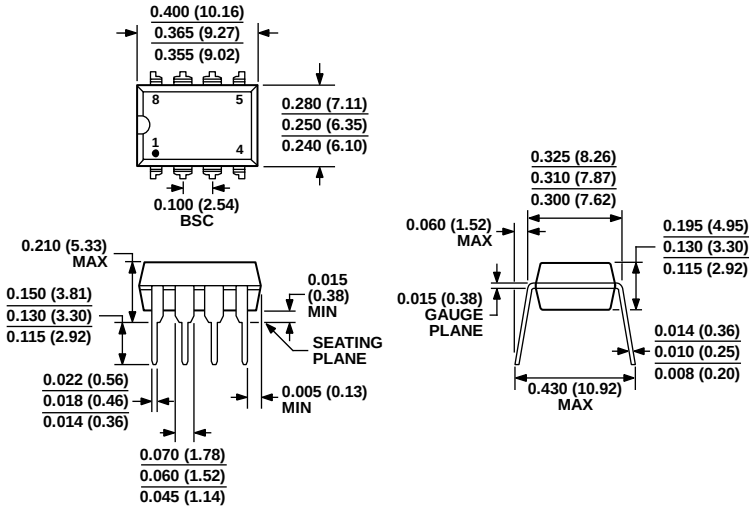


Figure 35. Saving Power by Increasing Feedback Resistor Network

In power-critical applications where some bandwidth can be sacrificed, increasing the size of the feedback resistor yields significant power savings. A good example of this is the gain of +10 case. Operating from a bipolar supply (±5 V), the quiescent current is 475 µA (excluding the feedback network). The recommended feedback and gain resistors are 499 Ω and 56.2 Ω respectively. In order to drive an rms output voltage of 2 V, the output must deliver a current of 3.6 mA to the feedback network. Increasing the size of the resistor network by a factor of 10, as shown in Figure 35, reduces this current to 360 µA; however, the closed loop bandwidth decreases to 20 MHz.

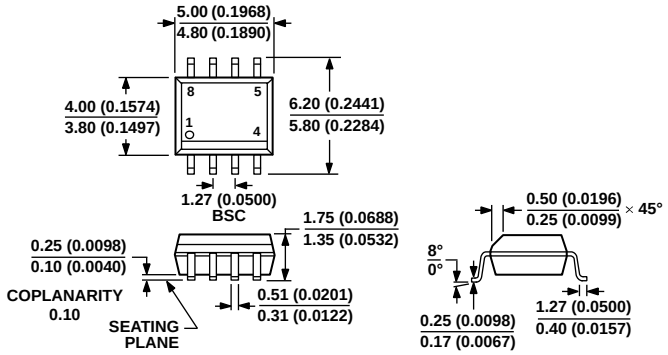
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 36. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 37. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

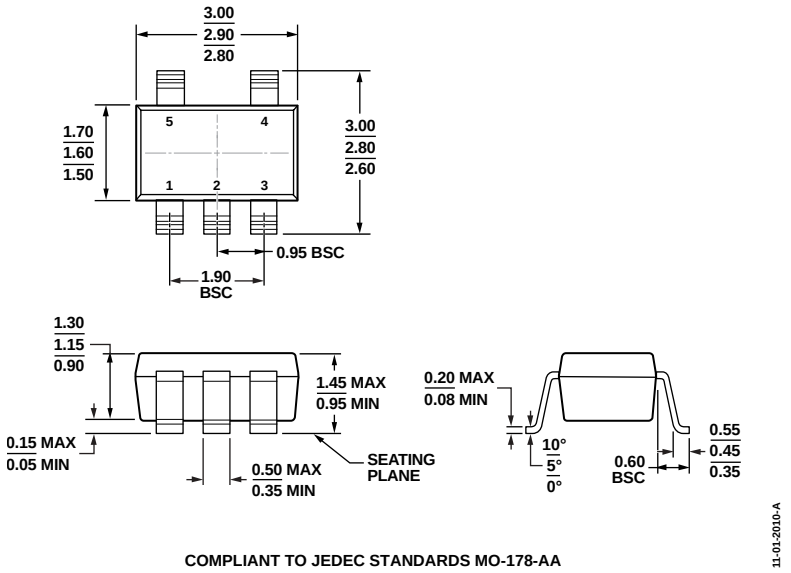


Figure 38. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding Code
AD8005ANZ	–40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
AD8005ARZ	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8005ARZ-REEL	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8005ARZ-REEL7	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8005ARTZ-R2	–40°C to +85°C	5-Lead Small Outline Transistor Package [SOT-23]	RJ-5	H05
AD8005ARTZ-REEL7	–40°C to +85°C	5-Lead Small Outline Transistor Package [SOT-23]	RJ-5	H05
AD8005AR-EBZ		Evaluation Board		
AD8005ART-EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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