TABLE OF CONTENTS

REVISION HISTORY

11/10—Rev. C to Rev. D

Changes to $D_{OUT}A$ and $D_{OUT}B$ Description in Table 6 ... 9
Changes to Serial Interface Section ... 22
Changes to Figure 27 ... 23

10/10—Rev. B to Rev. C

Changes to $D_{OUT}A$ and $D_{OUT}B$ Description in Table 6 ... 9
Changes to Serial Interface Section ... 22
Changes to Figure 27 ... 23

8/09—Rev. A to Rev. B

Changes to Table 2 ... 4
Changes to Table 3 ... 6

9/07—Rev. 0 to Rev. A

Changes to Title ... 1
Changes to Specifications ... 3
Changes to Figure 5 ... 11
Changes to Terminology Section ... 14
Changes to Figure 20 ... 18
Changes to Figure 28 ... 23
Updated Outline Dimensions ... 28
Changes to Ordering Guide ... 28

5/07—Revision 0: Initial Version

SPECIFICATIONS

AV_{CC} = DV_{CC} = 4.75 V to 5.25 V, V_{DD} = 11.5 V to 16.5 V, V_{SS} = −16.5 V to −11.5 V, V_{DRIVE} = 2.7 V to 5.25 V, f_S = 1.12 MSPS, f_{SCLK} = 48 MHz, V_{REF} = 2.5 V internal/external, T_A = −40°C to +85°C, unless otherwise noted.

Table 2. AD7366

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 50 kHz sine wave
Signal-to-Noise Ratio (SNR)[1]	70	72		dB	
Signal-to-Noise + Distortion Ratio (SINAD)[1]	70	71		dB	
Total Harmonic Distortion (THD)[1]		−85	−78	dB	
Spurious-Free Dynamic Range (SFDR)		−87	−78	dB	
Intermodulation Distortion (IMD)[1]					fa = 49 kHz, fb = 51 kHz
Second-Order Terms		−88		dB	
Third-Order Terms		−88		dB	
Channel-to-Channel Isolation[1]		−90		dB	
SAMPLE AND HOLD					
Aperture Delay[2]			10	ns	
Aperture Jitter[2]		40		ps	
Aperture Delay Matching[2]		±100		ps	
Full Power Bandwidth		35		MHz	@ 3 dB, ±10 V range
		8		MHz	@ 0.1 dB, ±10 V range
DC ACCURACY					
Resolution	12			Bits	
Integral Nonlinearity (INL)[1]		±0.5	±1	LSB	
Differential Nonlinearity (DNL)[1]		±0.25	±0.5	LSB	Guaranteed no missed codes to 12 bits
Positive Full-Scale Error[1]		±1	±7	LSB	±5 V and ±10 V analog input range
		±1	±6	LSB	0 V to 10 V analog input range
Positive Full-Scale Error Match[1]		±1.5		LSB	Matching from ADC A to ADC B
		±0.1		LSB	Channel-to-channel matching for ADC A and ADC B
Zero Code Error[1]		±0.5	±3	LSB	±5 V and ±10 V analog input range
		±1	±6	LSB	0 V to 10 V analog input range
Zero Code Error Match[1]		±1.5		LSB	Matching from ADC A to ADC B
		±0.1		LSB	Channel-to-channel matching for ADC A and ADC B
Negative Full-Scale Error[1]		±1	±7	LSB	±5 V and ±10 V analog input range
		±1	±6	LSB	0 V to 10 V analog input range
Negative Full-Scale Error Match[1]		±1.5		LSB	Matching from ADC A to ADC B
		±0.1		LSB	Channel-to-channel matching for ADC A and ADC B
ANALOG INPUT					
Input Voltage Ranges					Programmed via RANGE pins; see Table 8
			±10	V	
			±5	V	
			0 to 10	V	
DC Leakage Current		±0.01	±1	µA	
Input Capacitance		9		pF	When in track, ±10 V range
		13		pF	When in track, ±5 V and 0 V to 10 V range
Input Impedance		260		kΩ	±10 V @ 1 MSPS
		2.5		MΩ	±10 V @ 100 kSPS
		125		kΩ	±5 V and 0 V to 10 V range @ 1 MSPS
		1.2		MΩ	±5 V and 0 V to 10 V range @ 100 kSPS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[3]	2.495	2.5	2.505	V	±0.2% max @ 25°C
Long-Term Stability		150		ppm	1000 hours
Output Voltage Hysteresis[1]		50		ppm	
Reference Input Voltage Range	2.5		3.0	V	
DC Leakage Current		±0.01	±1	µA	External reference applied to Pin D_{CAP}A/Pin D_{CAP}B
Input Capacitance		25		pF	±5 V and ±10 V analog input range
		17		pF	0 V to 10 V analog input range
D_{CAP}A, D_{CAP}B Output Impedance		7		Ω	
Reference Temperature Coefficient		6	25	ppm/°C	
V_{REF} Noise		20		µV rms	Bandwidth = 3 kHz
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DRIVE}$			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}		±0.01	±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[2]		6		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$V_{DRIVE} - 0.2$			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current		±0.01	±1	µA	
Floating State Output Capacitance[2]		8		pF	
CONVERSION RATE					
Conversion Time			610	ns	
Track/Hold Acquisition Time[2]			140	ns	Full-scale step input
Throughput Rate			1.12	MSPS	4.75 V ≤ V_{DRIVE} ≤ 5.25 V, f_{SCLK} = 48 MHz
		1		MSPS	2.7 V ≤ V_{DRIVE} < 4.75 V, f_{SCLK} = 35 MHz
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{CC}	4.75		5.25	V	See Table 7
V_{DD}	+11.5		+16.5	V	See Table 7
V_{SS}	−16.5		−11.5	V	See Table 7
V_{DRIVE}	2.7		5.25	V	
Normal Mode (Static)					
I_{DD}		370	550	µA	V_{DD} = +16.5 V
I_{SS}		40	60	µA	V_{SS} = −16.5 V
I_{CC}		1.5	2.25	mA	V_{CC} = 5.5 V
Normal Mode (Operational)					f_S = 1.12 MSPS
I_{DD}		1.8	2.0	mA	V_{DD} = +16.5 V
I_{SS}		1.5	1.6	mA	V_{SS} = −16.5 V
I_{CC}		5	5.65	mA	V_{CC} = 5.25 V, internal reference enabled
Shutdown Mode					
I_{DD}		0.01	1	µA	V_{DD} = +16.5 V
I_{SS}		0.01	1	µA	V_{SS} = −16.5 V
I_{CC}		0.3	3	µA	V_{CC} = 5.25 V
Power Dissipation					
Normal Mode (Operational)			89.1	mW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = 5.25 V, f_S = 1.12 MSPS
		50		mW	±10 V input range, f_S = 1.12 MSPS
		70		mW	±5 V and 0 V to 10 V input range, f_S = 1.12 MSPS
Shutdown Mode		1.9	48.75	µW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = 5.25 V

[1] See the Terminology section.
[2] Sample tested during initial release to ensure compliance.
[3] Refers to Pin D_{CAP}A or Pin D_{CAP}B specified for 25°C.

AV_{CC} = DV_{CC} = 4.75 V to 5.25 V, V_{DD} = 11.5 V to 16.5 V, V_{SS} = −16.5 V to −11.5 V, V_{DRIVE} = 2.7 V to 5.25 V, f_S = 1 MSPS, f_{SCLK} = 48 MHz, V_{REF} = 2.5 V internal/external, T_A = −40°C to +85°C, unless otherwise noted.

Table 3. AD7367

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 50 kHz sine wave
Signal-to-Noise Ratio (SNR)[1]	74	76		dB	
Signal-to-Noise + Distortion Ratio (SINAD)[1]	73	75		dB	
Total Harmonic Distortion (THD)[1]		−84	−78	dB	
Spurious-Free Dynamic Range (SFDR)		−87	−79	dB	
Intermodulation Distortion (IMD)[1]					fa = 49 kHz, fb = 51 kHz
Second-Order Terms		−91		dB	
Third-Order Terms		−89		dB	
Channel-to-Channel Isolation[1]		−90		dB	
SAMPLE AND HOLD					
Aperture Delay[2]			10	ns	
Aperture Jitter[2]		40		ps	
Aperture Delay Matching[2]		±100		ps	
Full Power Bandwidth		35		MHz	@ 3 dB, ±10 V range
		8		MHz	@ 0.1 dB, ±10 V range
DC ACCURACY					
Resolution	14			Bits	
Integral Nonlinearity (INL)[1]		±2	±3.5	LSB	
Differential Nonlinearity (DNL)[1]		±0.5	±0.90	LSB	Guaranteed no missed codes to 14 bits
Positive Full-Scale Error[1]		±4	±20	LSB	±5 V and ±10 V analog input range
		±5	±20	LSB	0 V to 10 V analog input range
Positive Full-Scale Error Match[1]		±3		LSB	Matching from ADC A to ADC B
		±0.2		LSB	Channel-to-channel matching for ADC A and ADC B
Zero Code Error[1]		±1	±10	LSB	±5 V and ±10 V analog input range
		±5	±20	LSB	0 V to 10 V analog input range
Zero Code Error Match[1]		±3		LSB	Matching from ADC A to ADC B
		±0.2		LSB	Channel-to-channel matching for ADC A and ADC B
Negative Full-Scale Error[1]		±4	±20	LSB	±5 V and ±10 V analog input range
		±5	±20	LSB	0 V to 10 V analog input range
Negative Full-Scale Error Match[1]		±3		LSB	Matching from ADC A to ADC B
		±0.2		LSB	Channel-to-channel matching for ADC A and ADC B
ANALOG INPUT					
Input Voltage Ranges					Programmed via RANGE pins; see Table 8
			±10	V	
			±5	V	
			0 to 10	V	
DC Leakage Current		±0.01	±1	µA	
Input Capacitance		9		pF	When in track, ±10 V range
		13		pF	When in track, ±5 V and 0 V to 10 V range
Input Impedance		260		kΩ	±10 V @ 1 MSPS
		2.5		MΩ	±10 V @ 100 kSPS
		125		kΩ	±5 V and 0 V to 10 V range @ 1 MSPS
		1.2		MΩ	±5 V and 0 V to 10 V range @ 100 kSPS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[3]	2.495	2.5	2.505	V	±0.2% max @ 25°C
Long-Term Stability		150		ppm	1000 hours
Output Voltage Hysteresis[1]		50		ppm	
Reference Input Voltage Range	2.5		3.0	V	
DC Leakage Current		±0.01	±1	µA	External reference applied to Pin $D_{CAP}A$/Pin $D_{CAP}B$
Input Capacitance		25		pF	±5 V and ±10 V analog input range
		17		pF	0 V to 10 V analog input range
$D_{CAP}A$, $D_{CAP}B$ Output Impedance		7		Ω	
Reference Temperature Coefficient		6	25	ppm/°C	
V_{REF} Noise		20		µV rms	Bandwidth = 3 kHz
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DRIVE}$			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}		±0.01	±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[2]		6		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$V_{DRIVE} - 0.2$			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current		±0.01	±1	µA	
Floating State Output Capacitance[2]		8		pF	
CONVERSION RATE					
Conversion Time			680	ns	
Track/Hold Acquisition Time[2]			140	ns	Full-scale step input
Throughput Rate			1	MSPS	4.75 V ≤ V_{DRIVE} ≤ 5.25 V, f_{SCLK} = 48 MHz
		900		kSPS	2.7 V ≤ V_{DRIVE} < 4.75 V, f_{SCLK} = 35 MHz
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{CC}	4.75		5.25	V	See Table 7
V_{DD}	+11.5		+16.5	V	See Table 7
V_{SS}	−16.5		−11.5	V	See Table 7
V_{DRIVE}	2.7		5.25	V	
Normal Mode (Static)					
I_{DD}		370	550	µA	V_{DD} = +16.5 V
I_{SS}		40	60	µA	V_{SS} = −16.5 V
I_{CC}		1.5	2.25	mA	V_{CC} = 5.5 V
Normal Mode (Operational)					f_S = 1 MSPS
I_{DD}		1.8	2.0	mA	V_{DD} = +16.5 V
I_{SS}		1.5	1.6	mA	V_{SS} = −16.5 V
I_{CC}		5	5.65	mA	V_{CC} = 5.25 V, internal reference enabled
Shutdown Mode					
I_{DD}		0.01	1	µA	V_{DD} = +16.5 V
I_{SS}		0.01	1	µA	V_{SS} = −16.5 V
I_{CC}		0.3	3	µA	V_{CC} = 5.25 V
Power Dissipation					
Normal Mode (Operational)		80.7	89.1	mW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = 5.25 V
		50		mW	±10 V input range, f_S = 1 MSPS
		70		mW	±5 V and 0 V to 10 V input range, f_S = 1 MSPS
Shutdown Mode		1.9	48.75	µW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = 5.25 V

[1] See the Terminology section.
[2] Sample tested during initial release to ensure compliance.
[3] Refers to Pin $D_{CAP}A$ or Pin $D_{CAP}B$ specified for 25°C.

TIMING SPECIFICATIONS

AV_{CC} = DV_{CC} = 4.75 V to 5.25 V, V_{DD} = 11.5 V to 16.5 V, V_{SS} = −16.5 V to −11.5 V, V_{DRIVE} = 2.7 V to 5.25 V, T_A = −40°C to +85°C, unless otherwise noted.[1]

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Test Conditions/Comments
	2.7 V ≤ V_{DRIVE} < 4.75 V	**4.75 V ≤ V_{DRIVE} ≤ 5.25 V**		
$t_{CONVERT}$				Conversion time, internal clock; $\overline{CNVST}$ falling edge to BUSY falling edge
	680	680	ns max	AD7367
	610	610	ns max	AD7366
f_{SCLK}	10	10	kHz min	Frequency of serial read clock
	35	48	MHz max	
t_{QUIET}	30	30	ns min	Minimum quiet time required between the end of serial read and the start of the next conversion
t_1	10	10	ns min	Minimum $\overline{CNVST}$ low pulse
t_2	40	40	ns min	$\overline{CNVST}$ falling edge to BUSY rising edge
t_3	0	0	ns min	BUSY falling edge to MSB, valid when $\overline{CS}$ is low for t_4 prior to BUSY going low
t_4	10	10	ns max	Delay from $\overline{CS}$ falling edge until Pin 1 (D_{OUT}A) and Pin 23 (D_{OUT}B) are three-state disabled
t_5[2]	20	14	ns max	Data access time after SCLK falling edge
t_6	7	7	ns min	SCLK to data valid hold time
t_7	0.3 × t_{SCLK}	0.3 × t_{SCLK}	ns min	SCLK low pulse width
t_8	0.3 × t_{SCLK}	0.3 × t_{SCLK}	ns min	SCLK high pulse width
t_9	10	10	ns max	$\overline{CS}$ rising edge to D_{OUT}A, D_{OUT}B, high impedance
$t_{POWER-UP}$	70	70	µs max	Power-up time from shutdown mode; time required between $\overline{CNVST}$ rising edge and $\overline{CNVST}$ falling edge

[1] Sample tested during initial release to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications are with a 25 pF load capacitance. With a load capacitance greater than 25 pF, a digital buffer or latch must be used. See the Terminology section, Figure 25, and Figure 26.

[2] The time required for the output to cross is 0.4 V or 2.4 V.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{DD} to AGND, DGND	−0.3 V to +16.5 V
V_{SS} to AGND, DGND	−16.5 V to +0.3 V
V_{DRIVE} to DGND	−0.3 V to DV_{CC}
V_{DD} to AV_{CC}	(V_{CC} − 0.3 V) to +16.5 V
AV_{CC} to AGND, DGND	−0.3 V to +7 V
DV_{CC} to AV_{CC}	−0.3 V to +0.3 V
DV_{CC} to DGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to DV_{CC}
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
$D_{CAP}A$, $D_{CAP}B$ Input to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	128°C/W
θ_{JC} Thermal Impedance	42°C/W
Pb-Free Temperature, Soldering Reflow	260°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA will not cause latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

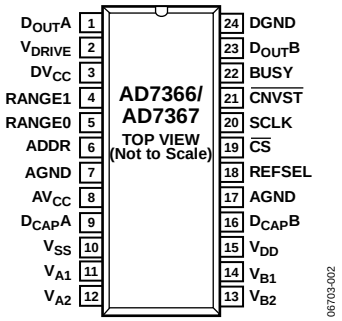


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 23	$D_{OUT}A$, $D_{OUT}B$	Serial Data Outputs. The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input; 12 SCLK cycles are required to access a result from the AD7366, and 14 SCLK cycles are required for the AD7367. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data stream consists of the 12 bits of conversion data for the AD7366 and 14 bits for the AD7367 and is provided MSB first. If $\overline{CS}$ is held low for a further 14 SCLK cycles, on either $D_{OUT}A$ or $D_{OUT}B$, the data from the other ADC follows on that D_{OUT} pin. Note, the second serial result from the AD7366 is preceeded by two zeros. Therfore data from a simultaneous conversion on both ADCs can be gathered in serial format on either $D_{OUT}A$ or $D_{OUT}B$ using only one serial port. See the Serial Interface section for more information.
2	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. This pin should be decoupled to DGND. The voltage range on this pin is 2.7 V to 5.25 V and may be different from the voltage at AV_{CC} and DV_{CC}, but should never exceed either by more than 0.3 V. To achieve a throughput rate of 1.12 MSPS for the AD7366 or 1 MSPS for the AD7367, V_{DRIVE} must be ≥ 4.75 V.
3	DV_{CC}	Digital Supply Voltage, 4.75 V to 5.25 V. The DV_{CC} and AV_{CC} voltages should ideally be at the same potential. For best performance, it is recommended that the DV_{CC} and AV_{CC} pins be shorted together, to ensure that the voltage difference between them never exceeds 0.3 V even on a transient basis. This supply should be decoupled to DGND. Place 10 µF and 100 nF decoupling capacitors on the DV_{CC} pin.
4, 5	RANGE1, RANGE0	Analog Input Range Selection, Logic Inputs. The polarity on these pins determines the input range of the analog input channels. See the Analog Inputs section and Table 8 for details.
6	ADDR	Multiplexer Select, Logic Input. This input is used to select the pair of channels to be simultaneously converted, either Channel 1 of both ADC A and ADC B, or Channel 2 of both ADC A and ADC B. The logic state on this pin is latched on the rising edge of BUSY to set up the multiplexer for the next conversion.
7, 17	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7366/AD7367. All analog input signals and any external reference signal should be referred to this AGND voltage. Both AGND pins should connect to the AGND plane of a system. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
8	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for the ADC cores. The AV_{CC} and DV_{CC} voltages should ideally be at the same potential. For best performance, it is recommended that the DV_{CC} and AV_{CC} pins be shorted together, to ensure that the voltage difference between them never exceeds 0.3 V even on a transient basis. This supply should be decoupled to AGND. Place 10 µF and 100 nF decoupling capacitors on the AV_{CC} pin.
9, 16	$D_{CAP}A$, $D_{CAP}B$	Decoupling Capacitor Pins. Decoupling capacitors are connected to these pins to decouple the reference buffer for each respective ADC. For best performance, it is recommended that a 680 nF decoupling capacitor be used on these pins. Provided the output is buffered, the on-chip reference can be taken from these pins and applied externally to the rest of a system.
10	V_{SS}	Negative Power Supply Voltage. This is the negative supply voltage for the high voltage analog input structure of the AD7366/AD7367. The supply must be less than a maximum voltage of −11.5 V for all analog input ranges. See Table 7 for more details. Place 10 µF and 100 nF decoupling capacitors on the V_{SS} pin.
11, 12	V_{A1}, V_{A2}	Analog Inputs of ADC A. Both analog inputs are single-ended. The analog input range on these channels is determined by the RANGE0 and RANGE1 pins.
13, 14	V_{B2}, V_{B1}	Analog Inputs of ADC B. Both analog inputs are single-ended. The analog input range on these channels is determined by the RANGE0 and RANGE1 pins.
15	V_{DD}	Positive Power Supply Voltage. This is the positive supply voltage for the high voltage analog input structure of the AD7366/AD7367. The supply must be greater than a minimum voltage of 11.5 V for all analog input ranges. See Table 7 for more details. Place 10 µF and 100 nF decoupling capacitors on the V_{DD} pin.

Pin No.	Mnemonic	Description
18	REFSEL	Internal/External Reference Selection, Logic Input. If this pin is tied to logic high, the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. In addition, Pin $D_{CAP}A$ and Pin $D_{CAP}B$ must be tied to decoupling capacitors. If the REFSEL pin is tied to GND, an external reference can be supplied to the AD7366/AD7367 through the $D_{CAP}A$ pin, the $D_{CAP}B$ pin, or both pins.
19	$\overline{CS}$	Chip Select, Active Low Logic Input. This input frames the serial data transfer. When $\overline{CS}$ is logic low, the output bus is enabled and the conversion result is output on $D_{OUT}A$ and $D_{OUT}B$.
20	SCLK	Serial Clock, Logic Input. A serial clock input provides the SCLK for accessing the data from the AD7366/AD7367.
21	$\overline{CNVST}$	Conversion Start, Logic Input. This pin is edge triggered. On the falling edge of this input, the track/hold goes into hold mode and the conversion is initiated. If $\overline{CNVST}$ is low at the end of a conversion, the part goes into power-down mode. In this case, the rising edge of $\overline{CNVST}$ instructs the part to power up again.
22	BUSY	Busy Output. BUSY transitions high when a conversion is started and remains high until the conversion is complete.
24	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7366/AD7367. The DGND pin should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

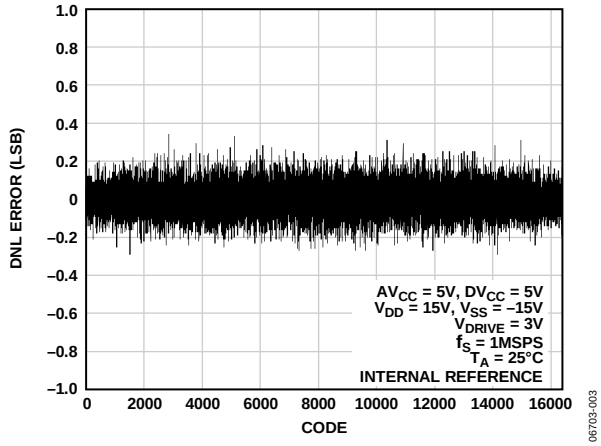


Figure 3. AD7367 Typical DNL

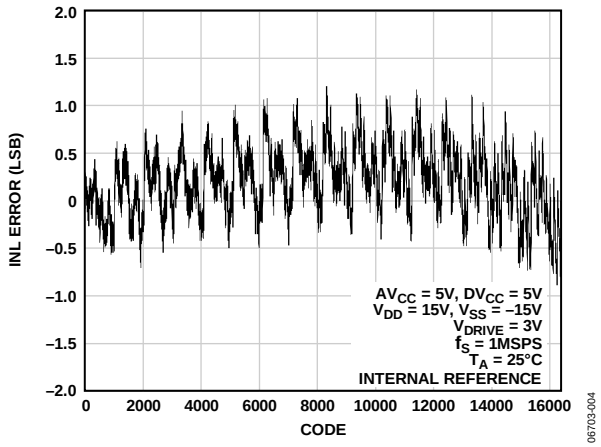


Figure 4. AD7367 Typical INL

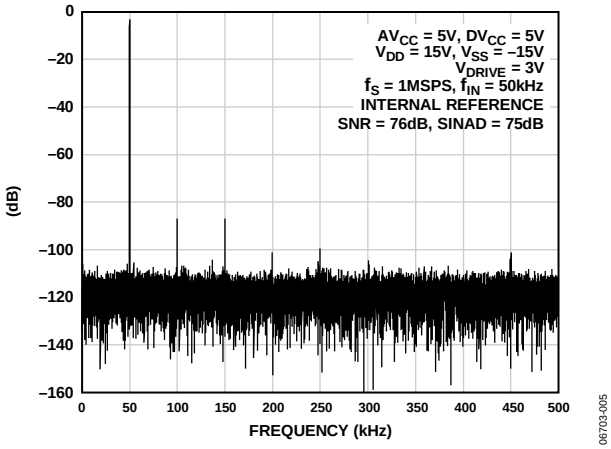


Figure 5. AD7367 FFT

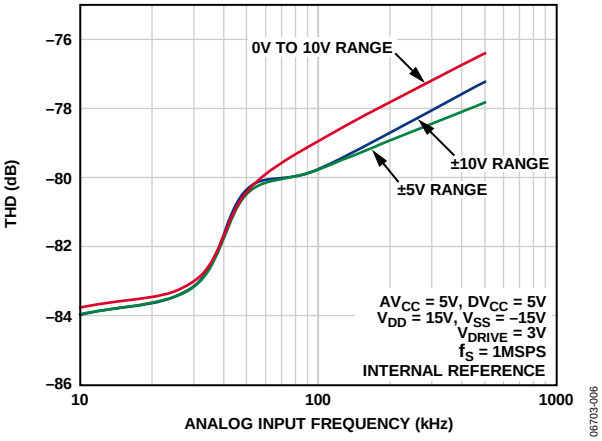


Figure 6. THD vs. Analog Input Frequency

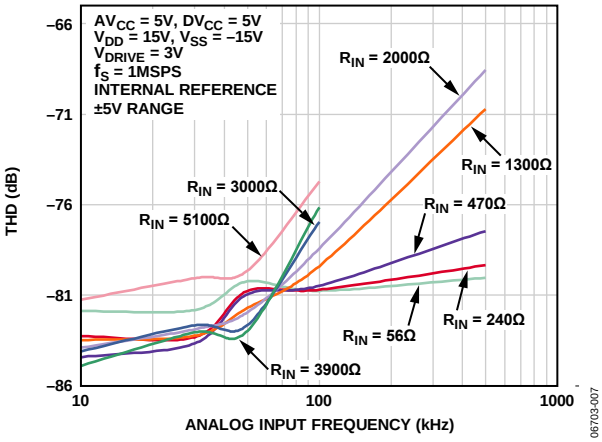


Figure 7. THD vs. Analog Input Frequency for Various Source Impedances

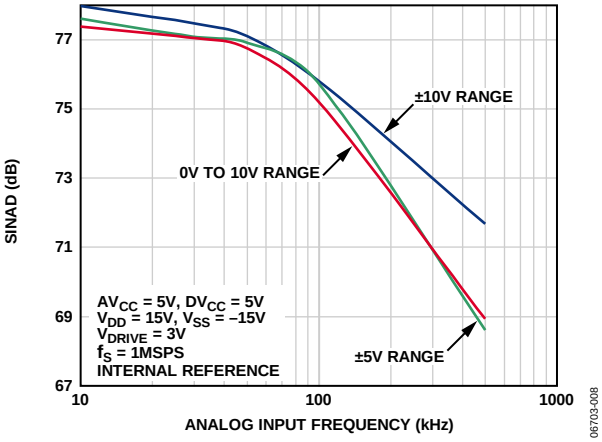


Figure 8. SINAD vs. Analog Input Frequency

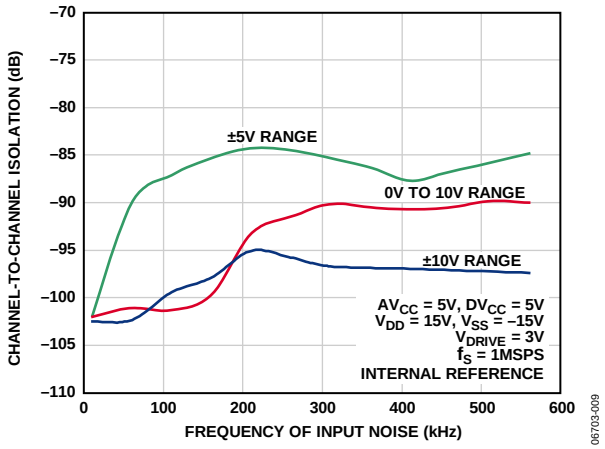


Figure 9. Channel-to-Channel Isolation

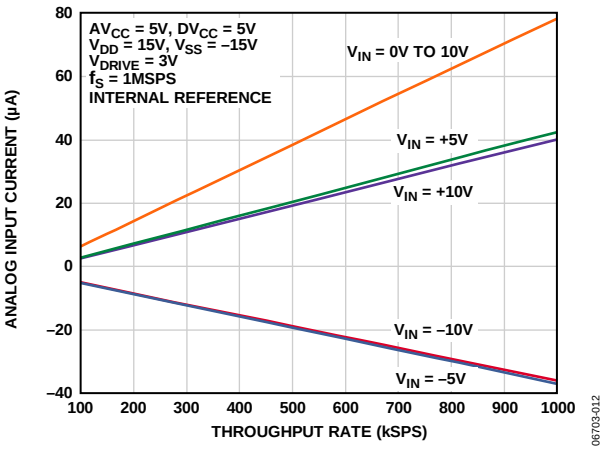


Figure 12. Analog Input Current vs. Throughput Rate

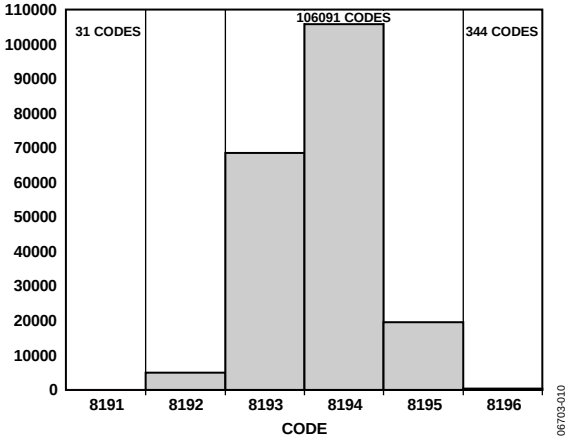


Figure 10. Histogram of Codes for 200k Samples

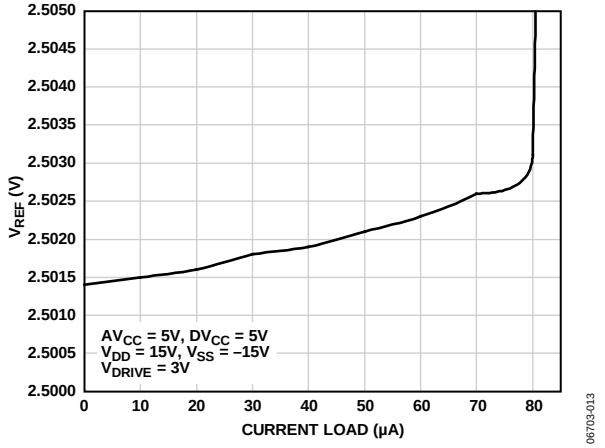


Figure 13. V_{REF} vs. Reference Output Current Drive

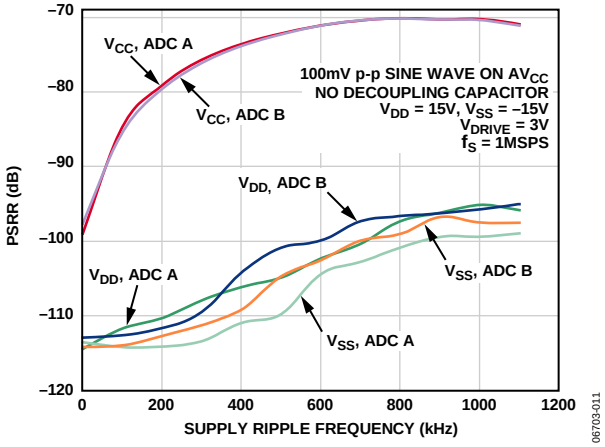


Figure 11. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

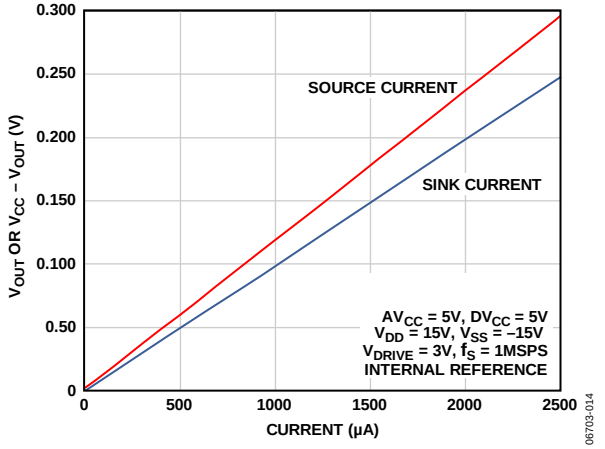


Figure 14. D_{OUT} Source Current vs. (V_{CC} – V_{OUT}) and D_{OUT} Sink Current vs. V_{OUT}

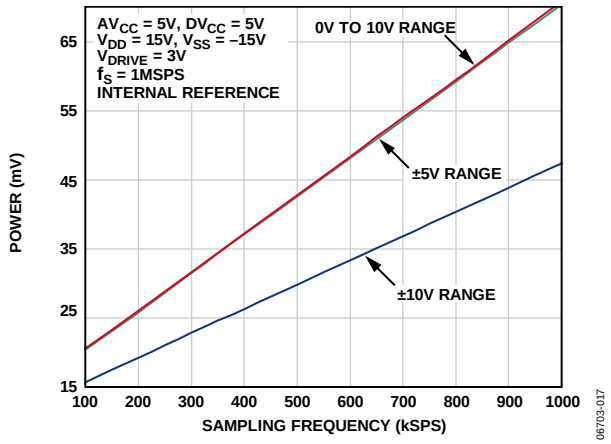


Figure 15. Power vs. Sampling Frequency in Normal Mode

TERMINOLOGY

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Zero Code Error
The deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, that is, AGND − ½ LSB for bipolar ranges and 2 × V_{REF} − 1 LSB for the unipolar range.

Positive Full-Scale Error
The deviation of the last code transition (011…110) to (011…111) from the ideal (that is, +4 × V_{REF} − 1 LSB or +2 × V_{REF} − 1 LSB) after the zero code error has been factored out.

Negative Full-Scale Error
The deviation of the first code transition (10…000) to (10…001) from the ideal (that is, −4 × V_{REF} + 1 LSB, −2 × V_{REF} + 1 LSB, or AGND + 1 LSB) after the zero code error has been factored out.

Zero Code Error Match
The difference in zero code error across all channels.

Positive Full-Scale Error Match
The difference in positive full-scale error across all channels.

Negative Full-Scale Error Match
The difference in negative full-scale error across all channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of a conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±½ LSB, after the end of a conversion.

Signal-to-Noise (+ Distortion) Ratio (SINAD)
This ratio is the measured ratio of signal-to-noise (+ distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-noise (+ distortion) ratio for an ideal N-bit converter with a sine wave input is as follows:

Signal-to-Noise (+ Distortion) = (6.02*N* + 1.76) dB

Thus, for a 12-bit converter, the SINAD is 74 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7366/AD7367, THD is defined as follows:

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic, or spurious noise, is the ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum. However, for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels when operating in any of the input ranges. It is measured by applying a full-scale, 150 kHz sine wave signal to all unselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. The figure given is the typical value across all four channels for the AD7366/AD7367 (see Figure 9 for more information).

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at the sum, and different frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7366/AD7367 are tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the converter's linearity. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see Figure 11).

Thermal (or Output Voltage) Hysteresis
Thermal (or output voltage) hysteresis is defined as the absolute maximum change of reference output voltage after the device is cycled through temperature from either

T_HYS+ = +25°C to T_{MAX} to +25°C

or

T_HYS- = +25°C to T_{MIN} to +25°C

It is expressed in ppm using the following equation:

$$V_{HYS}\,(\text{ppm}) = \left|\frac{V_{REF}(25°\text{C}) - V_{REF}(T\_HYS)}{V_{REF}(25°\text{C})}\right| \times 10^6$$

where:
V_{REF}(25°C) is V_{REF} at 25°C.
$V_{REF}(T\_HYS)$ is the maximum change of V_{REF} at T_HYS+ or T_HYS−.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7366/AD7367 are fast, dual, 2-channel, 12-/14-bit, bipolar input, simultaneous sampling, serial ADCs. The AD7366/AD7367 can accept bipolar input ranges of ±10 V and ±5 V. They can also accept a unipolar input range of 0 V to 10 V. The AD7366/AD7367 require V_{DD} and V_{SS} dual supplies for the high voltage analog input structures. These supplies must be equal to or greater than ±11.5 V. See Table 7 for the minimum requirements on these supplies for each analog input range. The AD7366/AD7367 require a low voltage 4.75 V to 5.25 V AV_{CC} supply to power the ADC core.

Table 7. Reference and Supply Requirements for Each Analog Input Range

Selected Analog Input Range (V)	Reference Voltage (V)	Full-Scale Input Range (V)	AV_{CC} (V)	Minimum V_{DD}/V_{SS} (V)
±10	2.5	±10	5	±11.5
	3.0	±12	5	±12
±5	2.5	±5	5	±11.5
	3.0	±6	5	±11.5
0 to 10	2.5	0 to 10	5	±11.5
	3.0	0 to 12	5	±12

The AD7366/AD7367 contain two on-chip, track-and-hold amplifiers, two successive approximation ADCs, and a serial interface with two separate data output pins. The AD7366/AD7367 are available in a 24-lead TSSOP, offering the user considerable space-saving advantages over alternative solutions. The AD7366/AD7367 require a $\overline{\text{CNVST}}$ signal to start conversion. On the falling edge of $\overline{\text{CNVST}}$, both track-and-holds are placed into hold mode and the conversions are initiated. The BUSY signal goes high to indicate that the conversions are taking place. The clock source for each successive approximation ADC is provided by an internal oscillator. The BUSY signal goes low to indicate the end of conversion. On the falling edge of BUSY, the track-and-hold returns to track mode. When the conversion is finished, the serial clock input accesses data from the part.

The AD7366/AD7367 have an on-chip 2.5 V reference that can be disabled if an external reference is preferred. If the internal reference is to be used elsewhere in a system, the output from $D_{CAP}A$ and $D_{CAP}B$ must first be buffered. On power-up, the REFSEL pin must be tied to either a high or low logic state to select either the internal or external reference option. If the internal reference is the preferred option, the user must tie the REFSEL pin logic high. Alternatively, if REFSEL is tied to GND then an external reference can be supplied to both ADCs through the $D_{CAP}A$ and $D_{CAP}B$ pins.

The analog inputs are configured as two single-ended inputs for each ADC. The input voltage range can be selected by programming the RANGE bits as shown in Table 8.

CONVERTER OPERATION

The AD7366/AD7367 have two successive approximation ADCs, each based around two capacitive DACs. Figure 16 and Figure 17 show simplified schematics of an ADC in acquisition and conversion phases. The ADC comprises control logic, a SAR, and a capacitive DAC. In Figure 16 (the acquisition phase), SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the signal on the input.

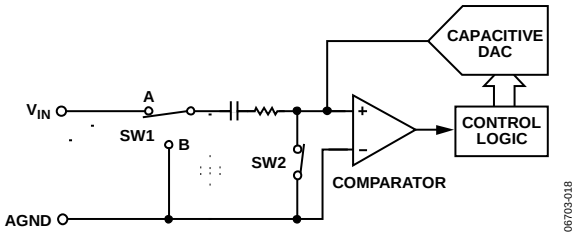


Figure 16. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 17), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is balanced again, the conversion is complete. The control logic generates the ADC output code.

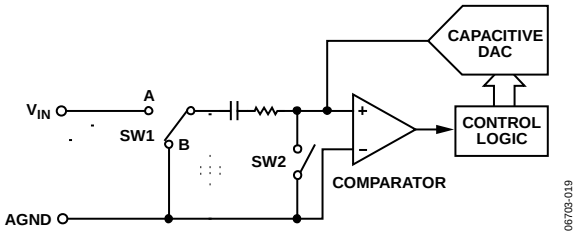


Figure 17. ADC Conversion Phase

ANALOG INPUTS

Each ADC in the AD7366/AD7367 has two single-ended analog inputs. Figure 18 shows the equivalent circuit of the analog input structure of the AD7366/AD7367. The two diodes provide ESD protection. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and to start conducting current into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 170 Ω. Capacitor C1 can primarily be attributed to pin capacitance, while Capacitor C2 is the sampling capacitor of the ADC. The total lumped capacitance of C1 and C2 is approximately 9 pF for the ±10 V input range and approximately 13 pF for all other input ranges.

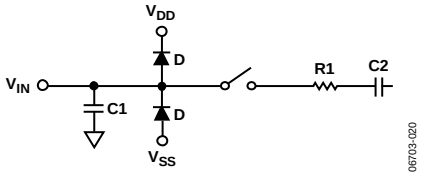


Figure 18. Equivalent Analog Input Structure

The AD7366/AD7367 can handle true bipolar input voltages. The analog input can be set to one of three ranges: ±10 V, ±5 V, or 0 V to 10 V. The logic levels on Pin RANGE0 and Pin RANGE1 determine which input range is selected as outlined in Table 8. These range bits should not be changed during the acquisition time prior to a conversion, but can be changed at any other time.

Table 8. Analog Input Range Selection

RANGE1	RANGE0	Range Selected
0	0	±10 V
0	1	±5 V
1	0	0 V to 10 V
1	1	Do not program

The AD7366/AD7367 require V_{DD} and V_{SS} dual supplies for the high voltage analog input structures. These supplies must be equal to or greater than ±11.5 V. See Table 7 for the requirements on these supplies. The AD7366/AD7367 require a low voltage 4.75 V to 5.25 V AV_{CC} supply to power the ADC core, a 4.75 V to 5.25 V DV_{CC} supply for digital power, and a 2.7 V to 5.25 V V_{DRIVE} supply for interface power.

Channel selection is made via the ADDR pin, as shown in Table 9. The logic level on the ADDR pin is latched on the rising edge of the BUSY signal for the next conversion, not the one in progress. When power is first supplied to the AD7366/AD7367, the default channel selection is V_{A1} and V_{B1}.

Table 9. Channel Selection

ADDR	Channels Selected
0	V_{A1}, V_{B1}
1	V_{A2}, V_{B2}

TRANSFER FUNCTION

The output coding of the AD7366/AD7367 is twos complement. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size is dependent on the analog input range selected (see Table 10). The ideal transfer characteristic is shown in Figure 19.

Table 10. LSB Sizes for Each Analog Input Range

	AD7366		AD7367	
Input Range	Full-Scale Range	LSB Size (mV)	Full-Scale Range	LSB Size (mV)
±10 V	20 V/4096	4.88	20 V/16,384	1.22
±5 V	10 V/4096	2.44	10 V/16,384	0.61
0 V to 10 V	10 V/4096	2.44	10 V/16,384	0.61

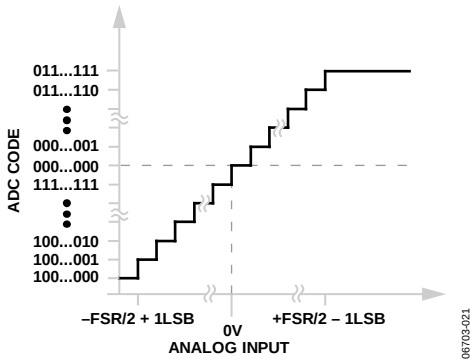


Figure 19. Transfer Characteristic

Track-and-Hold

The track-and-hold on the analog input of the AD7366/AD7367 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-/14-bit accuracy. The input bandwidth of the track-and-hold is greater than the Nyquist rate of the ADC. The AD7366/AD7367 can handle frequencies up to 35 MHz.

The track-and-hold enters its tracking mode when the BUSY signal goes low after the $\overline{CS}$ falling edge. The time required to acquire an input signal depends on how quickly the sampling capacitor is charged. With zero source impedance, 140 ns is sufficient to acquire the signal to the 12-bit level for the AD7366 and the 14-bit level for the AD7367. The acquisition time for the ±10 V, ±5 V, and 0 V to 10 V ranges to settle to within ±½ LSB is typically 140 ns. The ADC returns to hold mode on the falling edge of $\overline{CNVST}$.

The acquisition time required is calculated using the following formula:

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R)\ C)$$

where:
C is the sampling capacitance.
R is the resistance seen by the track-and-hold amplifier looking at the input.
R_{SOURCE} should include any extra source impedance on the analog input.

Unlike other bipolar ADCs, the AD7366/AD7367 do not have a resistive analog input structure. On the AD7366/AD7367, the bipolar analog signal is sampled directly onto the sampling capacitor. This gives the AD7366/AD7367 high analog input impedance. The analog input impedance can be calculated from the following formula:

$$Z = 1/(f_S \times C_S)$$

where:
f_S is the sampling frequency.
C_S is the sampling capacitor value.

C_S depends on the analog input range chosen (see the Analog Inputs section). When operating at 1 MSPS, the analog input impedance is typically 260 kΩ for the ±10 V range. As the sampling frequency is reduced, the analog input impedance further increases. As the analog input impedance increases, the current required to drive the analog input therefore decreases (see Figure 7 for more information).

TYPICAL CONNECTION DIAGRAM

Figure 20 shows a typical connection diagram for the AD7366/AD7367. In this configuration, the AGND pin is connected to the analog ground plane of the system, and the DGND pin is connected to the digital ground plane of the system. The analog inputs on the AD7366/AD7367 accept bipolar single-ended signals. The AD7366/AD7367 can operate with either an internal or an external reference. In Figure 20, the AD7366/AD7367 are configured to operate with the internal 2.5 V reference. A 680 nF decoupling capacitor is required when operating with the internal reference.

The AV_{CC} and DV_{CC} pins are connected to a 5 V supply voltage. The V_{DD} and V_{SS} are the dual supplies for the high voltage analog input structures. The voltage on these pins must be equal to or greater than ±11.5 V (see Table 7 for more information). The V_{DRIVE} pin is connected to the supply voltage of the microprocessor. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface. V_{DRIVE} can be set to 3 V or 5 V.

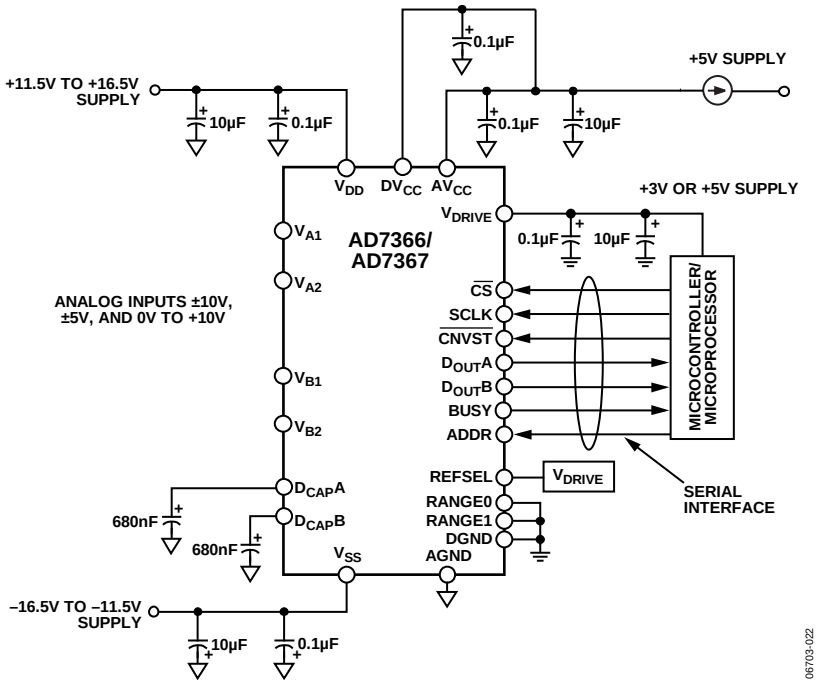


Figure 20. Typical Connection Diagram Using Internal Reference

DRIVER AMPLIFIER CHOICE

The AD7366/AD7367 have a total of four analog inputs, which operate in single-ended mode. The analog inputs for both ADCs can be programmed to one of the three analog input ranges. In applications where the signal source is high impedance, it is recommended that the signal be buffered before applying it to the ADC analog inputs. Figure 21 shows the configuration of the AD7366/AD7367 in single-ended mode.

In applications where the THD and SNR are critical specifications, the analog input of the AD7366/AD7367 should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and can necessitate the use of an input buffer amplifier.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated in the application. The THD increases as the source impedance increases and performance degrades. Figure 7 shows THD vs. the analog input frequency for various source impedances. Depending on the input range and analog input configuration selected, the AD7366/AD7367 can handle source impedances as illustrated in Figure 7.

Due to the programmable nature of the analog inputs on the AD7366/AD7367, the choice of op amp used to drive the inputs is a function of the particular application and depends on the analog input voltage range selected.

The driver amplifier must be able to settle for a full-scale step to a 14-bit level, 0.0061%, in less than the specified acquisition time of the AD7366/AD7367. An op amp such as the AD8021 meets this requirement when operating in single-ended mode. The AD8021 needs an external compensating NPO type of capacitor. The AD8022 can also be used in high frequency applications where a dual version is required. For lower frequency applications, recommended op amps are the AD797, AD845, and AD8610.

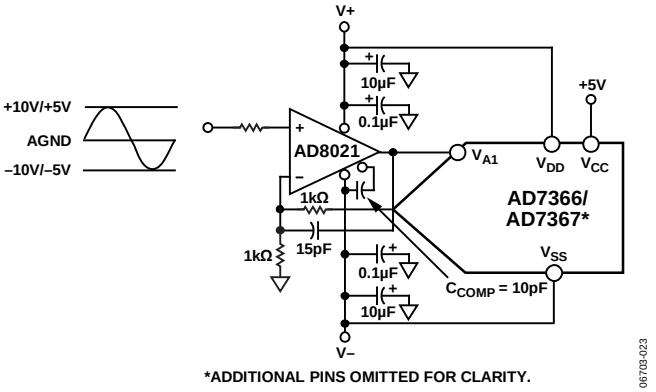


Figure 21. Typical Connection Diagram with the AD8021 for Driving the Analog Input

V_{DRIVE}

The AD7366/AD7367 also have a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7366/AD7367 were operated with a V_{CC} of 5 V, the V_{DRIVE} pin could be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors. Thus, the AD7366/AD7367 can be used with the ±10 V input range while still being able to interface to 3 V digital parts.

To achieve the maximum throughput rate of 1.12 MSPS for the AD7366 or 1 MSPS for the AD7367, V_{DRIVE} must be greater than or equal to 4.75 V (see Table 2 and Table 3). The maximum throughput rate with the V_{DRIVE} voltage set to less than 4.75 V and greater than 2.7 V is 1 MSPS for the AD7366 and 900 kSPS for the AD7367.

REFERENCE

The AD7366/AD7367 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The logic state of the REFSEL pin determines whether the internal reference is used. The internal reference is selected for both ADCs when the REFSEL pin is tied to logic high. If the REFSEL pin is tied to GND, an external reference can be supplied through the $D_{CAP}A$ and $D_{CAP}B$ pins. On power-up, the REFSEL pin must be tied to either a low or high logic state for the part to operate. Suitable reference sources for the AD7366/AD7367 include the AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When operating the AD7366/AD7367 in internal reference mode, the 2.5 V internal reference is available at the $D_{CAP}A$ and $D_{CAP}B$ pins, which should be decoupled to AGND using a 680 nF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system. The internal reference is capable of sourcing up to 150 µA with an analog input range of ±10 V and 70 µA for both the ±5 V and 0 V to 10 V ranges.

If the internal reference operation is required for the ADC conversion, the REFSEL pin must be tied to logic high on power-up. The reference buffer requires 70 µs to power up and charge the 680 nF decoupling capacitor during the power-up time.

The AD7366/AD7367 are specified for a 2.5 V to 3 V reference. When a 3 V reference is selected, the analog input ranges are ±12 V, ±6 V, and 0 V to 12 V. For these ranges, the V_{DD} supply must be greater than or equal to +12 V and the V_{SS} supply must be less than or equal to −12 V.

MODES OF OPERATION

The mode of operation of the AD7366/AD7367 is selected by the logic state of the $\overline{\text{CNVST}}$ signal at the end of a conversion. There are two possible modes of operation: normal mode and shutdown mode. These modes of operation are designed to provide flexible power management options, which can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

NORMAL MODE

Normal mode is intended for applications that require fast throughput rates. In normal mode, the AD7366/AD7367 remain fully powered at all times, so the user does not need to worry about power-up times. Figure 22 shows the general mode of operation of the AD7366 in normal mode; Figure 23 shows normal mode for the AD7367.

The conversion is initiated on the falling edge of $\overline{\text{CNVST}}$ as described in the Circuit Information section. To ensure that the part remains fully powered up at all times, $\overline{\text{CNVST}}$ must be at logic state high before the BUSY signal goes low. If $\overline{\text{CNVST}}$ is at logic state low when the BUSY signal goes low, the analog circuitry powers down and the part ceases converting. The BUSY signal remains high for the duration of the conversion.

The $\overline{\text{CS}}$ pin must be brought low to bring the data bus out of three-state. Therefore, 12 SCLK cycles are required to read the conversion result from the AD7366 and 14 SCLK cycles are required to read the conversion result from the AD7367. The D_{OUT} lines return to three-state only when $\overline{\text{CS}}$ is brought high. If $\overline{\text{CS}}$ is left low for an additional 12 SCLK cycles for the AD7366 or 14 SCLK cycles for the AD7367, the result from the other on-chip ADC is also accessed on the same D_{OUT} line, as shown in Figure 27 and Figure 28 (see the Serial Interface section).

When 24 SCLK cycles have elapsed for the AD7366 or 28 SCLK cycles for the AD7367, the D_{OUT} line returns to three-state only when $\overline{\text{CS}}$ is brought high, not on the 24th or 28th SCLK falling edge. If $\overline{\text{CS}}$ is brought high prior to this, the D_{OUT} line returns to three-state at that point. Thus, $\overline{\text{CS}}$ must be brought high when the read is completed, because the bus does not automatically return to three-state upon completion of the dual result read.

When a data transfer is complete and $D_{OUT}A$ and $D_{OUT}B$ have returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{\text{CNVST}}$ low again.

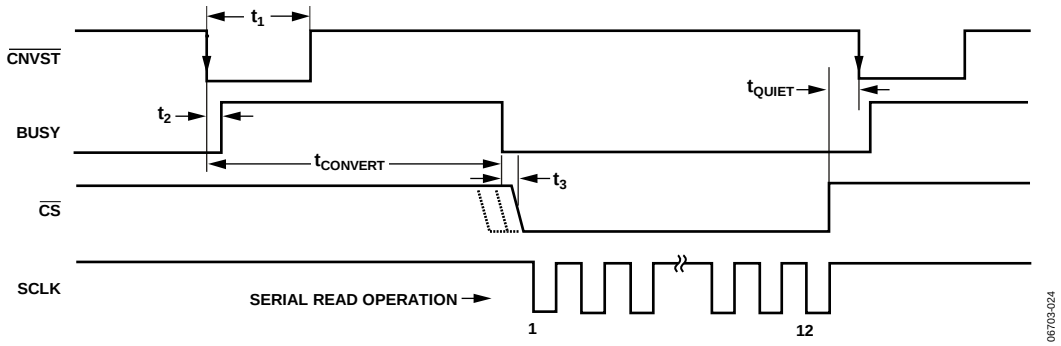


Figure 22. Normal Mode Operation for the AD7366

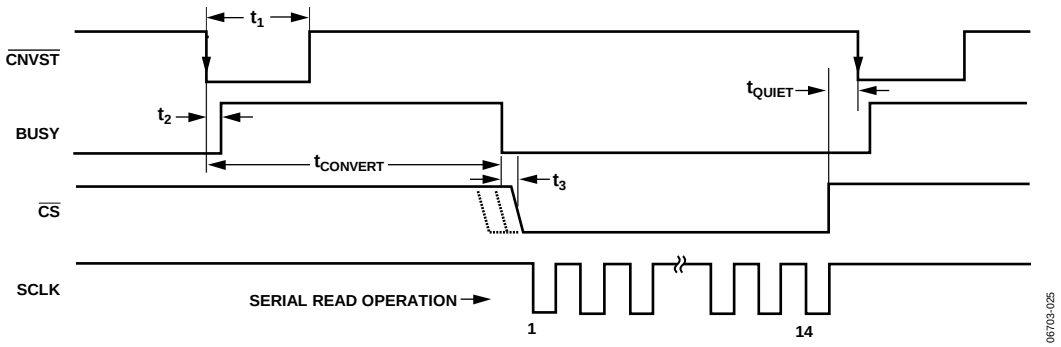


Figure 23. Normal Mode Operation for the AD7367

SHUTDOWN MODE

Shutdown mode is intended for use in applications where slow throughput rates are required. Shutdown mode is suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus, shutdown. When the AD7366/AD7367 are in full power-down, all analog circuitry is powered down. The falling edge of $\overline{\text{CNVST}}$ initiates the conversion. The BUSY output subsequently goes high to indicate that the conversion is in progress. After the conversion is completed, the BUSY output returns low. If the $\overline{\text{CNVST}}$ signal is at logic low when BUSY goes low, the part enters shutdown at the end of the conversion phase. While the part is in shutdown mode, the digital output code from the last conversion on each ADC can still be read from the D_{OUT} pins. To read the D_{OUT} data, $\overline{\text{CS}}$ must be brought low as described in the Serial Interface section. The D_{OUT} pins return to three-state when $\overline{\text{CS}}$ is brought back to logic high.

To exit full power-down and to power up the AD7366/AD7367, a rising edge of $\overline{\text{CNVST}}$ is required. After the required power-up time has elapsed, $\overline{\text{CNVST}}$ can be brought low again to initiate another conversion, as shown in Figure 24 (see the Power-Up Times section for power-up times associated with the AD7366/AD7367).

POWER-UP TIMES

The AD7366/AD7367 have one power-down mode, which is described in detail in the Shutdown Mode section. This section deals with the power-up time required when coming out of shutdown mode. It should be noted that the power-up times (as explained in this section) apply with the recommended capacitors in place on the $D_{CAP}A$ and $D_{CAP}B$ pins. To power up from shutdown, $\overline{\text{CNVST}}$ must be brought high and remain high for a minimum of 70 µs, as shown in Figure 24.

When power supplies are first applied to the AD7366/AD7367, the ADC can power up with $\overline{\text{CNVST}}$ in either the low or high logic state. Before attempting a valid conversion, $\overline{\text{CNVST}}$ must be brought high and remain high for the recommended power-up time of 70 µs. Then $\overline{\text{CNVST}}$ can be brought low to initiate a conversion. With the AD7366/AD7367, no dummy conversion is required before valid data can be read from the D_{OUT} pins. To place the part in shutdown mode when the supplies are first applied, the AD7366/AD7367 must be powered up and a conversion initiated. However, $\overline{\text{CNVST}}$ should remain in the logic low state so that when the BUSY signal goes low, the part enters shutdown.

When supplies are applied to the AD7366/AD7367, sufficient time must be allowed for any external reference to power up and to charge the various reference buffer decoupling capacitors to their final values.

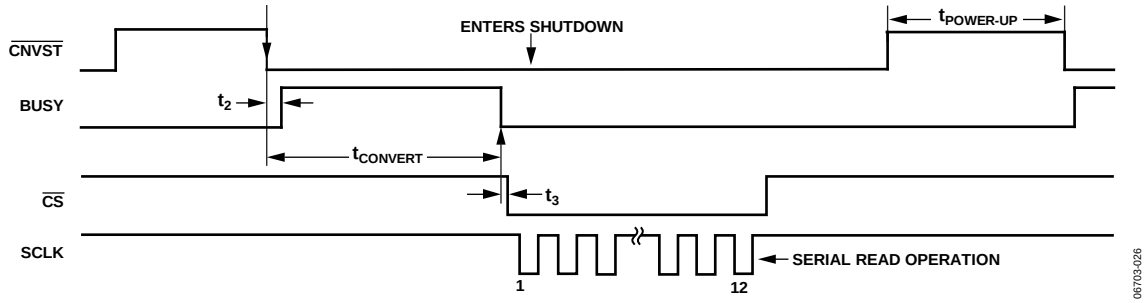


Figure 24. Autoshutdown Mode for the AD7366

SERIAL INTERFACE

Figure 25 and Figure 26 show the detailed timing diagram for serial interfacing to the AD7366 and the AD7367. On the falling edge of $\overline{\text{CNVST}}$, the AD7366/AD7367 simultaneously convert the selected channels. These conversions are performed using the on-chip oscillator. After the falling edge of $\overline{\text{CNVST}}$, the BUSY signal goes high, indicating that the conversion has started. The BUSY signal returns low when the conversion has been completed. The data can now be read from the D_{OUT} pins.

The $\overline{\text{CS}}$ and SCLK signals are required to transfer data from the AD7366/AD7367. The AD7366/AD7367 have two output pins corresponding to each ADC. Data can be read from the AD7366/AD7367 using both $D_{OUT}A$ and $D_{OUT}B$. Alternatively, a single output pin of the user's choice can be used. The SCLK input signal provides the clock source for the serial interface. The $\overline{\text{CS}}$ goes low to access data from the AD7366/AD7367. The falling edge of $\overline{\text{CS}}$ takes the bus out of three-state and clocks out the MSB of the conversion result. The data stream consists of 12 bits of data for the AD7366 and 14 bits of data for the AD7367, MSB first. The first bit of the conversion result is valid on the first SCLK falling edge after the $\overline{\text{CS}}$ falling edge. The subsequent 11/13 bits of data for the AD7366/AD7367, respectively, are clocked out on the falling edge of the SCLK signal. A minimum of 12 clock pulses must be provided to the AD7366 to access each conversion result, and a minimum of 14 clock pulses must be provided to the AD7367 to access the conversion result. Figure 25 shows how a 12 SCLK read is used to access the conversion results for the AD7366, and Figure 26 illustrates the case for the AD7367 with a 14 SCLK read.

On the rising edge of $\overline{\text{CS}}$ the conversion is terminated and $D_{OUT}A$ and $D_{OUT}B$ return to three-state. If $\overline{\text{CS}}$ is not brought high, but is instead held low for an additional 14 SCLK cycles the data from the other DOUT pin follows on the selected DOUT pin. Note, the second serial result from the AD7366 is preceeded by two zeros. See Figure 27 and Figure 28, where $D_{OUT}A$ is shown. In this case, the D_{OUT} line in use returns to three-state on the rising edge of $\overline{\text{CS}}$.

If the falling edge of SCLK coincides with the falling edge of $\overline{\text{CS}}$, the falling edge of SCLK is not acknowledged by the AD7366/AD7367, and the next falling edge of SCLK is the first one registered after the falling edge of $\overline{\text{CS}}$.

The $\overline{\text{CS}}$ pin can be brought low before the BUSY signal goes low, indicating the end of a conversion. When $\overline{\text{CS}}$ is at a logic low state, the data bus is brought out of three-state. This feature can be used to ensure that the MSB is valid on the falling edge of BUSY by bringing $\overline{\text{CS}}$ low a minimum of t_4 before the BUSY signal goes low. The dotted $\overline{\text{CS}}$ line in Figure 22 and Figure 23 illustrates this feature.

Alternatively, the $\overline{\text{CS}}$ pin can be tied to a low logic state continuously. In this case, the D_{OUT} pins never enter three-state and the data bus is continuously active. Under these conditions, the MSB of the conversion result for the AD7366/AD7367 is available on the falling edge of the BUSY signal. The next most significant bit is available on the first SCLK falling edge after the BUSY signal has gone low. This mode of operation enables the user to read the MSB as soon as it is made available by the converter.

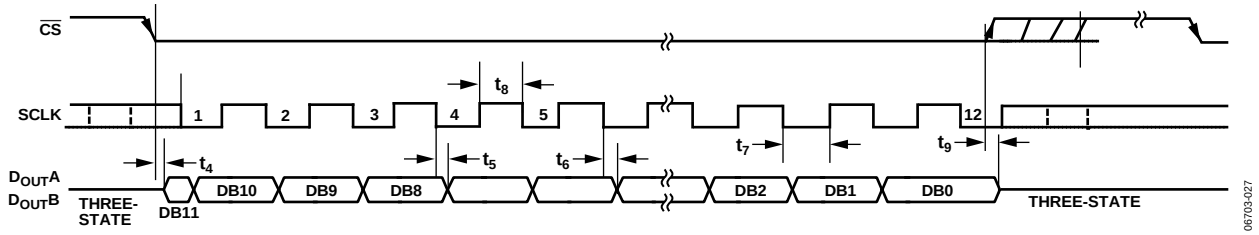


Figure 25. Serial Interface Timing Diagram for the AD7366

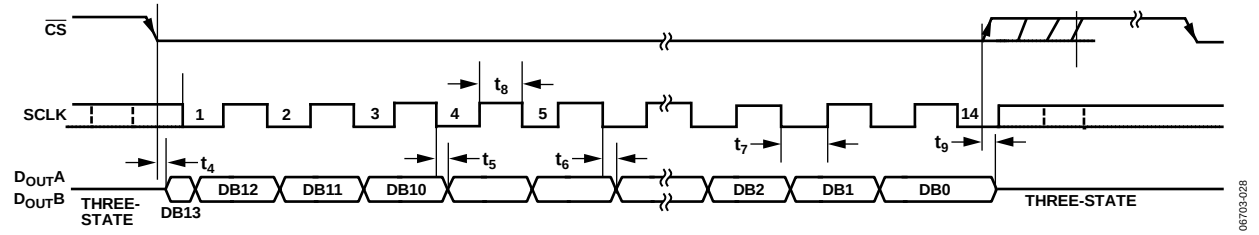


Figure 26. Serial Interface Timing Diagram for the AD7367

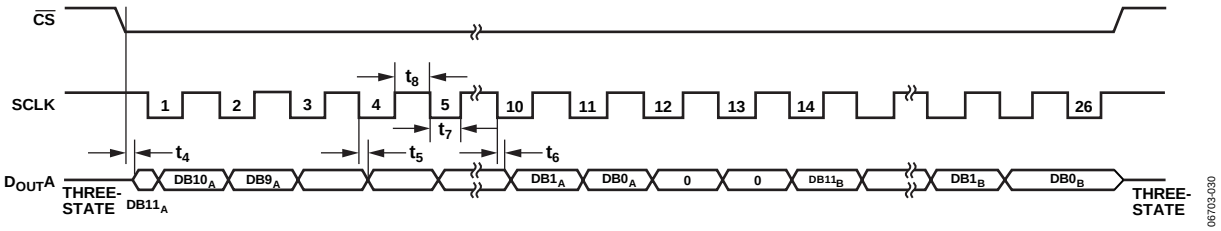


Figure 27. Reading Data from Both ADCs on One D_{OUT} Line with 26 SCLKs for the AD7366

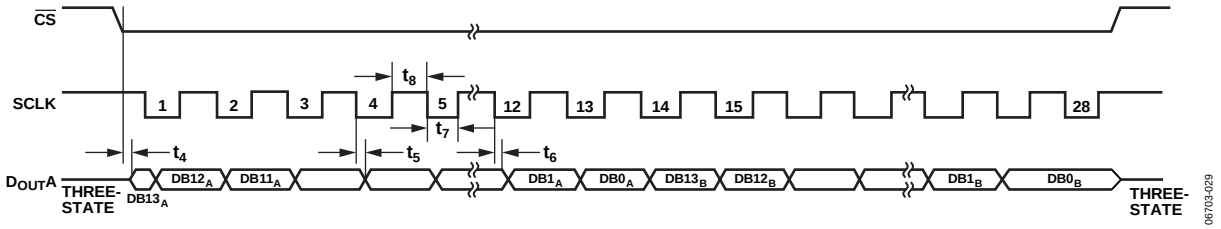


Figure 28. Reading Data from Both ADCs on One D_{OUT} Line with 28 SCLKs for the AD7367

MICROPROCESSOR INTERFACING

The serial interface on the AD7366/AD7367 allows the parts to be directly connected to a range of different microprocessors. This section explains how to interface the AD7366/AD7367 with some common microcontrollers and DSP serial interface protocols.

AD7366/AD7367 TO ADSP-218x

The ADSP-218x family of DSPs interfaces directly to the AD7366/AD7367 without any glue logic required. The V_{DRIVE} pin of the AD7366/AD7367 takes the same supply voltage as the power supply pin of the ADSP-218x. This allows the ADC to operate at a higher supply voltage than its serial interface and therefore, the ADSP-218x, if necessary. This example shows both $D_{OUT}A$ and $D_{OUT}B$ of the AD7366/AD7367 connected to both serial ports of the ADSP-218x. The SPORT0 and SPORT1 control registers should be set up as shown in Table 11 and Table 12.

Table 11. SPORT0 Control Register Setup

Setting	Description
TFSW = RFSW = 1	Alternate framing
INVRFS = INVTFS = 1	Active low frame signal
DTYPE = 00	Right-justify data
SLEN = 1111	16-bit data-word (or can be set to 1101 for 14-bit data-word)
ISCLK = 1	Internal serial clock
TFSR = RFSR = 1	Frame every word
IRFS = 0	
ITFS = 1	

Table 12. SPORT1 Control Register Setup

Setting	Description
TFSW = RFSW = 1	Alternate framing
INVRFS = INVTFS = 1	Active low frame signal
DTYPE = 00	Right-justify data
SLEN = 1111	16-bit data-word (or can be set to 1101 for 14-bit data-word)
ISCLK = 0	External serial clock
TFSR = RFSR = 1	Frame every word
IRFS = 0	
ITFS = 1	

The connection diagram is shown in Figure 29. The ADSP-218x has the TFS0 and RFS0 of the SPORT0 and the RFS1 of SPORT1 tied together. TFS0 is set as an output, and both RFS0 and RFS1 are set as inputs. The DSP operates in alternate framing mode, and the SPORT control register is set up as described in Table 11 and Table 12. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$.

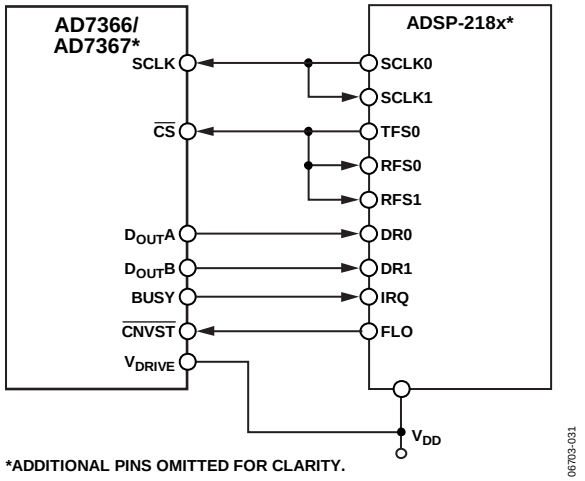


Figure 29. Interfacing the AD7366/AD7367 to the ADSP-218x

The AD7366/AD7367 BUSY line provides an interrupt to the ADSP-218x when the conversion is complete. The conversion results can then be read from the AD7366/AD7367 using a read operation. When an interrupt is received on IRQ from the BUSY signal, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and, therefore, the reading of data.

AD7366/AD7367 TO ADSP-BF53x

The ADSP-BF53x family of DSPs interfaces directly to the AD7366/AD7367 without any glue logic required. The availability of secondary receive registers on the serial ports of the Blackfin® DSPs means that only one serial port is necessary to read from both the $D_{OUT}A$ and $D_{OUT}B$ pins simultaneously. Figure 30 shows both $D_{OUT}A$ and $D_{OUT}B$ of the AD7366/AD7367 connected to Serial Port 0 of the ADSP-BF53x. The SPORT0 Receive Configuration 1 register and the SPORT0 Receive Configuration 2 register should be set up as outlined in Table 13 and Table 14.

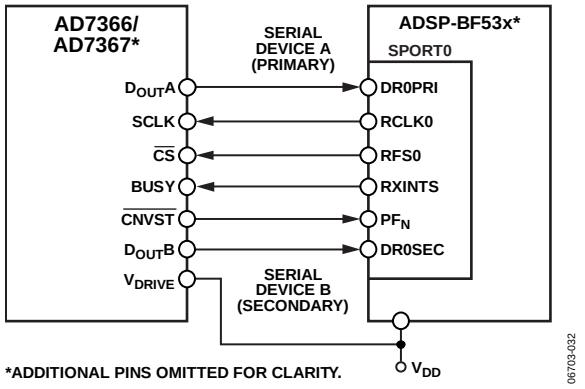


Figure 30. Interfacing the AD7366/AD7367 to the ADSP-BF53x

Table 13. SPORT0 Receive Configuration 1 Register (SPORT0_RCR1)

Setting	Description
RCKFE = 1	Sample data with falling edge of RSCLK
LRFS = 1	Active low frame signal
RFSR = 1	Frame every word
IRFS = 1	Internal RFS used
RLSBIT = 0	Receive MSB first
RDTYPE = 00	Zero fill
IRCLK = 1	Internal receive clock
RSPEN = 1	Receive enabled
SLEN = 1111	16-bit data-word (or can be set to 1101 for 14-bit data-word)
TFSR = RFSR = 1	

Table 14. SPORT0 Receive Configuration 2 Register (SPORT0_RCR2)

Setting	Description
RXSE = 1	Secondary side enabled
SLEN = 1111	16-bit data-word (or can be set to 1101 for 14-bit data-word)

AD7366/AD7367 TO TMS320VC5506

The serial interface on the TMS320VC5506 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices such as the AD7366/AD7367. The $\overline{CS}$ input allows easy interfacing between the TMS320VC5506 and the AD7366/AD7367 without any glue logic required. The serial ports of the TMS320VC5506 are set up to operate in burst mode with internal CLKX0 (Tx serial clock on Serial Port 0) and FSX0 (Tx frame sync from Serial Port 0). The serial port control (SPC) registers must be set up as shown in Table 15.

Table 15. Serial Port Control Register Setup

SPC	FO	FSM	MCM	TXM
SPC0	0	1	1	1
SPC1	0	1	0	0

The connection diagram is shown in Figure 31. The V_{DRIVE} pin of the AD7366/AD7367 takes the same supply voltage as the power supply pin of the TMS320VC5506. This allows the ADC to operate at a higher voltage than its serial interface and, therefore, the TMS320VC5506, if necessary.

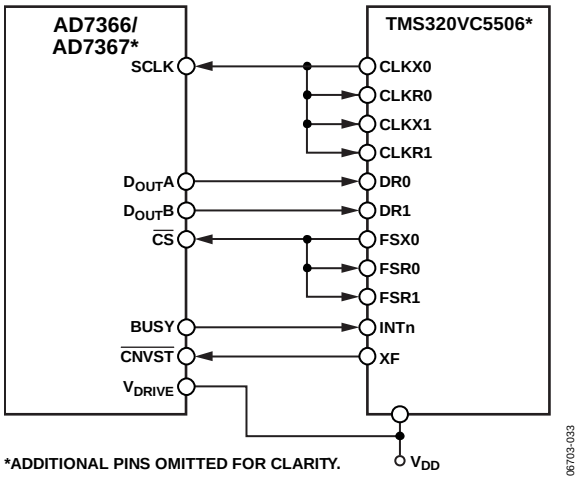


Figure 31. Interfacing the AD7366/AD7367 to the TMS320VC5506

As with the previous interfaces, conversion can be initiated from the TMS320VC5506 or from an external source, and the processor is interrupted when the conversion sequence is completed.

AD7366/AD7367 TO DSP563xx

The connection diagram in Figure 32 shows how the AD7366/AD7367 can be connected to the enhanced synchronous serial interface (ESSI) of the DSP563xx family of DSPs from Motorola. There are two on-board ESSIs, and each is operated in synchronous mode (Bit SYN = 1 in the CRB register) with internally generated word length frame sync for both Tx and Rx (Bit FSL1 = 0 and Bit FSL0 = 0 in the CRB register).

Normal operation of the ESSI is selected by setting MOD = 0 in the CRB register. Set the word length to 16 by setting Bit WL1 = 1 and Bit WL0 = 0 in the CRA register. The FSP bit in the CRB register should be set to 1 so that the frame sync is negative.

In the example shown in Figure 32, the serial clock is taken from the ESSI0, so the SCK0 pin must be set as an output (SCKD = 1) while the SCK1 pin is set as an input (SCKD = 0). The frame sync signal is taken from SC02 on ESSI0, so SCD2 = 1, while on ESSI1, SCD2 = 0; therefore, SC12 is configured as an input. The V_{DRIVE} pin of the AD7366/AD7367 takes the same supply voltage as the power supply pin of the DSP563xx. This allows the ADC to operate at a higher voltage than its serial interface and, therefore, the DSP563xx, if necessary.

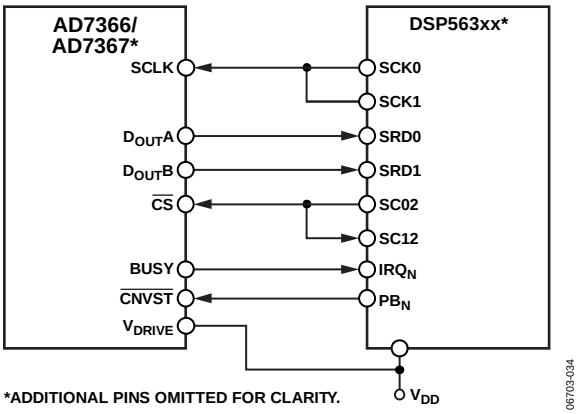


Figure 32. Interfacing the AD7366/AD7367 to the DSP563xx

APPLICATION HINTS

LAYOUT AND GROUNDING

The printed circuit board that houses the AD7366/AD7367 should be designed so that the analog and digital sections are confined to separate areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally the best option. All AGND pins on the AD7366/AD7367 should be connected to the AGND plane. Digital and analog ground pins should be joined in only one place. If the AD7366/AD7367 are in a system where multiple devices require an AGND and DGND connection, the connection should still be made at only one point. A star point should be established as close as possible to the ground pins on the AD7366/AD7367.

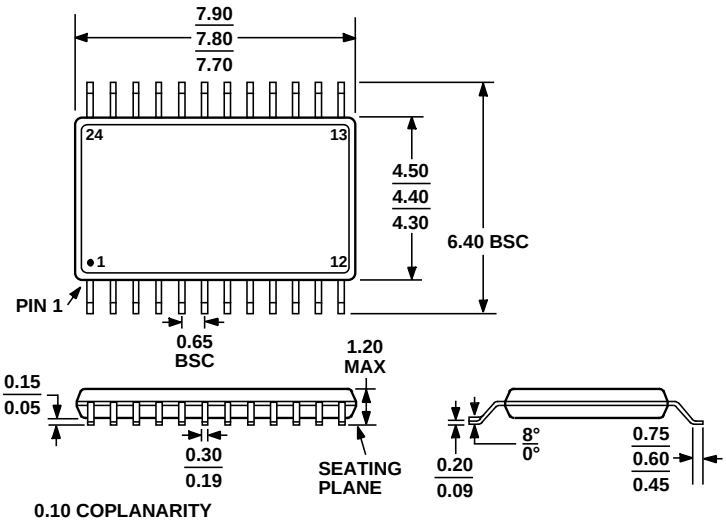
Good connections should be made to the power and ground planes. This can be done with a single via or multiple vias for each supply and ground pin.

Avoid running digital lines under the AD7366/AD7367 devices because this couples noise onto the die. However, the analog ground plane should be allowed to run under the AD7366/AD7367 to avoid noise coupling. The power supply lines to the AD7366/AD7367 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, components with fast switching signals, such as clocks, should be shielded with digital ground and should never be run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces should be run at right angles to each other. A microstrip technique is the best method, but its use may not be possible with a double-sided board. In the microstrip technique, the component side of the board is dedicated to ground planes, and signals are placed on the other side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to AGND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have a low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic and surface mount types of capacitors. These low ESR, low ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 33. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7366BRUZ	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7366BRUZ-RL7	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7366BRUZ-500RL7	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7367BRUZ	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7367BRUZ-500RL7	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7367BRUZ-RL7	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
EVAL-AD7366CBZ		Evaluation Board	
EVAL-AD7367CBZ		Evaluation Board	
EVAL-CONTROL BRD2		Control Board	

[1] Z = RoHS Compliant Part.

D06703-0-11/10(D)