# AD7298* Product Page Quick Links

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- UG-254: Evaluation Board for the AD7298 8-Channel, 1 MSPS, 12-Bit SAR ADC with Temperature Sensor

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- MS-2210: Designing Power Supplies for High Speed ADC

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- Integrated SAR ADC Family in 4mm x 4mm Package
- MT-002: What the Nyquist Criterion Means to Your Sampled Data System Design
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## REVISION HISTORY

**6/11—Rev. A to Rev. B**

Changes to Internal Temperature Sensor, Accuracy Parameter in Table 1 ... 3

**1/11—Rev. 0 to Rev. A**

Removed Input Impedance Parameter ... 3
Added Input Capacitance Parameter of 8 pF ... 3
Changes to Figure 11 ... 10
Changed C1 Value to 8 pF in Analog Input Section ... 13
Changes to Figure 23 ... 14
Changes to Ordering Guide ... 24

**9/10—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 2.8 V to 3.6 V; $V_{DRIVE}$ = 1.65 V to 3.6 V; $f_{SAMPLE}$ = 1 MSPS, $f_{SCLK}$ = 20 MHz, $V_{REF}$ = 2.5 V internal; $T_A$ = −40°C to +125°C, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | $f_{IN}$ = 50 kHz sine wave |
| Signal-to-Noise Ratio (SNR)[1, 2] | 70 | 72 | | dB | |
| Signal-to-Noise (and Distortion) Ratio (SINAD)[1] | 70 | 71 | | dB | |
| Total Harmonic Distortion (THD)[1] | | −82 | −77 | dB | |
| Spurious-Free Dynamic Range (SFDR) | | −84 | −77.5 | dB | |
| Intermodulation Distortion (IMD) | | | | | $f_A$ = 40.1 kHz, $f_B$ = 41.5 kHz |
| Second-Order Terms | | −84 | | dB | |
| Third-Order Terms | | −93 | | dB | |
| Channel-to-Channel Isolation | | −100 | | dB | $f_{IN}$ = 50 kHz, $f_{NOISE}$ = 60 kHz |
| SAMPLE AND HOLD | | | | | |
| Aperture Delay[3] | | | 12 | ns | |
| Aperture Jitter[3] | | 40 | | ps | |
| Full Power Bandwidth | | 30 | | MHz | @ 3 dB |
| | | 10 | | MHz | @ 0.1 dB |
| DC ACCURACY | | | | | |
| Resolution | 12 | | | Bits | |
| Integral Nonlinearity (INL)[1] | | ±0.5 | ±1 | LSB | |
| Differential Nonlinearity (DNL)[1] | | ±0.5 | ±0.99 | LSB | Guaranteed no missed codes to 12 bits |
| Offset Error[1] | | ±2 | ±4.5 | LSB | |
| Offset Error Matching[1] | | ±2.5 | ±4.5 | LSB | |
| Offset Temperature Drift | | 4 | | ppm/°C | |
| Gain Error[1] | | ±1 | ±4 | LSB | |
| Gain Error Matching[1] | | ±1 | ±2.5 | LSB | |
| Gain Temperature Drift | | 0.5 | | ppm/°C | |
| ANALOG INPUT | | | | | |
| Input Voltage Ranges | 0 | | $V_{REF}$ | V | |
| DC Leakage Current | | ±0.01 | ±1 | µA | |
| Input Capacitance | | 32 | | pF | When in track |
| | | 8 | | pF | When in hold mode |
| REFERENCE INPUT/OUTPUT | | | | | |
| Reference Output Voltage[4] | 2.4925 | 2.5 | 2.5075 | V | ±0.3% maximum @ 25°C |
| Long-Term Stability | | 150 | | ppm | For 1000 hours |
| Output Voltage Hysteresis | | 50 | | ppm | |
| Reference Input Voltage Range[5] | 1 | | 2.5 | V | |
| DC Leakage Current | | ±0.01 | ±1 | µA | External reference applied to Pin $V_{REF}$ |
| $V_{REF}$ Output Impedance | | 1 | | Ω | |
| $V_{REF}$ Temperature Coefficient | | 12 | 35 | ppm/°C | |
| $V_{REF}$ Noise | | 60 | | µV rms | Bandwidth = 10 MHz |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | $0.7 \times V_{DRIVE}$ | | | V | |
| Input Low Voltage, $V_{INL}$ | | | $+0.3 \times V_{DRIVE}$ | V | |
| Input Current, $I_{IN}$ | | ±0.01 | ±1 | µA | $V_{IN}$ = 0 V or $V_{DRIVE}$ |
| Input Capacitance, $C_{IN}$[3] | | 3 | | pF | |
| LOGIC OUTPUTS | | | | | |
| Output High Voltage, $V_{OH}$ | $V_{DRIVE} - 0.3$ | | | V | $V_{DRIVE} < 1.8$ |
| | $V_{DRIVE} - 0.2$ | | | V | $V_{DRIVE} \geq 1.8$ |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | |
| Floating State Leakage Current | | ±0.01 | ±1 | µA | |
| Floating State Output Capacitance[3] | | 8 | | pF | |
| INTERNAL TEMPERATURE SENSOR | | | | | |
| Operating Range | −40 | | +125 | | |
| Accuracy | | ±1 | ±2 | °C | $T_A$ = −40°C to +85°C |
| | | ±1 | ±3 | °C | $T_A$ = +85°C to +125°C |
| Resolution | | 0.25 | | °C | LSB size |
| CONVERSION RATE | | | | | |
| Conversion Time | | 1 | $t_2 + 16 \times t_{SCLK}$ | µs | For $V_{IN0}$ to $V_{IN7}$, with one cycle latency |
| | | | 100 | µs | $T_{SENSE}$ temperature sensor channel |
| Track-and-Hold Acquisition Time[3] | | | 100 | ns | Full-scale step input |
| Throughput Rate | | | 1 | MSPS | $f_{SCLK}$ = 20 MHz, for analog voltage conversions, one cycle latency |
| | | | 10 | KSPS | For the $T_{SENSE}$ channel, one cycle latency |
| POWER REQUIREMENTS | | | | | Digital inputs = 0 V or $V_{DRIVE}$ |
| $V_{DD}$ | 2.8 | 3 | 3.6 | V | |
| $V_{DRIVE}$ | 1.65 | 3 | 3.6 | V | |
| $I_{TOTAL}$[6] | | | | | $V_{DD}$ = 3.6 V, $V_{DRIVE}$ = 3.6 V |
| Normal Mode (Operational) | | 5.8 | 6.3 | mA | |
| Normal Mode (Static) | | 4.1 | 4.6 | mA | |
| Partial Power-Down Mode | | 2.7 | 3.3 | mA | |
| Full Power-Down Mode | | 1 | 1.6 | µA | $T_A$ = −40°C to +25°C |
| | | | 10 | µA | $T_A$ = −40°C to +125°C |
| Power Dissipation[7] | | | | | |
| Normal Mode (Operational) | | 17.4 | 18.9 | mW | $V_{DD}$ = 3 V, $V_{DRIVE}$ = 3 V |
| | | | 22.7 | mW | |
| Normal Mode (Static) | | 14.8 | 16.6 | mW | |
| Partial Power-Down Mode | | 9.8 | 11.9 | mW | |
| Full Power-Down Mode | | 3.6 | 5.8 | µW | $T_A$ = −40°C to +25°C |
| | | | 36 | µW | $T_A$ = −40°C to +125°C |

[1] See the Terminology section.
[2] All specifications expressed in decibels are referred to full-scale input, FSR, and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[3] Sample tested during initial release to ensure compliance.
[4] Refers to Pin $V_{REF}$ specified for 25°C.
[5] A correction factor may be required on the temperature sensor results when using an external $V_{REF}$ (see the Temperature Sensor Averaging section).
[6] $I_{TOTAL}$ is the total current flowing in $V_{DD}$ and $V_{DRIVE}$.
[7] Power dissipation is specified with $V_{DD}$ = $V_{DRIVE}$ = 3.6 V, unless otherwise noted.

## TIMING SPECIFICATIONS

$V_{DD}$ = 2.8 V to 3.6 V; $V_{DRIVE}$ = 1.65 V to 3.6 V; $V_{REF}$ = 2.5 V internal; $T_A$ = −40°C to + 125°C, unless otherwise noted. Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DRIVE}$) and timed from a voltage level of 1.6 V.

**Table 2.**

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Test Conditions/Comments |
|---|---|---|---|
| $t_{CONVERT}$ | $t_2 + (16 \times t_{SCLK})$ | µs max | Conversion time |
| | 820 | ns typ | Each ADC channel $V_{IN0}$ to $V_{IN7}$, $f_{SCLK}$ = 20 MHz |
| | 100 | µs max | Temperature sensor channel |
| $f_{SCLK}$[1] | 50 | kHz min | Frequency of external serial clock |
| | 20 | MHz max | Frequency of external serial clock |
| $t_{QUIET}$ | 6 | ns min | Minimum quiet time required between the end of serial read and the start of the next voltage conversion in repeat and nonrepeat mode. |
| $t_2$ | 10 | ns min | $\overline{CS}$ to SCLK setup time |
| $t_3$[1] | 15 | ns max | Delay from CS (falling edge) until DOUT three-state disabled |
| $t_4$[1] | | | Data access time after SCLK falling edge |
| | 35 | ns max | $V_{DRIVE}$ = 1.65 V to 3 V |
| | 28 | ns max | $V_{DRIVE}$ = 3 V to 3.6 V |
| $t_5$ | $0.4 \times t_{SCLK}$ | ns min | SCLK low pulse width |
| $t_6$ | $0.4 \times t_{SCLK}$ | ns min | SCLK high pulse width |
| $t_7$[1] | 14 | ns min | SCLK to DOUT valid hold time |
| $t_8$[1] | 16/34 | ns min/max | SCLK falling edge to DOUT high impedance |
| $t_9$ | 5 | ns min | DIN setup time prior to SCLK falling edge |
| $t_{10}$ | 4 | ns min | DIN hold time after SCLK falling edge |
| $t_{11}$ | 100 | ns min | $T_{SENSE}$_BUSY falling edge to $\overline{CS}$ falling edge |
| $t_{12}$[1] | 30 | ns max | Delay from $\overline{CS}$ rising edge to DOUT high impedance |
| $t_{POWER-UP\_PARTIAL}$ | 1 | µs max | Power-up time from partial power-down |
| $t_{POWER-UP}$ | 6 | ms max | Internal reference power-up time from full power-down |

[1] Measured with a load capacitance on DOUT of 15 pF.

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND, GND1 | −0.3 V to +5 V |
| $V_{DRIVE}$ to GND, GND1 | −0.3 V to + 5 V |
| Analog Input Voltage to GND1 | −0.3 V to 3 V |
| Digital Input Voltage to GND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| $V_{REF}$ to GND1 | −0.3 V to +3 V |
| GND1 to GND | −0.3 V to +0.3 V |
| Input Current to Any Pin Except Supplies | ±10 mA |
| Operating Temperature Range | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| Pb-Free Temperature, Soldering Reflow | 260(+0)°C |
| ESD | 3.5 kV |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## THERMAL RESISTANCE

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 20-Lead LFCSP | 52 | 6.5 | °C/W |

# PIN CONFIGURATION AND FUNCTION DESCRIPTION

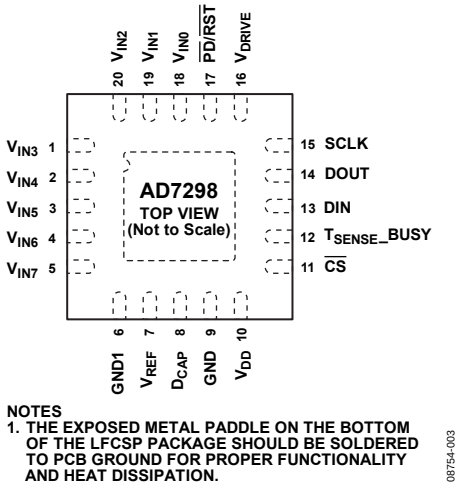



*Figure 2. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 to 5, 18 to 20 | $V_{IN3}$, $V_{IN4}$, $V_{IN5}$, $V_{IN6}$, $V_{IN7}$, $V_{IN0}$, $V_{IN1}$, $V_{IN2}$ | Analog Inputs. The AD7298 has eight single-ended analog inputs that are multiplexed into the on-chip track-and-hold. Each input channel can accept analog inputs from 0 V to 2.5 V. Any unused input channels should be connected to GND1 to avoid noise pickup. |
| 6 | GND1 | Ground. Ground reference point for the internal reference circuitry on the AD7298. The external reference signals and all analog input signals should be referred to this GND1 voltage. The GND1 pin should be connected to the GND plane of a system. All ground pins should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. The $V_{REF}$ pin should be decoupled to this ground pin via a 10 µF decoupling capacitor. |
| 7 | $V_{REF}$ | Internal Reference/External Reference Supply. The nominal internal reference voltage of 2.5 V appears at this pin. Provided the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. Decoupling capacitors should be connected to this pin to decouple the reference buffer. For best performance, it is recommended to use a 10 µF decoupling capacitor on this pin to GND1. The internal reference can be disabled and an external reference supplied to this pin, if required. The input voltage range for the external reference is 2.0 V to 2.5 V. |
| 8 | $D_{CAP}$ | Decoupling Capacitor Pin. Decoupling capacitors (1 µF recommended) are connected to this pin to decouple the internal LDO. |
| 9 | GND | Ground. Ground reference point for all analog and digital circuitry on the AD7298. The GND pin should be connected to the ground plane of the system. All ground pins should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. Both $D_{CAP}$ and $V_{DD}$ pins should be decoupled to this GND pin. |
| 10 | $V_{DD}$ | Supply Voltage, 2.8 V to 3.6 V. This supply should be decoupled to GND with 10 µF and 100 nF decoupling capacitors. |
| 11 | $\overline{CS}$ | Chip Select, Active Low Logic Input. This pin is edge triggered on the falling edge of this input, the track-and-hold goes into hold mode, and a conversion is initiated. This input also frames the serial data transfer. When $\overline{CS}$ is low, the output bus is enabled, and the conversion result becomes available on the DOUT output. |
| 12 | $T_{SENSE}$_BUSY | Busy Output. This pin transitions high when a temperature sensor conversion starts and remains high until the conversion completes. |
| 13 | DIN | Data In, Logic input. Data to be written to the AD7298 control register is provided on this input and is clocked into the register on the falling edge of SCLK. |
| 14 | DOUT | Serial Data Output. The conversion result from the AD7298 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7298 consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data (MSB first). The output coding is straight binary for the voltage channels and twos complement for the temperature sensor result. |
| 15 | SCLK | Serial Clock, Logic Input. A serial clock input provides the SCLK for accessing the data from the AD7298. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 16 | $V_{DRIVE}$ | Logic Power Supply Input. The voltage supplied at this pin determines at the voltage at which the interface operates. This pin should be decoupled to GND. The voltage range on this pin is 1.65 V to 3.6 V and may be less than the voltage at $V_{DD}$, but should never exceed it by more than 0.3 V. |
| 17 | $\overline{PD}/\overline{RST}$ | Power-Down Pin. This pin places the part into full power-down mode and enables power conservation when operation is not required. This pin can be used to reset the device by toggling the pin low for a minimum of 1 ns and a maximum of 100 ns. If the maximum time is exceeded, the part enters power-down mode. When placing the AD7298 in full power-down mode, the analog inputs must return to 0 V. |
| EPAD | EPAD | The exposed metal paddle on the bottom of the LFCSP package should be soldered to PCB ground for proper functionality and heat dissipation. |

# TYPICAL PERFORMANCE CHARACTERISTICS

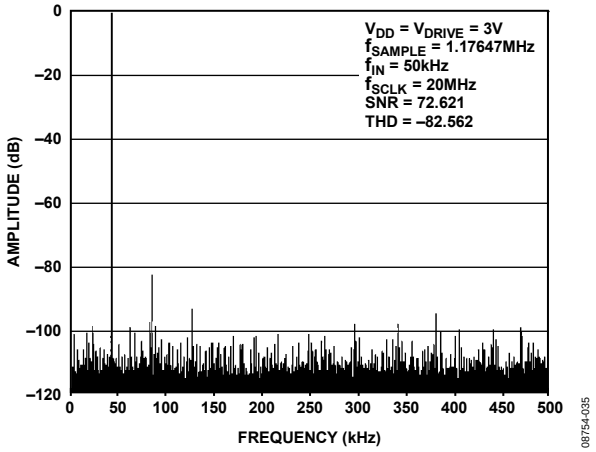



*Figure 3.Typical FFT*

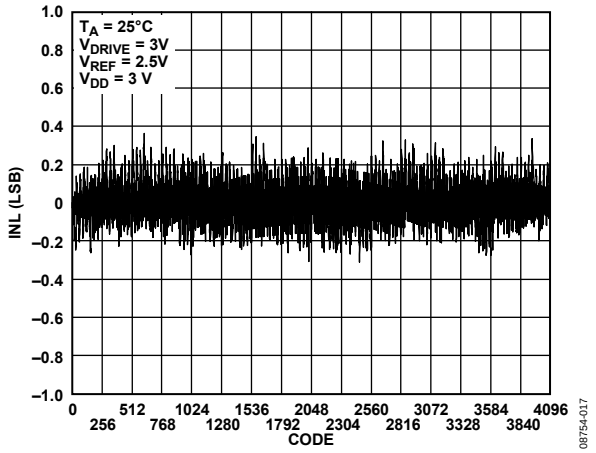



*Figure 4.Typical ADC INL*

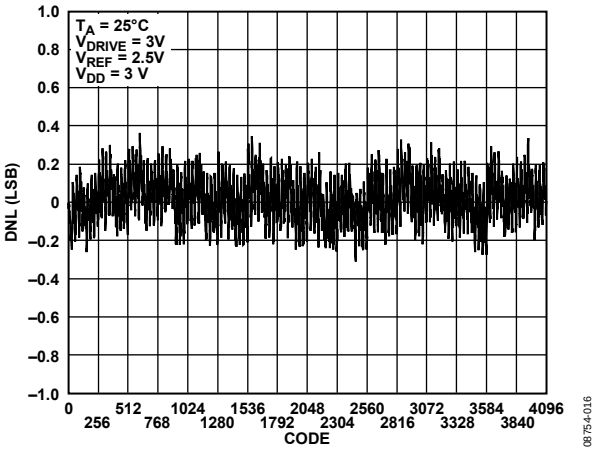



*Figure 5. Typical ADC DNL*

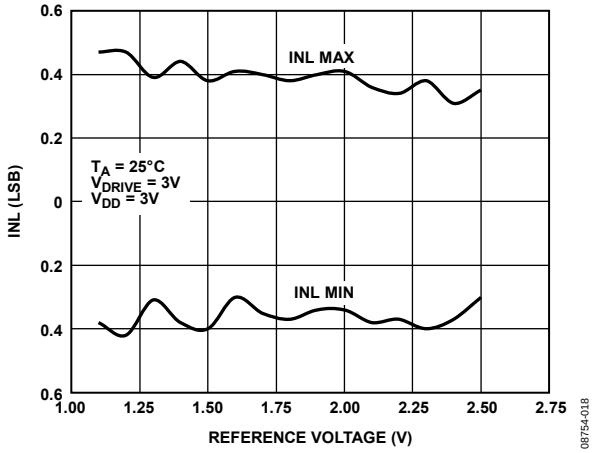



*Figure 6. INL vs. $V_{REF}$*

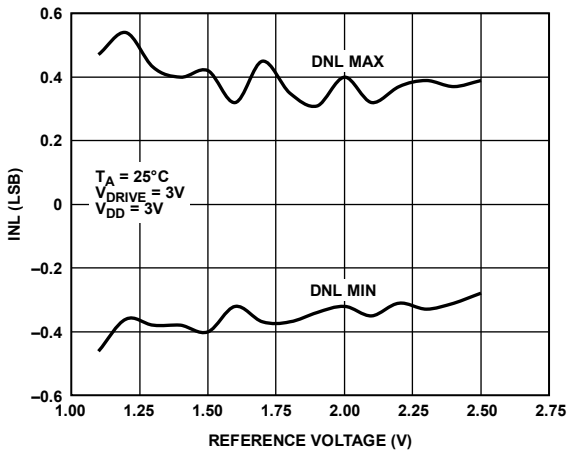



*Figure 7. DNL vs. $V_{REF}$*

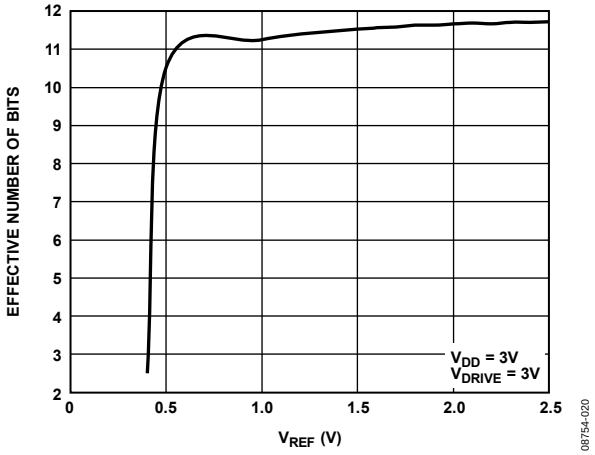



*Figure 8. Effective Number of Bits vs. $V_{REF}$*

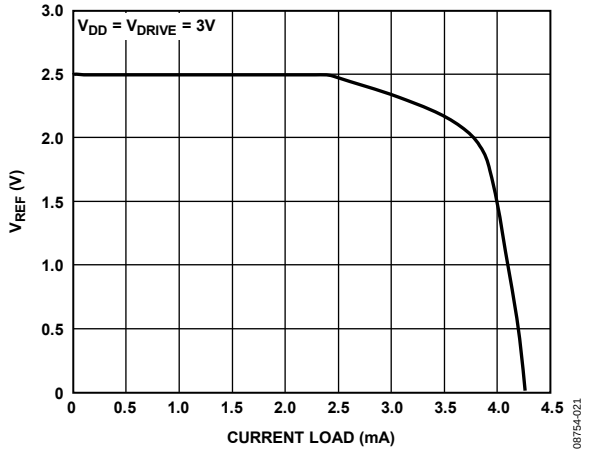



Figure 9. $V_{REF}$ vs. Reference Output Current Drive

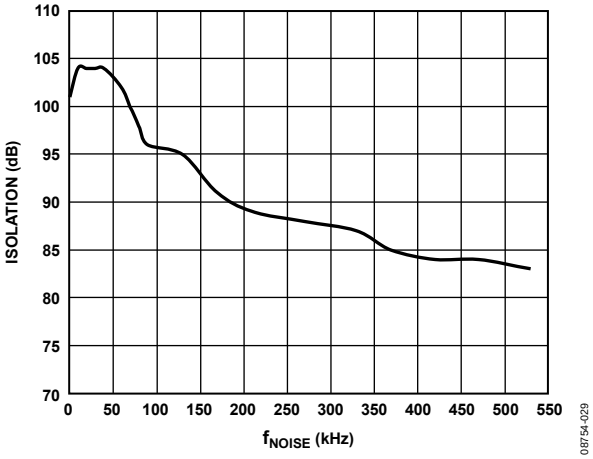



Figure 12. Channel-to-Channel Isolation, $f_{IN}$ = 50 kHz

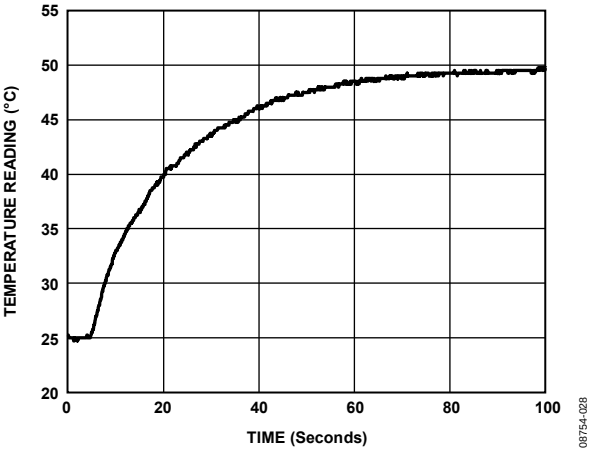



Figure 10. Response to Thermal Shock from Room Temperature into 50°C Stirred Oil

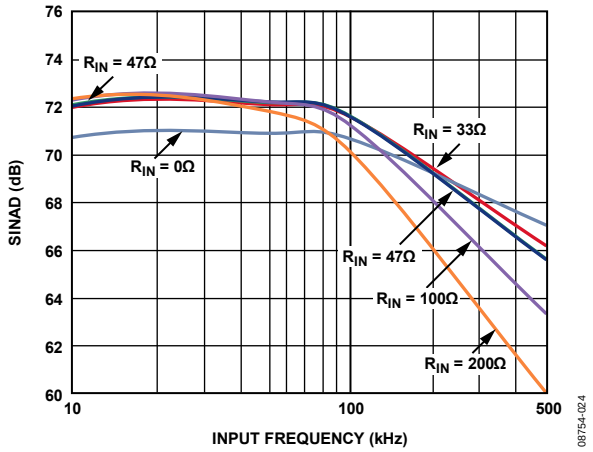



Figure 13. SINAD vs. Analog Input Frequency for Various Source Impedances

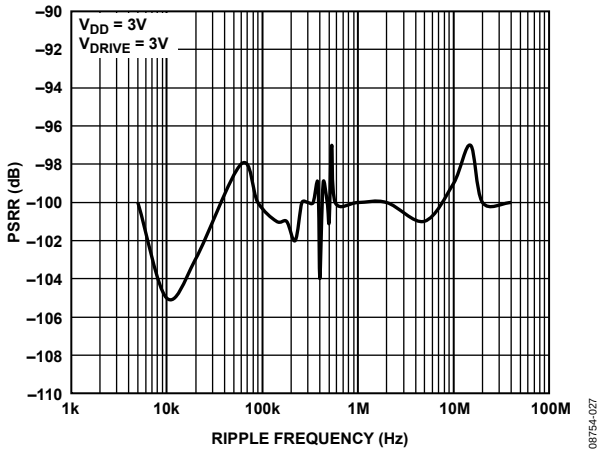



Figure 11. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

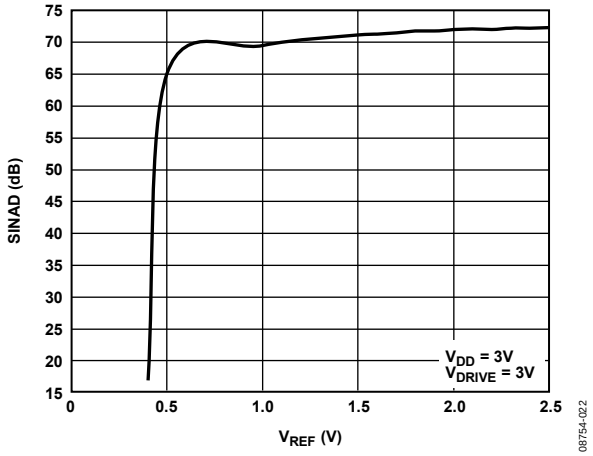



Figure 14. SINAD vs. Reference Voltage

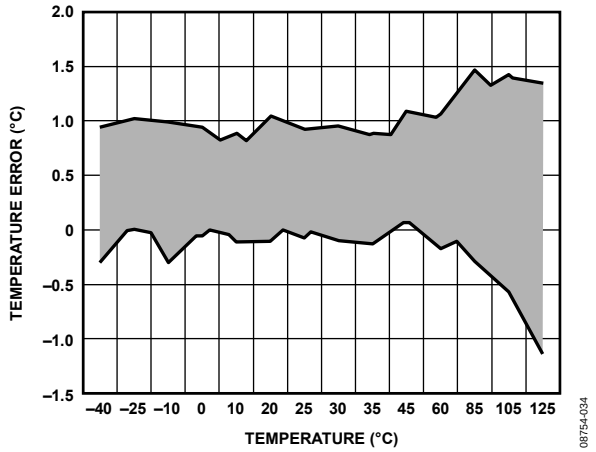



Figure 15. Temperature Accuracy at 3 V

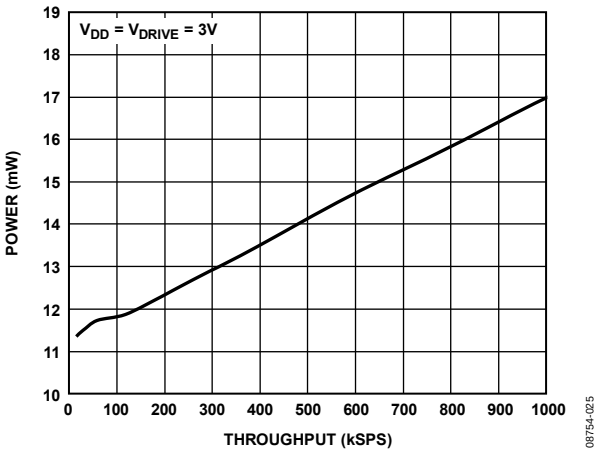



Figure 18. Power vs. Throughput in Normal Mode with $V_{DD}$ = 3 V

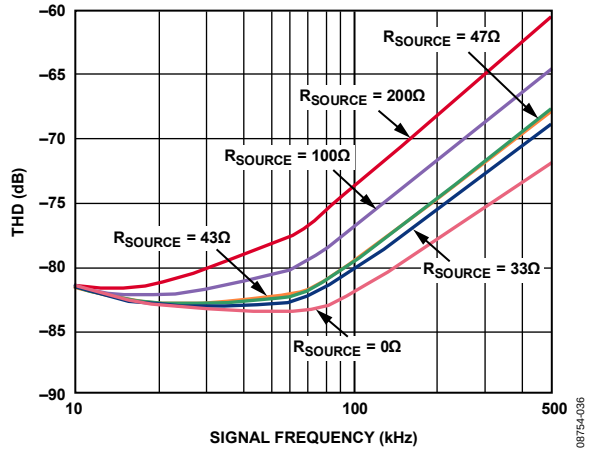



Figure 16. THD vs. Analog Input Frequency for Various Source Impedances

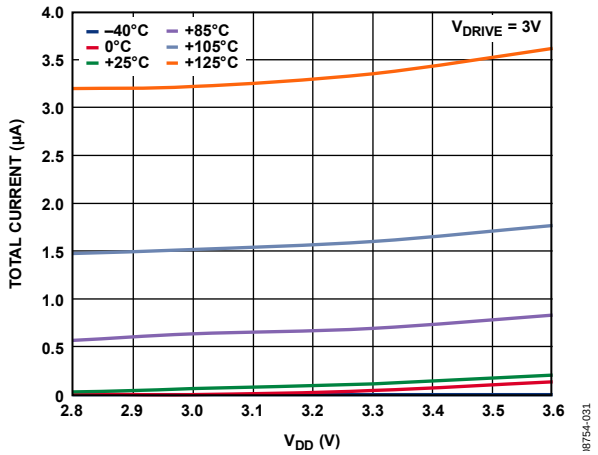



Figure 19. Full Shutdown Current vs. Supply Voltage for Various Temperatures

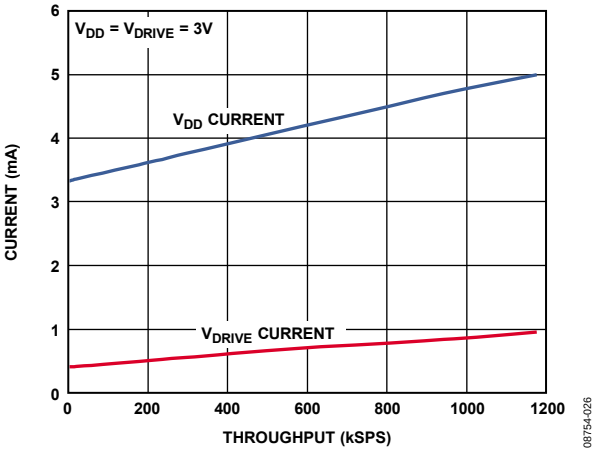



Figure 17. Average Supply Current vs. Throughput Rate

# TERMINOLOGY

**Signal-to-Noise and Distortion Ratio (SINAD)**
The measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise and distortion ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus, the SINAD is 74 dB for an ideal 12-bit converter.

**Total Harmonic Distortion (THD)**
The ratio of the rms sum of harmonics to the fundamental. For the AD7298, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where $V_1$ is the rms amplitude of the fundamental, and $V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second through sixth harmonics.

**Peak Harmonic or Spurious Noise**
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Typically, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

**Integral Nonlinearity**
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

**Differential Nonlinearity**
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Offset Error**
The deviation of the first code transition (00…000) to (00…001) from the ideal—that is, GND1 + 1 LSB.

**Offset Error Match**
The difference in offset error between any two channels.

**Gain Error**
The deviation of the last code transition (111…110) to (111…111) from the ideal (that is, $REF_{IN}$ − 1 LSB) after the offset error has been adjusted out.

**Gain Error Matching**
The difference in gain error between any two channels.

**Track-and-Hold Acquisition Time**

The track-and-hold amplifier returns to track mode at the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of conversion.

**Power Supply Rejection Ratio (PSRR)**
PSRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC $V_{DD}$ supply of frequency, $f_S$. The frequency of the input varies from 5 kHz to 25 MHz.

$$PSRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
*Pf* is the power at frequency, f, in the ADC output.
$Pf_S$ is the power at frequency, $f_S$, in the ADC output.

# CIRCUIT INFORMATION

The AD7298 is a high speed, 8-channel, 12-bit ADC with an internal temperature sensor. The part can be operated from a 2.8 V to 3.6 V supply and is capable of throughput rates of 1 MSPS per analog input channel.

The AD7298 provides the user with an on-chip, track-and-hold ADC and a serial interface housed in a 20-lead LFCSP. The AD7298 has eight single-ended input channels with channel repeat functionality, which allows the user to select a channel sequence through which the ADC can cycle with each consecutive $\overline{CS}$ falling edge. The serial clock input accesses data from the part, controls the transfer of data written to the ADC, and provides the clock source for the successive approximation ADC. The analog input range for the AD7928 is 0 V to $V_{REF}$. The AD7298 operates with one cycle latency, which means that the conversion result is available in the serial transfer following the cycle in which the conversion is performed.

The AD7298 includes a high accuracy band gap temperature sensor, which is monitored and digitized by the 12-bit ADC to give a resolution of 0.25°C. The AD7298 provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the partial power-down bit, PPD, in the control register and using the $\overline{PD}/\overline{RST}$ pin.

## CONVERTER OPERATION

The AD7298 is a 12-bit successive approximation ADC based around a capacitive DAC. Figure 20 and Figure 21 show simplified schematics of the ADC. The ADC is comprised of control logic, SAR, and a capacitive DAC that are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 20 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected $V_{IN}$ channel.

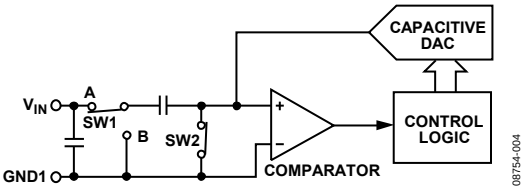



*Figure 20. ADC Acquisition Phase*

When the ADC starts a conversion (see Figure 21), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 23 shows the ADC's transfer functions.

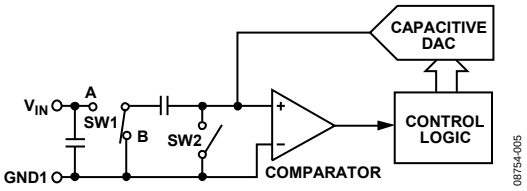



*Figure 21. ADC Conversion Phase*

## ANALOG INPUT

Figure 22 shows an equivalent circuit of the analog input structure of the AD7298. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the internally generated LDO voltage of 2.5 V ($D_{CAP}$) by more than 300 mV. This causes the diodes to become forward-biased and start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 10 mA. Capacitor C1, in Figure 22, is typically about 8 pF and can primarily be attributed to pin capacitance. The Resistor R1 is a lumped component made up of the on resistance of a switch (track-and-hold switch) and also includes the on resistance of the input multiplexer. The total resistance is typically about 155 Ω. The capacitor, C2, is the ADC sampling capacitor and has a capacitance of 34 pF typically.

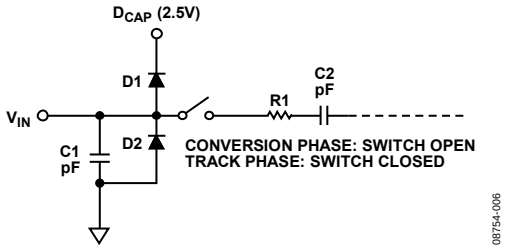



*Figure 22. Equivalent Analog Input Circuit*

For ac applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratios are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application performance criteria.

### *ADC Transfer Function*

The output coding of the AD7298 is straight binary for the analog input channel conversion results and twos complement, for the temperature conversion result. The designed code transitions occur at successive LSB values (that is, 1 LSB, 2 LSBs, and so forth). The LSB size is $V_{REF}/4096$ for the AD7298. The ideal transfer characteristic for the AD7298 for straight binary coding is shown in Figure 23.

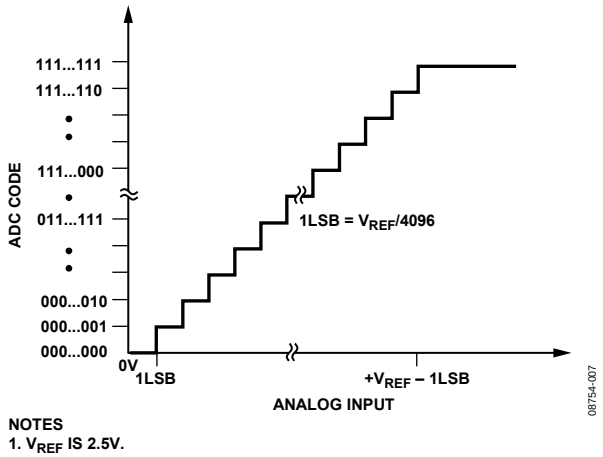



*Figure 23. Straight Binary Transfer Characteristic*

## TEMPERATURE SENSOR OPERATION

The AD7298 contains one local temperature sensor. The on-chip, band gap temperature sensor measures the temperature of the AD7298 die.

The temperature sensor module on the AD7298 is based on the three-current principle (see Figure 24), where three currents are passed through a diode and the forward voltage drop is measured, allowing the temperature to be calculated free of errors caused by series resistance.

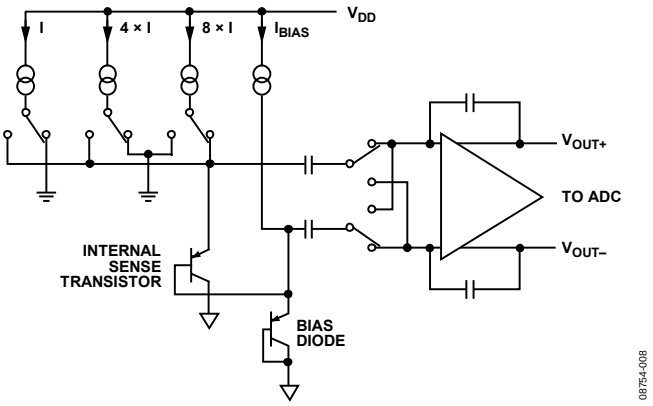



*Figure 24. Top-Level Structure of Internal Temperature Sensor*

The temperature conversion consists of two phases, the integration followed by the conversion. The integration is initiated on the $\overline{CS}$ falling edge. It takes a period of approximately 100 µs to complete the integration and conversion of the temperature result. When the integration is completed, the conversion is initiated automatically. Once the temperature integration is initiated, the $T_{SENSE}$_BUSY signal goes high to indicate that a temperature conversion is in progress and remains high until the conversion is completed.

Theoretically, the temperature measuring circuit can measure temperatures from −512°C to +511°C with a resolution of 0.25°C. However, temperatures outside $T_A$ (the specified temperature range for the AD7298) are outside the guaranteed operating temperature range of the device. The temperature sensor is selected by setting the $T_{SENSE}$ bit in the control register.

## TEMPERATURE SENSOR AVERAGING

The AD7298 incorporates a temperature sensor averaging feature to enhance the accuracy of the temperature measurements. To enable the temperature sensor averaging feature, both the $T_{SENSE}$AVG bit and the $T_{SENSE}$ bit must be enabled in the control register. In this mode the temperature is internally averaged to reduce the effect of noise on the temperature result. The temperature is measured each time a $T_{SENSE}$ conversion is performed and a moving average method is used to determine the result in the $T_{SENSE}$ Result Register. The average result is given by the following equation:

$$T_{SENSE}AVG = \frac{7}{8}(Previous\_Average\_Result) + \frac{1}{8}(Current\_Result)$$

The $T_{SENSE}$ result read when averaging is enabled is the $T_{SENSE}$AVG result, a moving average temperature measurement.

The first $T_{SENSE}$ conversion result given by the AD7298 after the temperature sensor and averaging mode has been selected in the control register (Bit D1 and Bit D5) is the actual first $T_{SENSE}$ conversion result. If the control register is written to and the content of the $T_{SENSE}$AVG bit changed, the averaging function is reset and the next $T_{SENSE}$ average conversion result is the current temperature conversion result. If the status of the $T_{SENSE}$AVG bit is not changed on successive writes to the control register, the averaging function is reinitialized and continues calculating the cumulative average.

The user has the option of disabling the averaging by setting Bit $T_{SENSE}$AVG to 0 in the control register. The AD7298 defaults on power-up with the averaging function disabled. The total time to measure a temperature channel is typically 100 µs.

### *Temperature Value Format*

One LSB of the ADC corresponds to 0.25°C. The temperature reading from the ADC is stored in a 12-bit twos complement format to accommodate both positive and negative temperature measurements. The temperature data format is provided in Table 6.

**Table 6. Temperature Data Format**

| Temperature (°C) | Digital Output |
|---|---|
| −40 | 1111 0110 0000 |
| −25 | 1111 1001 1100 |
| −10 | 1111 1101 1000 |
| −0.25 | 1111 1111 1111 |
| 0 | 0000 0000 0000 |
| +0.25 | 0000 0000 0001 |
| +10 | 0000 0010 1000 |
| +25 | 0000 0110 0100 |
| +50 | 0000 1100 1000 |
| +75 | 0001 0010 1100 |
| +100 | 0001 1001 0000 |
| +105 | 0001 1010 0100 |
| +125 | 0001 1111 0100 |

The temperature conversion formulas are as follows:

*Positive Temperature* = *ADC Code*/4

*Negative Temperature* = (4096 − *ADC Code*)/4

The previous formulas are for a $V_{REF}$ of 2.5 V only.

If an external reference is used, the temperature sensor requires an external reference of between 2 V and 2.5 V for correct operation. When an external reference of less than 2.5 V is applied, the temperature results are calculated using the following formula, where $V_{EXT\_REF}$ is the value of the external reference voltage.

$$Temperature = V_{EXT\_REF}\left(\frac{ADCCode}{10} + 109.3\right) - 273.15$$

### $V_{DRIVE}$

The AD7298 also provides the $V_{DRIVE}$ feature. $V_{DRIVE}$ controls the voltage at which the serial interface operates. $V_{DRIVE}$ allows the ADC to easily interface to both 1.8 V and 3 V processors. For example, if the AD7298 is operated with a $V_{DD}$ of 3.3 V, the $V_{DRIVE}$ pin can be powered from a 1.8 V supply.

This enables the AD7298 to operate with a larger dynamic range with a $V_{DD}$ of 3.3 V while still being able to interface to 1.8 V processors. Take care to ensure $V_{DRIVE}$ does not exceed $V_{DD}$ by more than 0.3 V (see the Absolute Maximum Ratings section).

## THE INTERNAL OR EXTERNAL REFERENCE

The AD7298 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The EXT_REF bit in the control register is used to determine whether the internal reference is used. If the EXT_REF bit is selected in the control register, an external reference can be supplied through the $V_{REF}$ pin. On power-up, the internal reference is enabled. Suitable external reference sources for the AD7298 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When the AD7298 operates in internal reference mode, the 2.5 V internal reference is available at the $V_{REF}$ pin, which should be decoupled to GND1 using a 10 µF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system.

The internal reference is capable of sourcing up to 2 mA of current when the converter is static. The reference buffer requires 5.5 ms to power up and charge the 10 µF decoupling capacitor during the power-up time.

# CONTROL REGISTER

The control register of the AD7298 is a 16-bit, write-only register. Data is loaded from the DIN pin of the AD7298 on the falling edge of SCLK. The data is transferred on the DIN line at the same time that the conversion result is read from the part. The data transferred on the DIN line corresponds to the AD7298 configuration for the next conversion. This requires 16 serial clocks for every data transfer. Only the information provided on the first 16 falling clock edges (after the falling edge of $\overline{CS}$) is loaded to the control register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table 7 and Table 8. On power-up, the default content of the control register is all zeros.

**Table 7. Control Register Bit Functions**

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| WRITE | REPEAT | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | $T_{SENSE}$ | DONTC | DONTC | EXT_REF | $T_{SENSE}$AVG | PPD |

**Table 8. Control Register Bit Function Description**

| Bit | Mnemonic | Description |
|---|---|---|
| D15 | WRITE | The value written to this bit determines whether the subsequent 15 bits are loaded to the control register. If this bit is a 1, the following 15 bits are written to the control register; if it is a 0, then the remaining 15 bits are not loaded to the control register and it remains unchanged. |
| D14 | REPEAT | This bit enables the repeated conversion of the selected sequence of channels. |
| D13 to D6 | CH0 to CH7 | These eight channel selection bits are loaded at the end of the current conversion and select which analog input channel is to be converted in the next serial transfer, or they may select the sequence of channels for conversion in the subsequent serial transfers. Each CHX bit corresponds to an analog input channel. A channel or sequence of channels is selected for conversion by writing a 1 to the appropriate CHX bit/bits. Channel address bits corresponding to the conversion result are output on DOUT prior to the 12 bits of data. The next channel to be converted is selected by the mux on the 14th SCLK falling edge. |
| D4 | $T_{SENSE}$ | Writing a 1 to this bit enables the temperature conversion. When the temperature sensor is selected for conversion, the $T_{SENSE}$_BUSY pin goes high after the next CS falling edge to indicate that the conversion is in progress; the previous conversion result can be read while the temperature conversion is in progress. Once $T_{SENSE}$_BUSY goes low, $\overline{CS}$ can be brought low 100 ns later to read the $T_{SENSE}$ conversion result. |
| 4 to 3 | DONTC | Don't care. |
| D2 | EXT_REF | Writing a Logic 1 to this bit, enables the use of an external reference. The input voltage range for the external reference is 1 V to 2.5 V. The external reference should not exceed 2.5 V or the device performance is affected. |
| D1 | $T_{SENSE}$AVG | Writing a 1 to this bit enables the temperature sensor averaging function. When averaging is enabled, the AD7298 internally computes a running average of the conversion results to determine the final $T_{SENSE}$ result (see the Temperature Sensor Averaging section for more details). This mode reduces the influence of noise on the final $T_{SENSE}$ result. Selecting this feature does not automatically select the $T_{SENSE}$ for conversion. The $T_{SENSE}$ bit must also be set to start a temperature sensor conversion. |
| D0 | PPD | This partial power-down mode is selected by writing a 1 to this bit in the control register. In this mode, some of the internal analog circuitry is powered down. The AD7298 retains the information in the control register while in partial power-down mode. The part remains in this mode until a 0 is written to this bit. |

**Table 9. Channel Address Bits**

| ADD3 | ADD2 | ADD1 | ADD0 | Analog Input Channel |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $V_{IN0}$ |
| 0 | 0 | 0 | 1 | $V_{IN1}$ |
| 0 | 0 | 1 | 0 | $V_{IN2}$ |
| 0 | 0 | 1 | 1 | $V_{IN3}$ |
| 0 | 1 | 0 | 0 | $V_{IN4}$ |
| 0 | 1 | 0 | 1 | $V_{IN5}$ |
| 0 | 1 | 1 | 0 | $V_{IN6}$ |
| 0 | 1 | 1 | 1 | $V_{IN7}$ |
| 1 | 0 | 0 | 0 | $T_{SENSE}$ |
| 1 | 0 | 0 | 1 | $T_{SENSE}$ with averaging enabled |

# MODES OF OPERATION

The AD7298 offers different modes of operation that are designed to provide additional flexibility for the user. These options can be chosen by programming the content of the control register to select the desired mode.

## TRADITIONAL MULTICHANNEL MODE OF OPERATION

The AD7298 can operate as a traditional multichannel ADC, where each serial transfer selects the next channel for conversion. One must write to the control register to configure and select the desired input channel prior to initiating any conversions. In the traditional mode of operation, the $\overline{CS}$ signal is used to frame the first write to the converter on the DIN pin. In this mode of operation, the REPEAT bit in the control register is set to a low logic level, 0, thus the REPEAT function is not in use. The data, which appears on the DOUT pin during the initial write to the control register, is invalid. The first $\overline{CS}$ falling edge initiates a write to the control register to configure the device; a conversion is then initiated for the selected analog input channel ($V_{IN0}$) on the subsequent ($2^{nd}$) $\overline{CS}$ falling edge; the third $\overline{CS}$ falling edge will have the result ($V_{IN2}$) available for reading. The AD7298 operates with one cycle latency, thus the conversion result corresponding to each conversion is available one serial read cycle after the cycle in which the conversion was initiated.

As the device operates with one cycle latency, the control register configuration sets up the configuration for the next conversion, which is initiated on the next $\overline{CS}$ falling edge, but the first bit of the corresponding result is not clocked out until the subsequent falling $\overline{CS}$ edge, as shown in Figure 25.

If more than one channel is selected in the control register, the AD7298 converts all selected channels sequentially in ascending order on successive $\overline{CS}$ falling edges. Once all the selected channels in the control register are converted, the AD7298 ceases converting until the user rewrites to the control register to select the next channel for conversion. This operation is shown in Figure 26. DOUT returns all 1s if the sequence of conversions is completed or if no channel is selected.

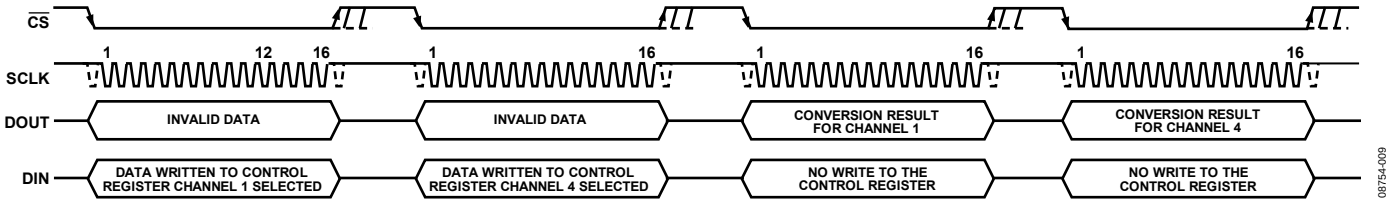



*Figure 25. Configuring a Conversion and Read with the AD7298. One channel selected for conversion.*

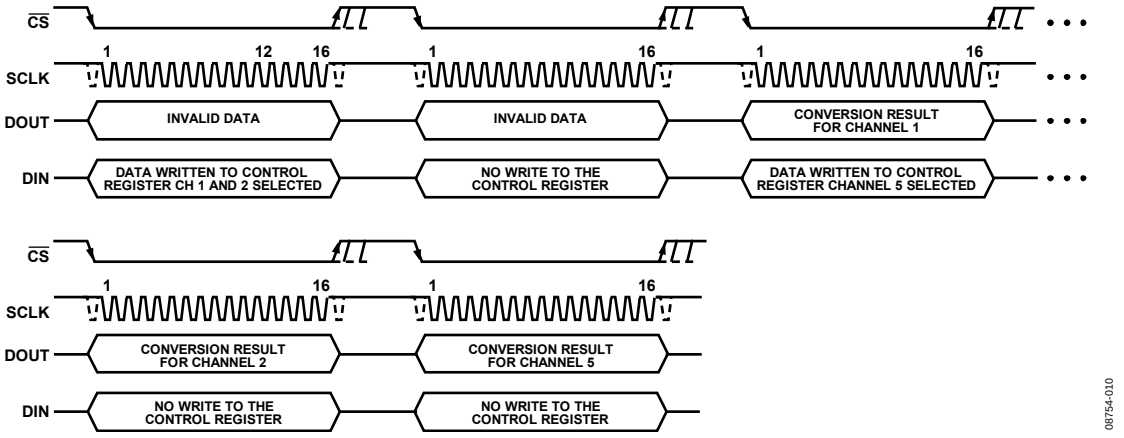



*Figure 26. Configuring a Conversion and Read with the AD7298. Numerous channels selected for conversion.*

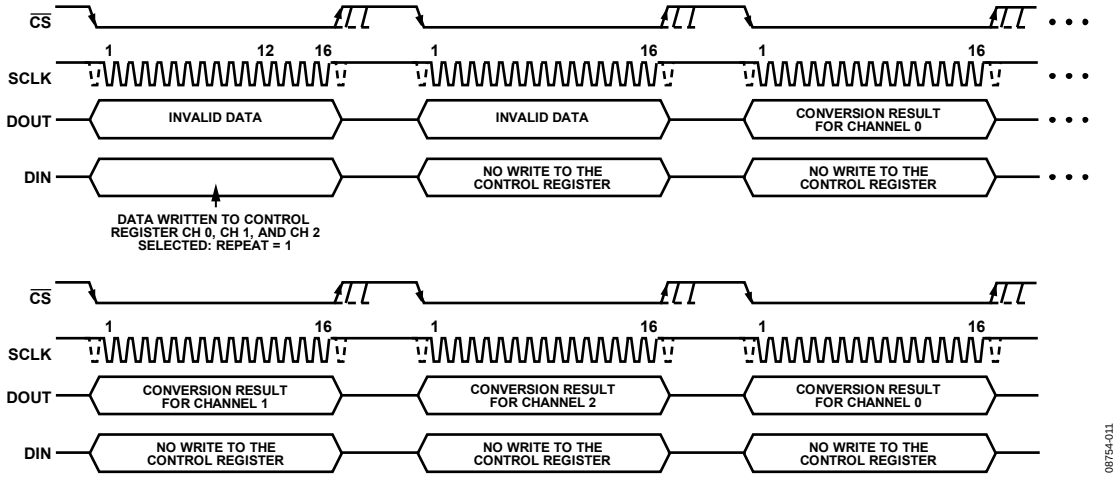



*Figure 27. Configuring a Conversion and Read in Repeat Mode*

## REPEAT OPERATION

The REPEAT bit in the control register allows the user to select a sequence of channels on which the AD7298 continuously converts. When the REPEAT bit is set in the control register, the AD7298 continuously cycles through the selected channels in ascending order, beginning with the lowest channel and converting all channels selected in the control register. On completion of the sequence, the AD7298 returns to the first selected channel in the control register and recommences the sequence.

The conversion sequence of the selected channels in the repeat mode of operation continues until such time as the control register of the AD7298 is reprogrammed. If the $T_{SENSE}$ bit is selected in the control register, then the temperature conversion will be available for conversion after the last analog input channel in the sequence has been converted. It is not necessary to write to the control register once a repeat operation is initiated unless a change in the AD7298 configuration is required. The WRITE bit must be set to zero or the DIN line tied low to ensure that the control register is not accidentally overwritten, or the automatic conversion sequence interrupted.

A write to the control register during the repeat mode of operation resets the cycle even if the selected channels are unchanged. Thus, the next conversion by the AD7298 after a write operation will be the first selected channel in the sequence.

To select a sequence of channels, the associated channel bit must be set to a logic high state (1) for each analog input whose conversion is required. For example, if the REPEAT bit = 1, then CH0, CH1, and CH2 = 1. The $V_{IN0}$ analog input is converted on the first $\overline{CS}$ falling edge following the write to the control register, the $V_{IN1}$ channel is converted on the subsequent $\overline{CS}$ falling edge, and the $V_{IN0}$ conversion result is available for reading. The third $\overline{CS}$ falling edge following the write operation initiates a conversion on $V_{IN2}$ and has the $V_{IN1}$ result available for reading. The AD7298 operates with one cycle latency, thus the conversion result corresponding to each conversion is available one serial read cycle after the cycle in which the conversion is initiated.

This mode of operation simplifies the operation of the device by allowing consecutive channels to be converted without having to reprogram the control register or write to the part on each serial transfer. Figure 27 illustrates how to set up the AD7298 to continuously convert on a particular sequence of channels. To exit the repeat mode of operation and revert back to the traditional mode of operation of a multichannel ADC, ensure that the REPEAT bit = 0 on the next serial write.

## POWER-DOWN MODES

The AD7298 has a number of power conservation modes of operation that are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements. The power-down modes of operation of the AD7298 are controlled by the power-down (PPD) bit in the control register and the $\overline{PD}/\overline{RST}$ pin on the device. When power supplies are first applied to the AD7298, care should be taken to ensure that the part is placed in the required mode of operation

### *Normal Mode*

Normal mode is intended for the fastest throughput rate performance because the user does not have to be concerned about any power-up times because the AD7298 remains fully powered on at all times. Figure 28 shows the general diagram of operation of the AD7298 in this mode. The conversion is initiated on the falling edge of $\overline{CS}$ and the track-and-hold enters hold mode. On the 14th SCLK falling edge, the track-and-hold returns to track mode and starts acquiring the analog input, as described in the Serial Interface section. The data presented to the AD7298 on the DIN line during the first 16 clock cycles of the data transfer are loaded into the control register (provided the WRITE bit is 1). The part remains fully powered up in normal mode at the end of the conversion as long as the PPD bit is set to 0 in the write transfer during that conversion.

To ensure continued operation in normal mode, the PPD bit should be loaded with 0 on every data write operation. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. For specified performance, the throughput rate should not exceed 1 MSPS. Once a conversion is complete and the $\overline{CS}$ has returned high, a minimum of the quiet time, $t_{QUIET}$, must elapse before bringing $\overline{CS}$ low again to initiate another conversion and access the previous conversion result.

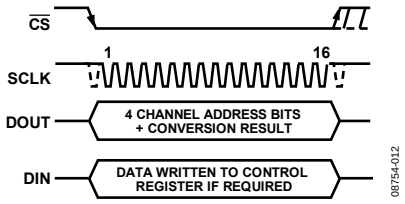



*Figure 28. Normal Mode Operation*

### *Partial Power-Down Mode*

In this mode, part of the internal circuitry on the AD7298 is powered down. The AD7298 enters partial power-down on the $\overline{CS}$ rising edge once the current serial write operation containing 16 SCLK clock cycles is completed. To enter partial power-down, the PPD bit in the control register should be set to 1 on the last required read transfer from the AD7298. Once in partial power-down mode, the AD7298 transmits all 1s on the DOUT pin if $\overline{CS}$ is toggled low. If the averaging feature for the temperature sensor is enabled in the control register, the averaging is reset once the device enters partial power-down mode.

The AD7298 remains in partial power-down until the power-down bit, PPD, in the control register is changed to a logic level zero (0). The AD7298 begins powering up on the rising edge of $\overline{CS}$ following the write to the control register disabling the power-down bit. Once $t_{QUIET}$ has elapsed, a full 16-SCLK write to the control register must be completed to update its content with the desired channel configuration for the subsequent conversion. A valid conversion is then initiated on the next $\overline{CS}$ falling edge.

Because the AD7298 has one cycle latency, the first conversion result after exiting partial power-down mode is available in the fourth serial transfer, as shown in Figure 29. The first cycle updates the PPD bit, the second cycle updates the configuration and Channel ID bits, the third completes the conversion, and the fourth accesses the DOUT valid result. The use of this mode enables a reduction in the overall power consumption of the device.

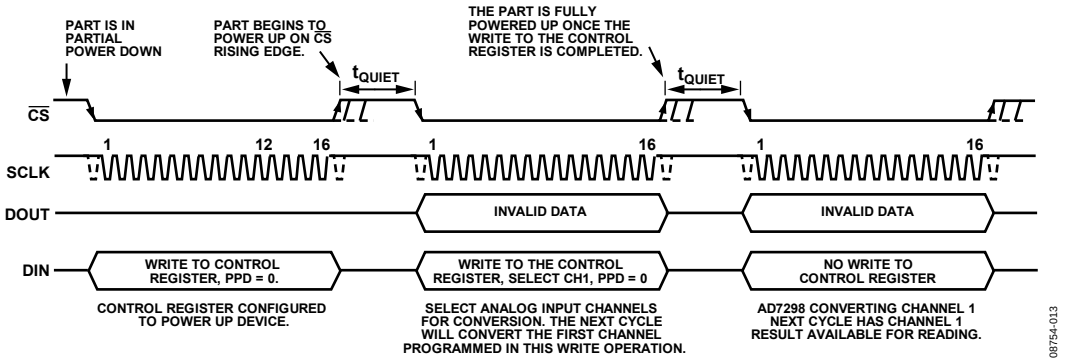



*Figure 29. Partial Power-Down Mode of Operation*

### *Full Power-Down Mode*

In this mode, all internal circuitry on the AD7298 is powered down and no information is retained in the control register or any other internal register. If the averaging feature for the temperature sensor is enabled in the control register ($T_{SENSE}AVG$), the averaging is reset once the device enters power-down mode.

The AD7298 is placed into full power-down mode by bringing the logic level on the $\overline{PD}/\overline{RST}$ pin low for greater than 100 ns. When placing the AD7298 in full power-down mode, the ADC inputs must return to 0 V. The $\overline{PD}/\overline{RST}$ pin is asynchronous to the clock, thus it can be triggered at any time. The part can be powered up for normal operation by bringing the $\overline{PD}/\overline{RST}$ pin logic level back to a high logic state.

The full power-down feature can be used to reduce the average power consumed by the AD7298 when operating at lower throughput rates. The user should ensure that $t_{POWER\_UP}$ has elapsed prior to programming the control register and initiating a valid conversion.

## POWERING UP THE AD7298

The AD7298 contains a power-on reset circuit, which sets the control register to its default setting of all zeros, thus the internal reference is enabled and the device is configured for the normal mode of operation. On power-up, the internal reference is by default enabled, which takes up 6 ms (maximum) to power-up.

If an external reference is being used, the user does not need to wait for the internal reference to power-up fully. The AD7298 digital interface is fully functional after 500 µs from initial power-up. Therefore, the user can write to the control register after 500 µs to switch to external reference mode. The AD7298 is then immediately ready to convert once the external reference is available on the $V_{REF}$ pin.

When supplies are first applied to the AD7298, the user must wait the specified 500 µs before programming the control register to select the desired channels for conversion.

## RESET

The AD7298 includes a reset feature that can be used to reset the device and the contents of all internal registers, including the control register, to their default state.

To activate the reset operation, the $\overline{PD}/\overline{RST}$ pin should be brought low for no longer than 100 ns. It is asynchronous with the clock, thus it can be triggered at any time. If the $\overline{PD}/\overline{RST}$ pin is held low for greater than 100 ns, the part enters full power-down mode. It is imperative that the $\overline{PD}/\overline{RST}$ pin be held at a stable logic level at all times to ensure normal operation.

# SERIAL INTERFACE

Figure 30 shows the detailed timing diagram for the serial interface to the AD7298. The serial clock provides the conversion clock and controls the transfer of information to and from the AD7298 during each conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode at which point the analog input is sampled and the bus is taken out of three-state. The conversion is also initiated at this point and requires 16 SCLK cycles to complete. The track-and-hold goes back into track on the 14th SCLK falling edge as shown in Figure 30 at Point B. On the 16th SCLK falling edge or on the rising edge of $\overline{CS}$ , the DOUT line goes back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion is terminated, the DOUT line goes back into tri-state, and the control register is not updated; otherwise, DOUT returns to three-state on the 16th SCLK falling edge. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7298.

For the AD7298, four-channel address bits (ADD3 to ADD0) that identify which channel the conversion result corresponds to precede the 12 bits of data (see Table 9).

The $\overline{CS}$ going low provides the first address bit to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with a second address bit. Thus, the first falling clock edge on the serial clock has the first address bit provided for reading and also clocks out the second address bit. The three remaining address bits and 12 data bits are clocked out by subsequent SCLK falling edges. The final bit in the data transfer is valid for reading on the 16th falling edge having been clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge depending on the SCLK frequency. The first rising edge of SCLK after the $\overline{CS}$ falling edge would have the first address bit provided, and the 15th rising SCLK edge would have last data bit provided.

Writing information to the control register takes place on the first 16 falling edges of SCLK in a data transfer, assuming the MSB (that is, the WRITE bit) has been set to 1. The 16-bit word read from the AD7298 always contains four channel address bits that the conversion result corresponds to, followed by the 12-bit conversion result.

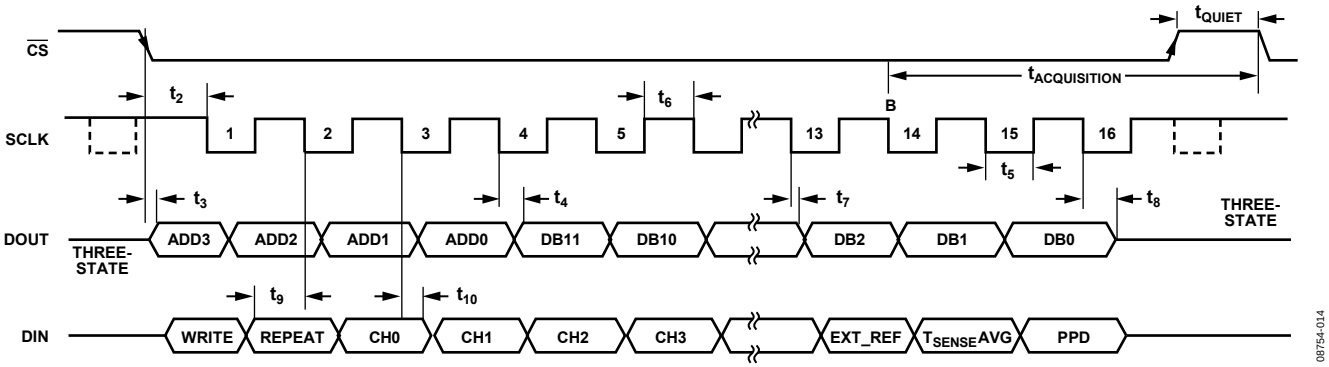



*Figure 30. Serial Interface Timing Diagram*

## TEMPERATURE SENSOR READ

The temperature sensor conversion involves two phases, the integration phase and the conversion phase as detailed in the Temperature Sensor Operation section. The integration phase is initiated on the falling edge of $\overline{CS}$ and once completed the conversion is automatically initiated internally by the AD7298. When a temperature conversion integration is initiated, the $T_{SENSE}$_BUSY signal goes high to indicate that a temperature conversion is in progress and remains high until the conversion is completed.

The total time to measure and convert a temperature channel with the AD7298 is 100 µs max. Once the $T_{SENSE}$_BUSY signal goes low to indicate that the temperature conversion is completed, 100 ns must elapse prior to the next falling edge of $\overline{CS}$. If a minimum of 100 ns is not adhered to between the falling edge of $T_{SENSE}$_BUSY and the subsequent falling edge of $\overline{CS}$, the next conversion will be corrupted but the temperature result that is framed by the $\overline{CS}$ will not be affected. This restriction is in place to ensure that sufficient acquisition time is allowed for the next conversion.

Once the $T_{SENSE}$_BUSY signal goes high, the user may provide a $\overline{CS}$ falling edge to frame the read of the previous conversion and program the control register if required (see Figure 31).

Once the previous conversion result has been read, any subsequent $\overline{CS}$ falling edges which occur while the $T_{SENSE}$_BUSY signal is high are internally ignored by the AD7298. If additional $\overline{CS}$ falling edges are provided while $T_{SENSE}$_BUSY is high, the AD7298 provides an invalid digital output of all 1s.

Alternatively, if $\overline{CS}$ remains high while $T_{SENSE}$_BUSY is high, then the DOUT bus remains in three-state.

If the user writes to the control register during the first 16 SCLK cycles following $T_{SENSE}$_BUSY going high, the configuration of the device for the next conversion, which is initiated on the subsequent $\overline{CS}$ falling edge after $T_{SENSE}$_BUSY goes low, is altered. If the user configures the part for partial power-down in a write to the control register during the first 16 SCLK cycles following $T_{SENSE}$_BUSY going high, the temperature sensor conversion is aborted and the part enters partial power-down on the 16$^{th}$ SCLK falling edge.

Thus, it is recommended not to write to the control register if the $\overline{CS}$ signal will be toggling while $T_{SENSE}$_BUSY is high. Care should be taken to ensure that the WRITE bit is set to zero during the temperature conversion phase when $\overline{CS}$ is toggling.

If an SCLK frequency of more than 10 kHz is used, the temperature conversion requires more than one standard read cycle to complete. In this case, the user can monitor the $T_{SENSE}$_BUSY signal to determine when the conversion is completed and the result is available for reading.

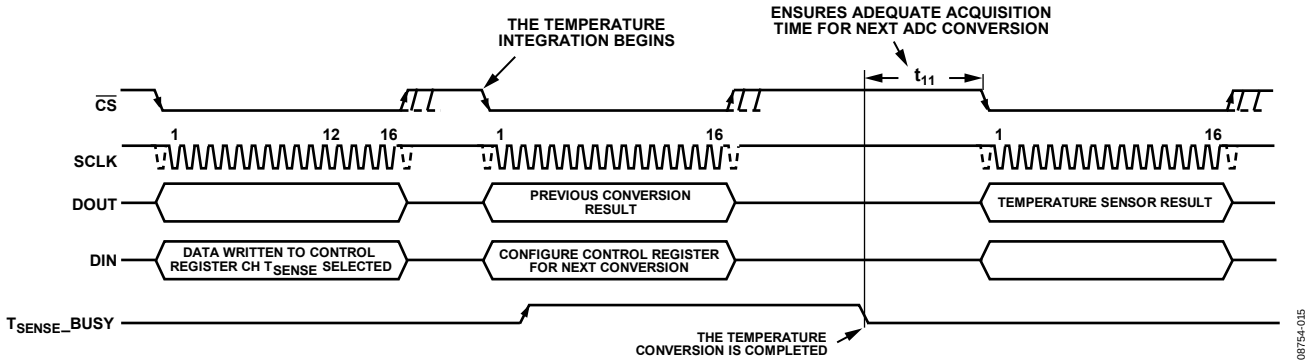



*Figure 31. Serial Interface Timing Diagram for the Temperature Sensor Conversion*

# LAYOUT AND CONFIGURATION

## POWER SUPPLY BYPASSING AND GROUNDING

For optimum performance, carefully consider the power supply and ground return layout on any PCB where the AD7298 is used. The PCB containing the AD7298 should have separate analog and digital sections, each having its own area of the board. The AD7298 should be located in the analog section on any PCB.

Decouple the power supply to the AD7298 to ground with 10 μF and 0.1 μF capacitors. Place the capacitors as physically close as possible to the device, with the 0.1 μF capacitor ideally right up against the device. It is important that the 0.1 μF capacitor have low effective series resistance (ESR) and low effective series inductance (ESL); common ceramic types of capacitors are suitable. The 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching. The 10 μF capacitors are the tantalum bead type.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other components with fast switching digital signals from other parts of the board by a digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board.

The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side; however, this is not always possible with a 2-layer board.

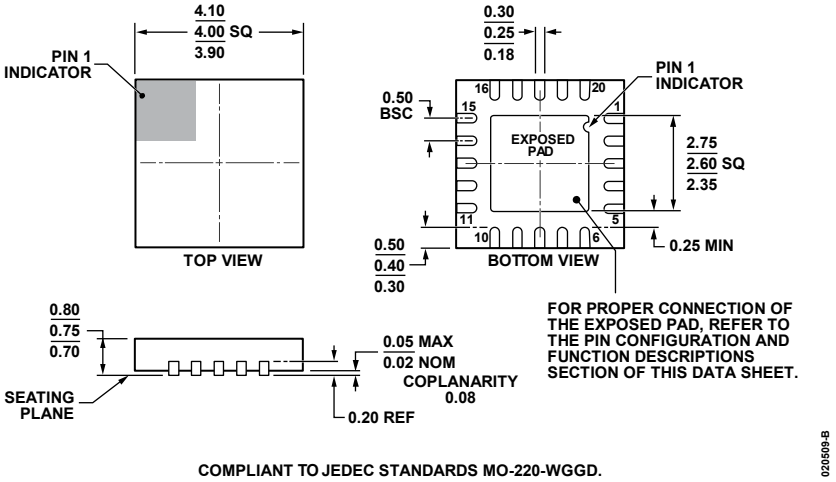
## TEMPERATURE MONITORING

The AD7298 is ideal for monitoring the thermal environment. The die accurately reflects the exact thermal conditions that affect nearby integrated circuits. The AD7298 measures and converts the temperature at the surface of its own semiconductor chip.

When it is used to measure the temperature of a nearby heat source, the thermal impedance between the heat source and the AD7298 must be considered. When the thermal impedance is determined, the temperature of the heat source can be inferred from the AD7298 output.

As much as 60% of the heat transferred from the heat source to the thermal sensor on the AD7298 die is discharged via the copper tracks and the bond pads. Of the pads on the AD7298, the GND pad transfers most of the heat. Therefore, to measure the temperature of a heat source, it is recommended that the thermal resistance between the AD7298 GND pad and the GND of the heat source be reduced as much as possible.

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

*Figure 32. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]*
*4 mm × 4 mm Body, Very, Very Thin Quad*
*(CP-20-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7298BCPZ | −40°C to +125°C | 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-20-8 |
| AD7298BCPZ-RL7 | −40°C to +125°C | 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-20-8 |
| EVAL-AD7298SDZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.