

## Selection Guide

Part Number	Package	Packing	Ambient
A6841EA-T	18-pin DIP	21 pieces per tube	-40°C to 85°C
A6841ELW-T <sup>1,2</sup>	18-pin wide body SOIC	41 pieces per tube	
A6841ELWTR-T <sup>1,2</sup>	18-pin wide body SOIC	1000 pieces per reel	
A6841ELW-20-T	20-pin wide body SOIC	37 pieces per tube	
A6841ELWTR-20-T	20-pin wide body SOIC	1000 pieces per reel	
A6841SA-T	18-pin DIP	21 pieces per tube	-20°C to 85°C
A6841SLW-T <sup>1,2</sup>	18-pin wide body SOIC	41 pieces per tube	
A6841SLWTR-T <sup>1,2</sup>	18-pin wide body SOIC	1000 pieces per reel	
A6841SLW-20-T	20-pin wide body SOIC	37 pieces per tube	
A6841SLWTR-20-T	20-pin wide body SOIC	1000 pieces per reel	

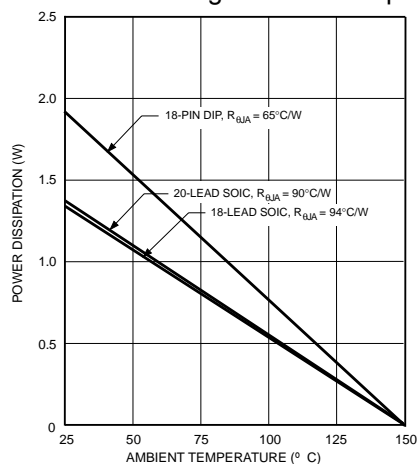
<sup>1</sup>18-pin SOIC variants are pin-for-pin compatible with the 20-pin SOIC variants that are replacing them. The 20-pin variants have two additional pins, at one end, which are not internally connected. The 18-pin variants are being discontinued due to limited demand.

<sup>2</sup>Certain variants cited in this footnote are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The variants should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change April 30, 2007. Deadline for receipt of LAST TIME BUY orders is August 24, 2007. These variants include: A6841ELW-T, A6841ELWTR-T, A6841SLW-T, and A6841SLWTR-T.

## Absolute Maximum Ratings\*

Characteristic	Symbol	Notes	Rating	Units
Logic Supply Voltage	$V_{DD}$		7	V
Emitter Supply Voltage	$V_{EE}$		-20	V
Input Voltage Range	$V_{IN}$		-0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_{CE}$		50	V
	$V_{CE(SUS)}$	For inductive load applications	35	V
Continuous Output Current	$I_{OUT}$	Each output	500	mA
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	°C
		Range S	-20 to 85	°C
Maximum Junction Temperature	$T_J(max)$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.

Allowable Package Power Dissipation,  $P_D$ 




**ELECTRICAL CHARACTERISTICS<sup>1</sup>** Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{EE} = 0\text{ V}$ , logic supply operating voltage  $V_{DD} = 3.0\text{ to }5.5\text{ V}$

Characteristic	Symbol	Test Conditions	$V_{dd} = 3.3\text{ V}$			$V_{dd} = 5\text{ V}$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	$I_{CEX}$	$V_{OUT} = 50\text{ V}$	–	–	10	–	–	10	$\mu\text{A}$
Output Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = 350\text{ mA}$ , $L = 3\text{ mH}$	35	–	–	35	–	–	V
Collector–Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{ mA}$	–	–	1.1	–	–	1.1	V
		$I_{OUT} = 200\text{ mA}$	–	–	1.3	–	–	1.3	V
		$I_{OUT} = 350\text{ mA}$	–	–	1.6	–	–	1.6	V
Input Voltage	$V_{IN(1)}$		2.2	–	–	3.3	–	–	V
	$V_{IN(0)}$		–	–	1.1	–	–	1.7	V
Input Resistance	$R_{IN}$		50	–	–	50	–	–	k $\Omega$
Serial Data Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -200\text{ }\mu\text{A}$	2.8	3.05	–	4.5	4.75	–	V
	$V_{OUT(0)}$	$I_{OUT} = 200\text{ }\mu\text{A}$	–	0.15	0.3	–	0.15	0.3	V
Maximum Clock Frequency <sup>2</sup>	$f_c$		10	–	–	10	–	–	MHz
Logic Supply Current	$I_{DD(1)}$	One output on, OE = L, ST = H	–	–	2.0	–	–	2.0	mA
	$I_{DD(0)}$	All outputs off, OE = H, ST = H, P1 through P8 = L	–	–	100	–	–	100	$\mu\text{A}$
Clamp Diode Leakage Current	$I_r$	$V_r = 50\text{ V}$	–	–	50	–	–	50	$\mu\text{A}$
Clamp Diode Forward Voltage	$V_f$	$I_f = 350\text{ mA}$	–	–	2	–	–	2	V
Output Enable-to-Output Delay	$t_{dis(BQ)}$	$V_{CC} = 50\text{ V}$ , $R_1 = 500\text{ }\Omega$ , $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	$\mu\text{s}$
	$t_{en(BQ)}$	$V_{CC} = 50\text{ V}$ , $R_1 = 500\text{ }\Omega$ , $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	$\mu\text{s}$
Strobe-to-Output Delay	$t_{p(STH-QL)}$	$V_{CC} = 50\text{ V}$ , $R_1 = 500\text{ }\Omega$ , $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	$\mu\text{s}$
	$t_{p(STH-QH)}$	$V_{CC} = 50\text{ V}$ , $R_1 = 500\text{ }\Omega$ , $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	$\mu\text{s}$
Output Fall Time	$t_f$	$V_{CC} = 50\text{ V}$ , $R_1 = 500\text{ }\Omega$ , $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	$\mu\text{s}$
Output Rise Time	$t_r$	$V_{CC} = 50\text{ V}$ , $R_1 = 500\text{ }\Omega$ , $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	$\mu\text{s}$
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	$I_{OUT} = \pm 200\text{ }\mu\text{A}$	–	50	–	–	50	–	ns

<sup>1</sup>Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.

<sup>2</sup>Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

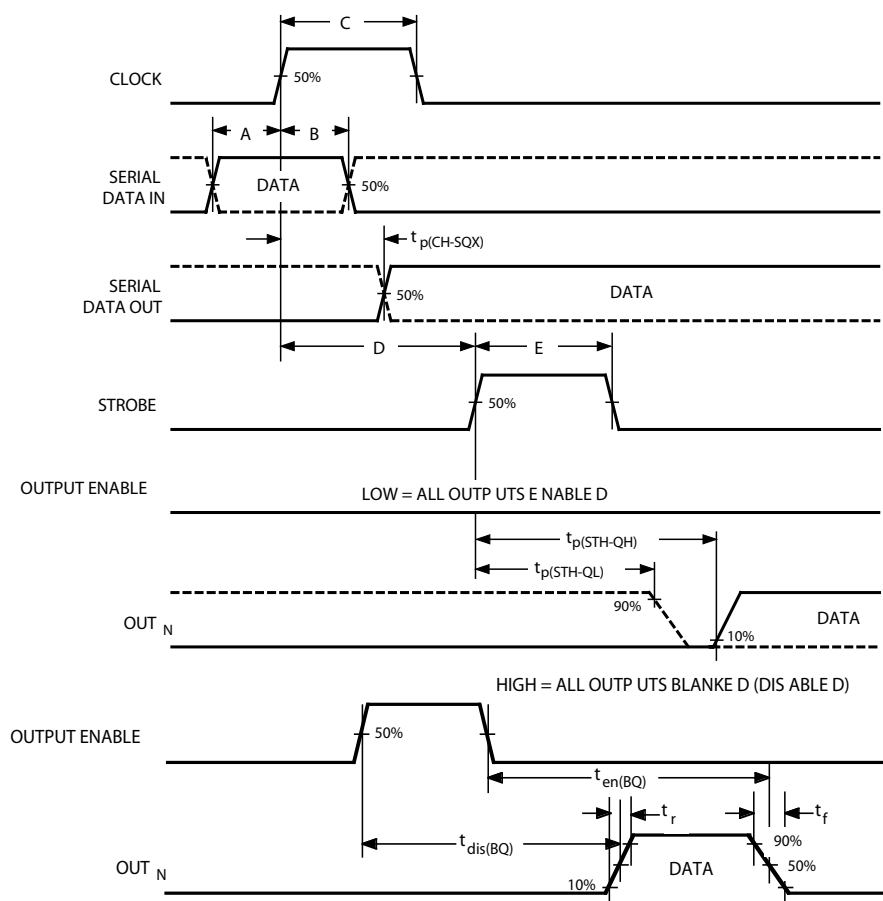
Truth Table

Serial Data Input	Clock Input	Shift Register Contents					Serial Data Output	Strobe Input	Latch Contents					Output Enable Input	Output Contents				
		$I_1$	$I_2$	$I_3$	...	$I_8$			$I_1$	$I_2$	$I_3$	...	$I_8$		$I_1$	$I_2$	$I_3$	...	$I_8$
H		H	$R_1$	$R_2$	...	$R_7$	$R_7$												
L		L	$R_1$	$R_2$	...	$R_7$	$R_7$												
X		$R_1$	$R_2$	$R_3$	...	$R_8$	$R_8$												
		X	X	X	...	X	X	L	$R_1$	$R_2$	$R_3$	...	$R_8$						
		$P_1$	$P_2$	$P_3$	...	$P_8$	$P_8$	H	$P_1$	$P_2$	$P_3$	...	$P_8$	L	$P_1$	$P_2$	$P_3$	...	$P_8$
									X	X	X	...	X	H	H	H	...	H	

L = Low Logic Level  
H = High Logic Level  
X = Irrelevant

P = Present State  
R = Previous State

### Timing Requirements and Specifications (Logic Levels are $V_{DD}$ and Ground)



Key	Description	Symbol	Time (ns)
A	Data Active Time Before Clock Pulse (Data Set-Up Time)	$t_{su(D)}$	25
B	Data Active Time After Clock Pulse (Data Hold Time)	$t_{h(D)}$	25
C	Clock Pulse Width	$t_{w(CH)}$	50
D	Time Between Clock Activation and Strobe	$t_{su(C)}$	100
E	Strobe Pulse Width	$t_{w(STH)}$	50

NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

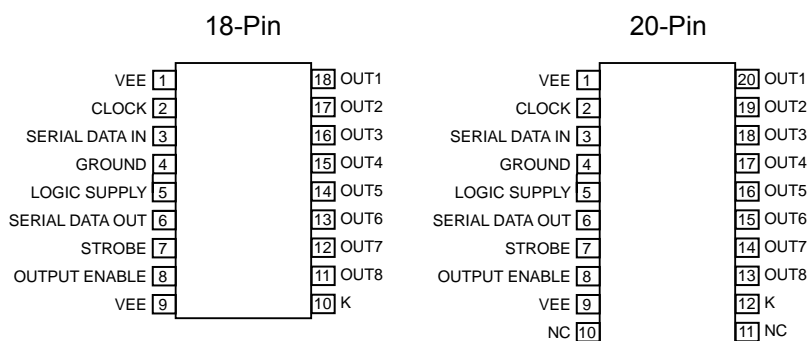
Powering-on with the inputs in the low state ensures that the registers and latches power-on in the low state (POR).

Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The serial data must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF). The information stored in the latches or shift register is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

## Pin-out Diagrams

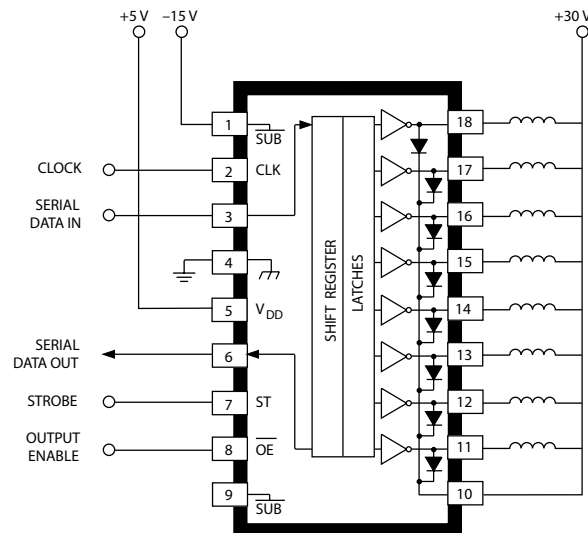


The 18-pin and 20-pin packages are electrically identical. They share common terminal assignments, except for the two NC pins on the 20-pin variant.

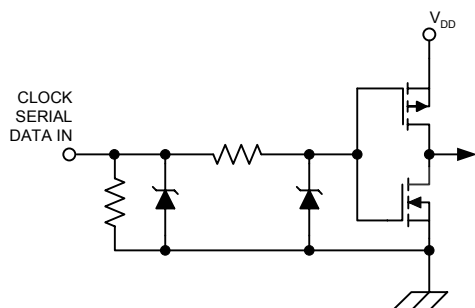
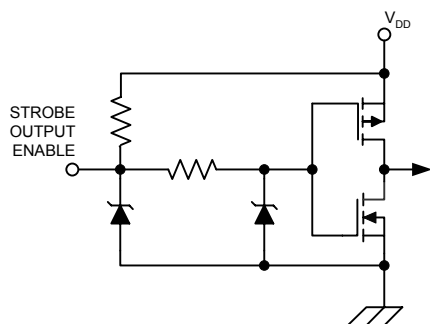
Terminal List Table

Name	Description	Pin	
		18-pin	20-pin
VEE	Power Ground to substrate	1, 9	1, 9
CLOCK	Clock	2	2
SERIAL DATA IN	Serial Data In	3	3
GROUND	Logic Ground	4	4
VDD	Logic Supply	5	5
SERIAL DATA OUT	Serial Data Out, for cascading devices	6	6
STROBE	Strobe	7	7
OUTPUT ENABLE	Output Enable (active low)	8	8
K	Common to +V <sub>L</sub> , for inductive loads	10	12
NC	Not internally connected	—	10, 11
OUT8	Sink Output 8	11	13
OUT7	Sink Output 7	12	14
OUT6	Sink Output 6	13	15
OUT5	Sink Output 5	14	16
OUT4	Sink Output 4	15	17
OUT3	Sink Output 3	16	18
OUT2	Sink Output 2	17	19
OUT1	Sink Output 1	18	20

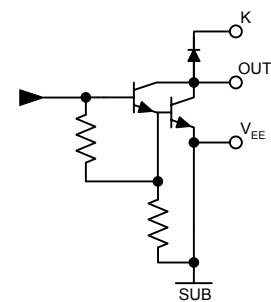
Typical Application  
Relay/solenoid driver using split supply



Typical Input Circuits

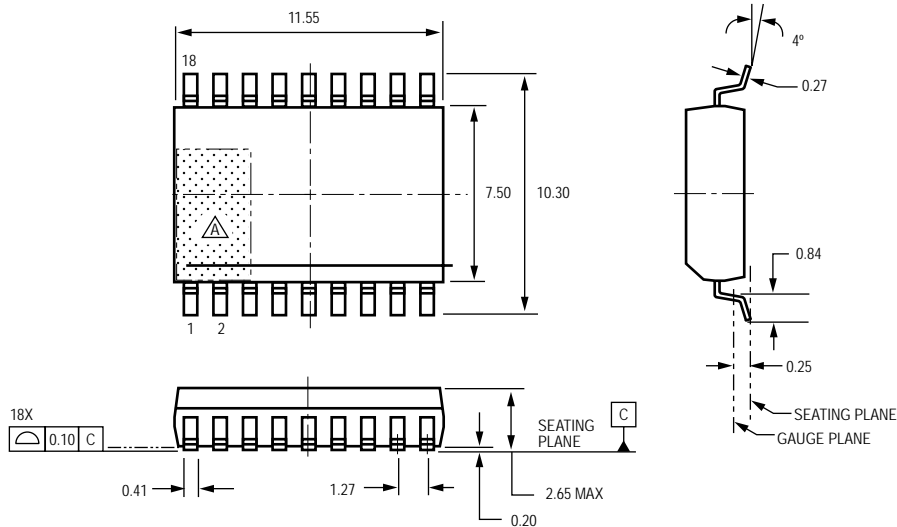


Typical Output Driver



## Package LW

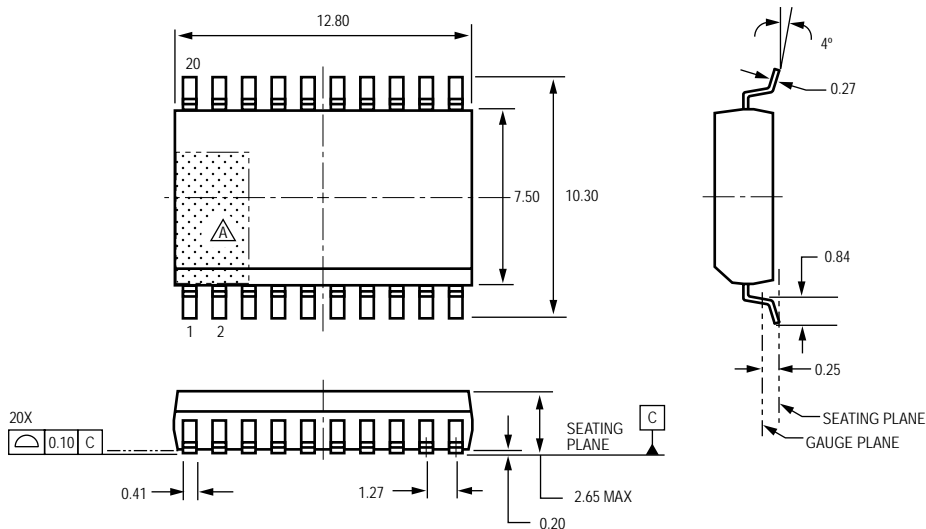
## 18-pin Wide Body SOIC



All dimensions nominal, not for tooling use  
 Dimensions in millimeters  
 (reference JEDEC MS-013 AB)  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown

Terminal #1 mark area

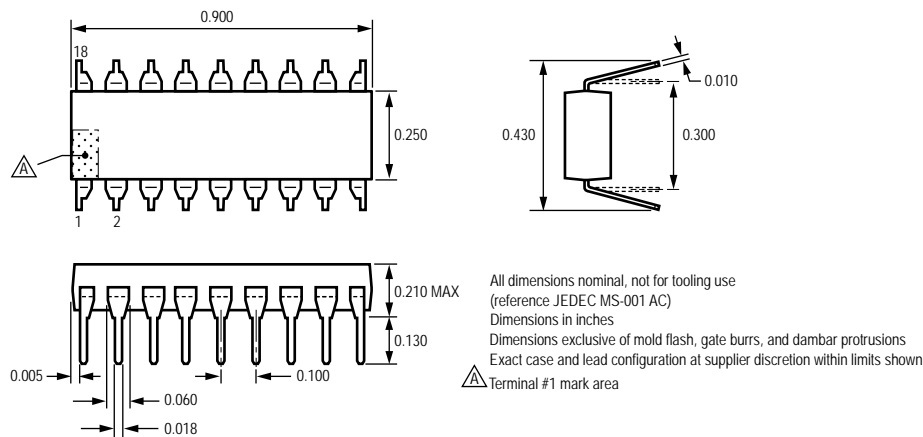
## 20-pin Wide Body SOIC



All dimensions nominal, not for tooling use  
 Dimensions in millimeters  
 (reference JEDEC MS-013 AC)  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown

Terminal #1 mark area

Package A  
18-pin DIP



Copyright ©2004, 2007 Allegro MicroSystems, Inc.

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in life support devices or systems, if a failure of an Allegro product can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website:

[www.allegromicro.com](http://www.allegromicro.com)



Allegro MicroSystems, Inc.  
115 Northeast Cutoff  
Worcester, Massachusetts 01615-0036 U.S.A.  
1.508.853.5000; [www.allegromicro.com](http://www.allegromicro.com)